PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	V_{in}	Positive power supply input voltage.
2	GND	Power supply ground.
3	Enable	This input is used to place the device into low−power standby. When this input is pulled low, the device is disabled. If this function is not used, Enable should be connected to V_{in}.
4	N/C	No Internal Connection.
5	V_{out}	Regulated output voltage.

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input Voltage		V_{in}	0 to 12	V
Enable Voltage		V_{EN}	−0.3 to V_{in} +0.3	V
Output Voltage		V_{out}	−0.3 to V_{in} +0.3	V
Power Dissipation		P_D	Internally Limited	W
Operating Junction Temperature		T_J	+150	°C
Operating Ambient Temperature	NCP551 NCV551	T_A	−40 to +85 −40 to +125	°C
Storage Temperature		T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model 2000 V per MIL−STD−883, Method 3015
   Machine Model Method 200 V
   Charge Device Model (CDM) tested C3B per EIA/JESD22−C101.
2. Latchup capability (85°C) ±100 mA DC with trigger voltage.

THERMAL CHARACTERISTICS

Rating	Symbol	Test Conditions	Typical Value	Unit
Junction−to−Ambient	$R_{\theta JA}$	1 oz Copper Thickness, 100 mm^2	250	°C/W
PSIJ−Lead 2	Ψ_{J-L2}	1 oz Copper Thickness, 100 mm^2	68	°C/W

NOTE: Single component mounted on an 80 x 80 x 1.5 mm FR4 PCB with stated copper head spreading area. Using the following boundary conditions as stated in EIA/JESD 51−1, 2, 3, 7, 12.

ELECTRICAL CHARACTERISTICS

($V_{in} = V_{out(nom.)} + 1.0$ V, $V_{EN} = V_{in}$, $C_{in} = 1.0$ μF, $C_{out} = 1.0$ μF, $T_A = 25°C$, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage ($T_A = 25°C$, $I_{out} = 10$ mA)	V_{out}				V
1.4 V		1.358	1.4	1.442	
1.5 V		1.455	1.5	1.545	
1.8 V		1.746	1.8	1.854	
2.5 V		2.425	2.5	2.575	
2.7 V		2.646	2.7	2.754	
2.8 V		2.744	2.8	2.856	
2.9 V		2.842	2.9	2.958	
3.0 V		2.940	3.0	3.060	
3.1 V		3.038	3.1	3.162	
3.2 V		3.136	3.2	3.264	
3.3 V		3.234	3.3	3.366	
5.0 V		4.90	5.0	5.10	
Output Voltage ($T_A = T_{low}$ to T_{high}, $I_{out} = 10$ mA)	V_{out}				V
1.4 V		1.344	1.4	1.456	
1.5 V		1.440	1.5	1.560	
1.8 V		1.728	1.8	1.872	
2.5 V		2.400	2.5	2.600	
2.7 V		2.619	2.7	2.781	
2.8 V		2.716	2.8	2.884	
2.9 V		2.813	2.9	2.987	
3.0 V		2.910	3.0	3.090	
3.1 V		3.007	3.1	3.193	
3.2 V		3.104	3.2	3.296	
3.3 V		3.201	3.3	3.399	
5.0 V		4.850	5.0	5.150	
Line Regulation ($V_{in} = V_{out} + 1.0$ V to 12 V, $I_{out} = 10$ mA)	Reg_{line}	–	10	30	mV
Load Regulation ($I_{out} = 10$ mA to 150 mA, $V_{in} = V_{out} + 2.0$ V)	Reg_{load}	–	40	65	mV
Output Current (V_{out} = (V_{out} at $I_{out} = 100$ mA) −3%)	$I_{o(nom.)}$				mA
1.4 V−2.0 V ($V_{in} = 4.0$ V)		150	–	–	
2.1 V−3.0 V ($V_{in} = 5.0$ V)		150	–	–	
3.1 V−4.0 V ($V_{in} = 6.0$ V)		150	–	–	
4.1 V−5.0 V ($V_{in} = 8.0$ V)		150	–	–	
Dropout Voltage ($I_{out} = 10$ mA, Measured at V_{out} −3.0%)	$V_{in}-V_{out}$				mV
1.4 V		–	170	250	
1.5 V, 1.8 V, 2.5 V		–	130	220	
2.7 V, 2.8 V, 2.9 V, 3.0 V, 3.1 V, 3.2 V, 3.3 V, 5.0 V		–	40	150	
Quiescent Current	I_Q				μA
(Enable Input = 0 V)		–	0.1	1.0	
(Enable Input = V_{in}, $I_{out} = 1.0$ mA to $I_{o(nom.)}$)		–	4.0	8.0	
Output Voltage Temperature Coefficient	T_c	–	±100	–	ppm/°C
Enable Input Threshold Voltage	$V_{th(en)}$				V
(Voltage Increasing, Output Turns On, Logic High)		1.3	–	–	
(Voltage Decreasing, Output Turns Off, Logic Low)		–	–	0.3	
Output Short Circuit Current ($V_{out} = 0$ V)	$I_{out(max)}$				mA
1.4 V−2.0 V ($V_{in} = 4.0$ V)		160	350	600	
2.1 V−3.0 V ($V_{in} = 5.0$ V)		160	350	600	
3.1 V−4.0 V ($V_{in} = 6.0$ V)		160	350	600	
4.1 V−5.0 V ($V_{in} = 8.0$ V)		160	350	600	

3. Maximum package power dissipation limits must be observed.

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

4. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. NCP551 $T_{low} = -40°C$ $T_{high} = +85°C$
   NCV551 $T_{low} = -40°C$ $T_{high} = +125°C$.

DEFINITIONS

Load Regulation

The change in output voltage for a change in output current at a constant temperature.

Dropout Voltage

The input/output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. Measured when the output drops 3% below its nominal. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Maximum Power Dissipation

The maximum total dissipation for which the regulator will operate within its specifications.

Quiescent Current

The quiescent current is the current which flows through the ground when the LDO operates without a load on its output: internal IC operation, bias, etc. When the LDO becomes loaded, this term is called the Ground current. It is actually the difference between the input current (measured through the LDO input pin) and the output current.

Line Regulation

The change in output voltage for a change in input voltage. The measurement is made under conditions of low dissipation or by using pulse technique such that the average chip temperature is not significantly affected.

Line Transient Response

Typical over and undershoot response when input voltage is excited with a given slope.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 160°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The maximum power package dissipation is the power dissipation level at which the junction temperature reaches its maximum operating value, i.e. 125°C. Depending on the ambient power dissipation and thus the maximum available output current.

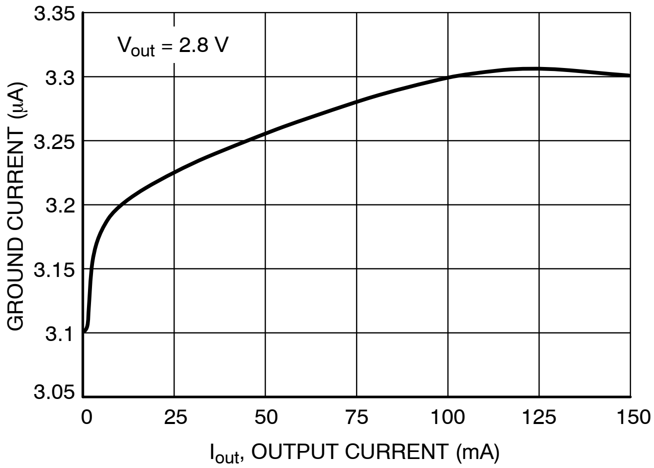


Figure 2. Ground Pin Current versus Output Current

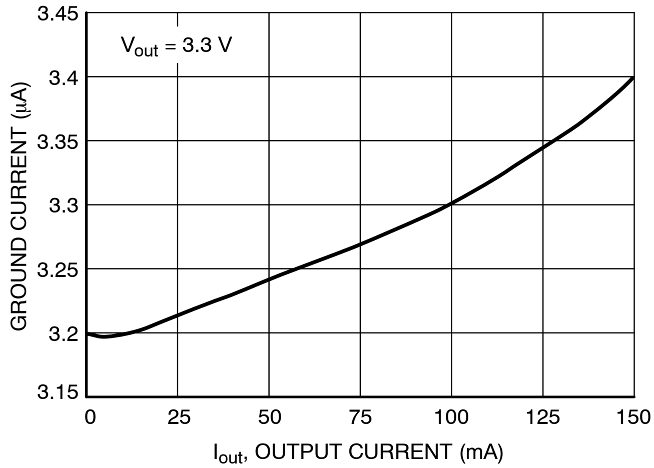


Figure 3. Ground Pin Current versus Output Current

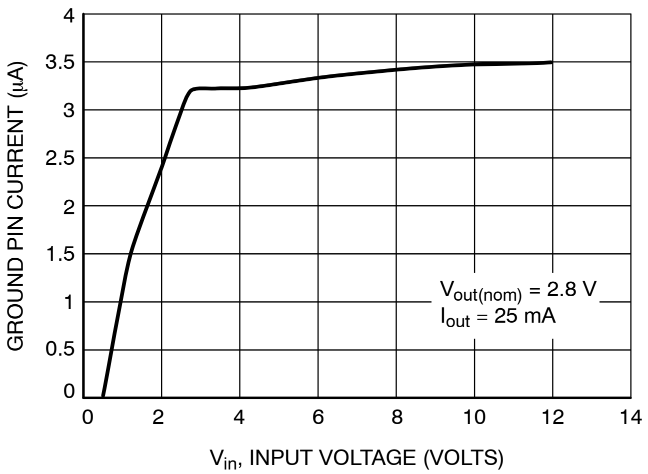


Figure 4. Ground Pin Current versus Input Voltage

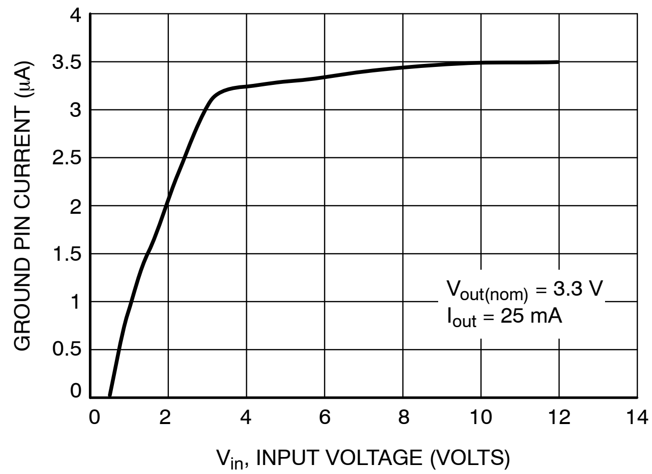


Figure 5. Ground Pin Current versus Input Voltage

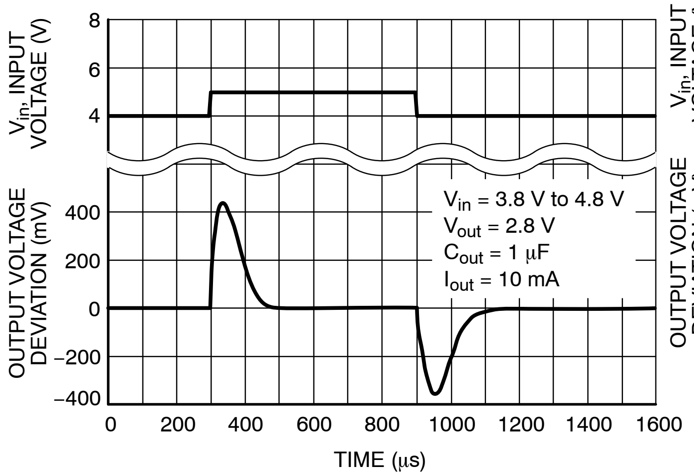


Figure 6. Line Transient Response

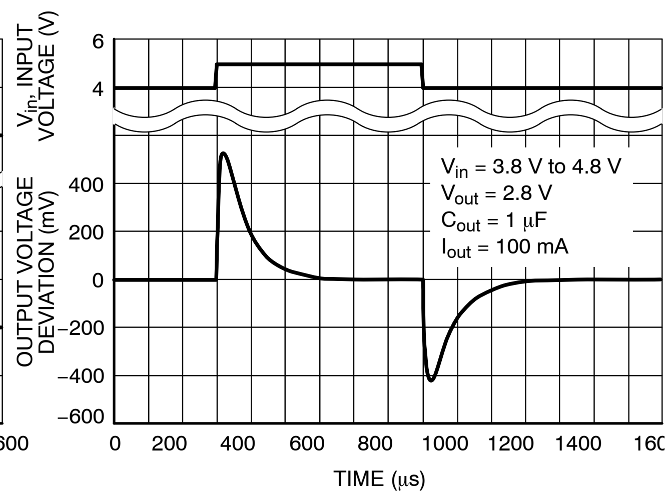


Figure 7. Line Transient Response

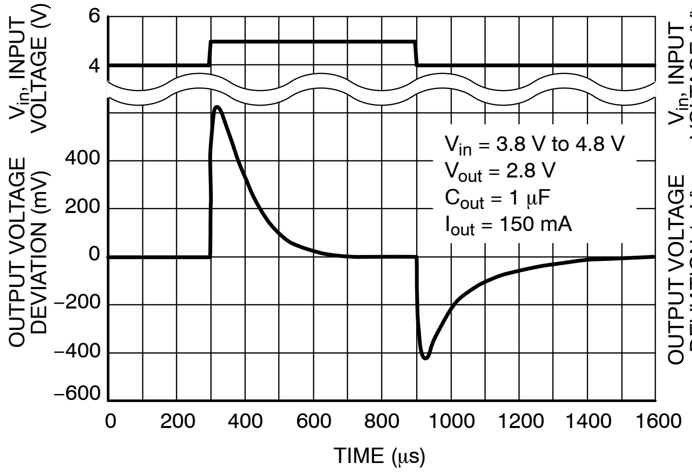


Figure 8. Line Transient Response

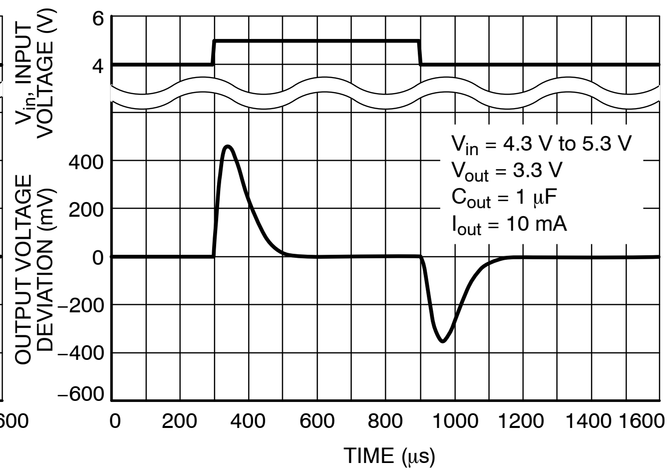


Figure 9. Line Transient Response

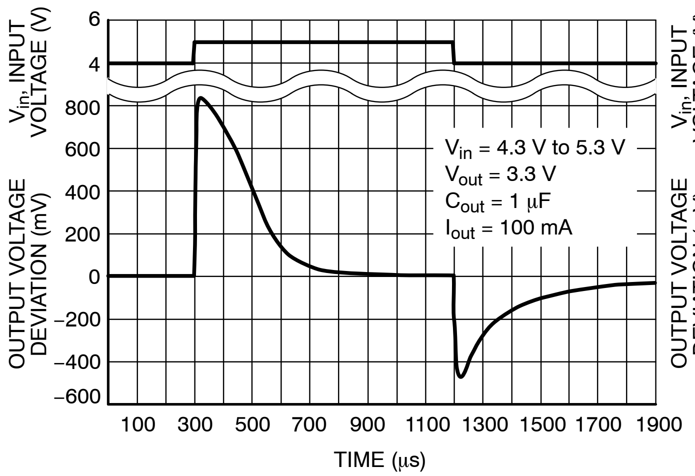


Figure 10. Line Transient Response

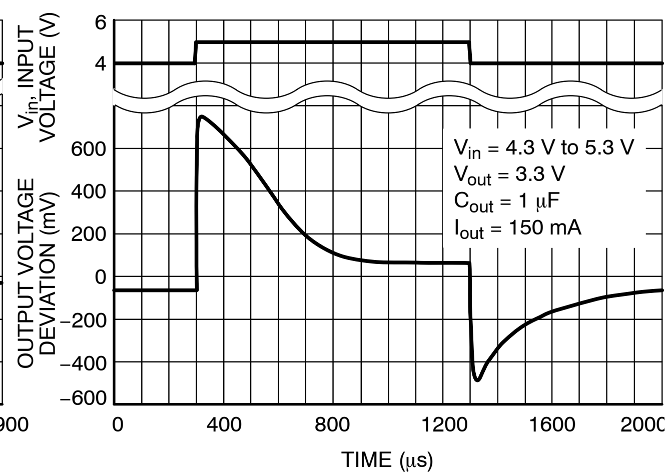


Figure 11. Line Transient Response

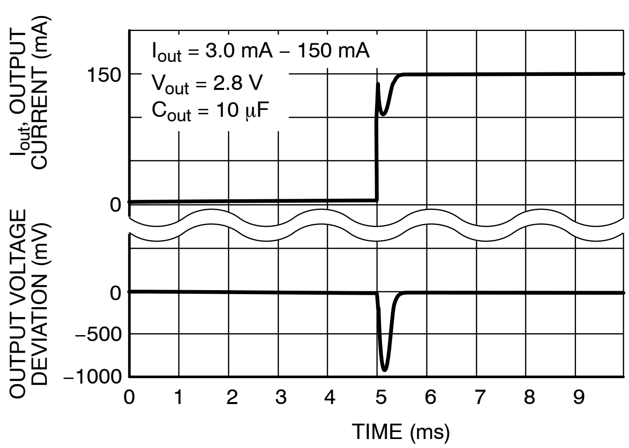


Figure 12. Load Transient Response ON

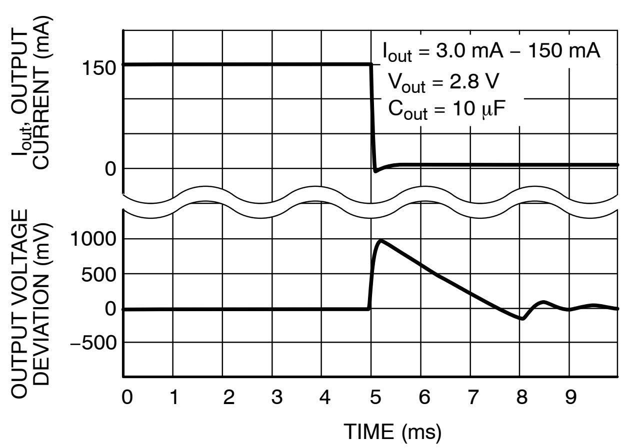


Figure 13. Load Transient Response OFF

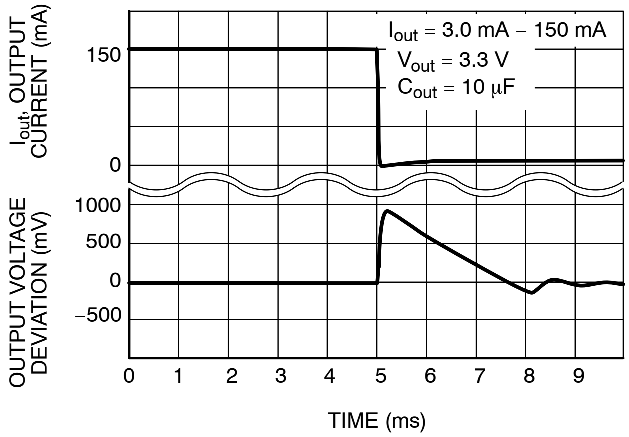


Figure 14. Load Transient Response OFF

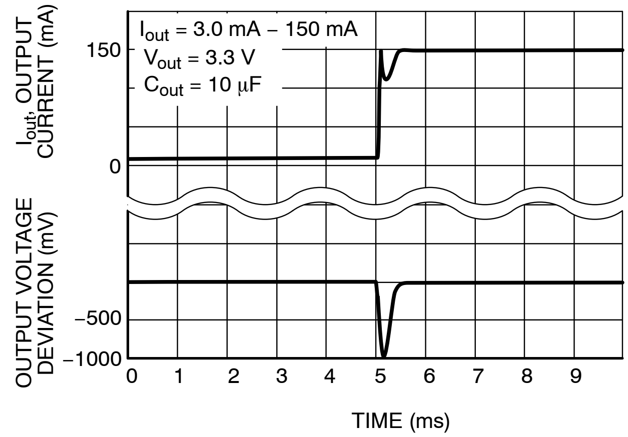


Figure 15. Load Transient Response ON

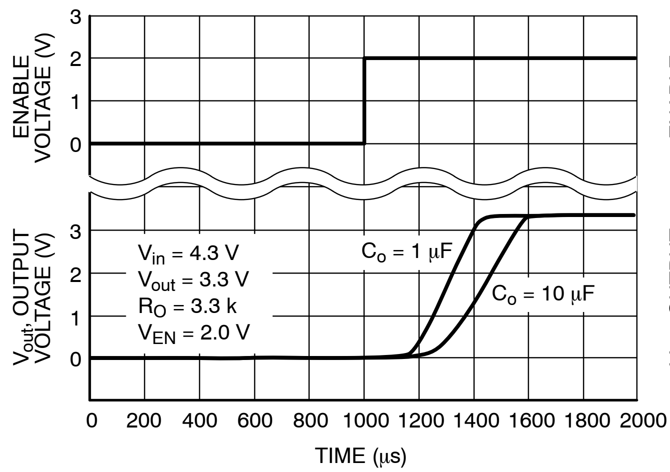


Figure 16. Turn−On Response

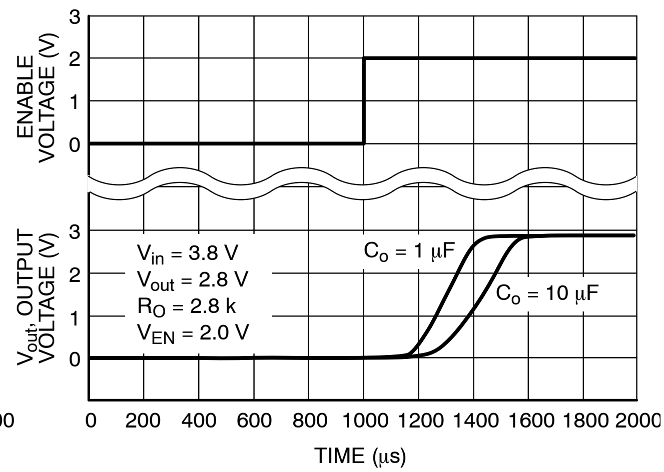


Figure 17. Turn−On Response

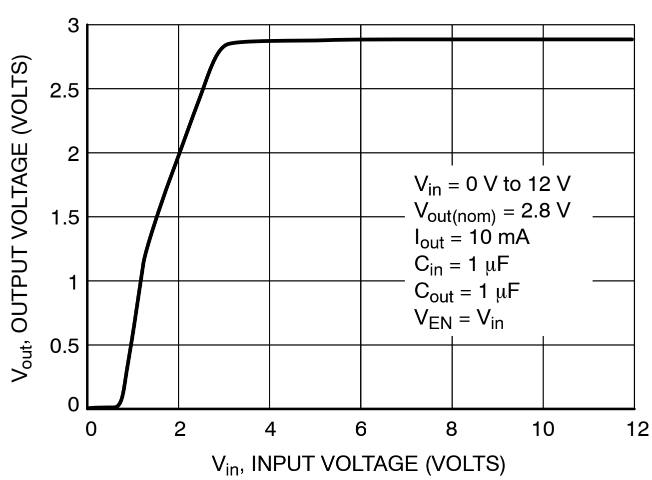


Figure 18. Output Voltage versus Input Voltage

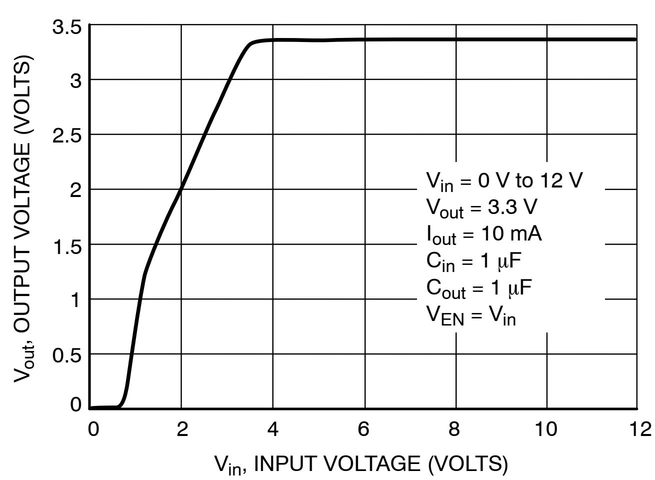


Figure 19. Output Voltage versus Input Voltage

APPLICATIONS INFORMATION

A typical application circuit for the NCP551 series is shown in Figure 20.

Input Decoupling (C1)

A 0.1 μF capacitor either ceramic or tantalum is recommended and should be connected close to the NCP551 package. Higher values and lower ESR will improve the overall line transient response.

Output Decoupling (C2)

The NCP551 is a stable Regulator and does not require any specific Equivalent Series Resistance (ESR) or a minimum output current. Capacitors exhibiting ESRs ranging from a few mΩ up to 3.0 Ω can thus safely be used. The minimum decoupling value is 0.1 μF and can be augmented to fulfill stringent load transient requirements. The regulator accepts ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load regulation transient response.

Enable Operation

The enable pin will turn on or off the regulator. These limits of threshold are covered in the electrical specification section of this data sheet. If the enable is not used then the pin should be connected to V_{in}.

Hints

Please be sure the V_{in} and GND lines are sufficiently wide. When the impedance of these lines is high, there is a chance to pick up noise or cause the regulator to malfunction.

Set external components, especially the output capacitor, as close as possible to the circuit, and make leads as short as possible.

Thermal

As power across the NCP551 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature effect the rate of temperature rise for the part. This is stating that when the NCP551 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power dissipation applications.

The maximum dissipation the package can handle is given by:

$$PD = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

If junction temperature is not allowed above the maximum 125°C, then the NCP551 can dissipate up to 400 mW @ 25°C.

The power dissipated by the NCP551 can be calculated from the following equation:

$$P_{tot} = [V_{in} * I_{gnd}(I_{out})] + [V_{in} - V_{out}] * I_{out}$$

or

$$V_{inMAX} = \frac{P_{tot} + V_{out} * I_{out}}{I_{GND} + I_{out}}$$

If a 150 mA output current is needed then the ground current from the data sheet is 4.0 μA. For an NCP551SN30T1 (3.0 V), the maximum input voltage will then be 5.6 V.

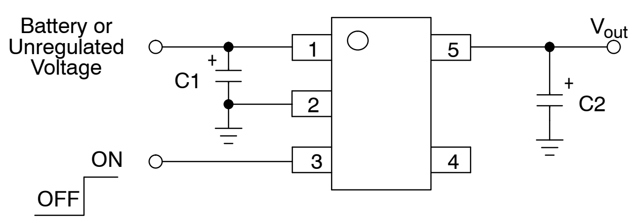


Figure 20. Typical Application Circuit

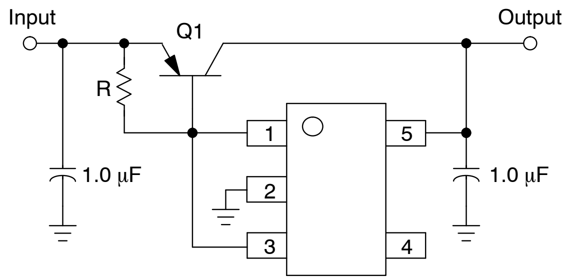


Figure 21. Current Boost Regulator

The NCP551 series can be current boosted with a PNP transistor. Resistor R in conjunction with V_{BE} of the PNP determines when the pass transistor begins conducting; this circuit is not short circuit proof. Input/Output differential voltage minimum is increased by V_{BE} of the pass resistor.

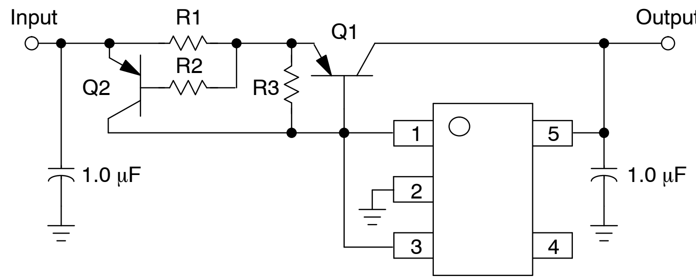


Figure 22. Current Boost Regulator with Short Circuit Limit

Short circuit current limit is essentially set by the V_{BE} of Q2 and R1. $I_{SC} = ((V_{BEQ2} - ib * R2) / R1) + I_{O(max)}$ Regulator

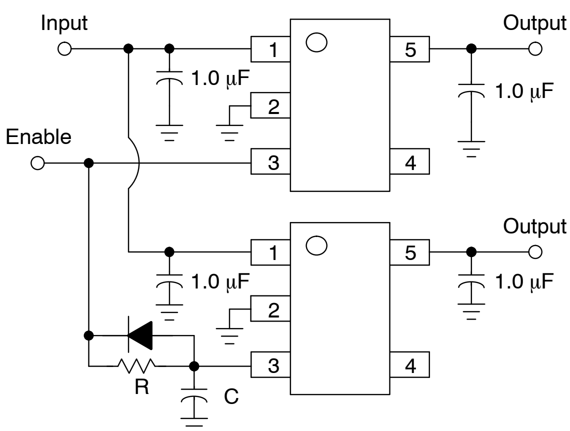


Figure 23. Delayed Turn−on

If a delayed turn−on is needed during power up of several voltages then the above schematic can be used. Resistor R, and capacitor C, will delay the turn−on of the bottom regulator.

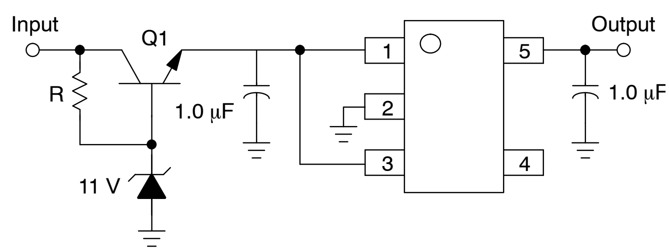


Figure 24. Input Voltages Greater than 12 V

A regulated output can be achieved with input voltages that exceed the 12 V maximum rating of the NCP551 series with the addition of a simple pre−regulator circuit. Care must be taken to prevent Q1 from overheating when the regulated output (V_{out}) is shorted to GND.

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Package	Shipping†
NCP551SN15T1	1.5	LAO	TSOP−5	3000 / Tape & Reel
NCP551SN15T1G	1.5	LAO	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP551SN18T1	1.8	LAP	TSOP−5	3000 / Tape & Reel
NCP551SN18T1G	1.8	LAP	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP551SN25T1	2.5	LAQ	TSOP−5	3000 / Tape & Reel
NCP551SN25T1G	2.5	LAQ	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP551SN27T1	2.7	LAR	TSOP−5	3000 / Tape & Reel
NCP551SN27T1G	2.7	LAR	TSOP−5 (Pb−Free)	3000 / Tape & Reel

NOTE: Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
6. NCV551 is qualified for automotive use.

ORDERING INFORMATION

Device	Nominal Output Voltage	Marking	Package	Shipping†
NCP551SN28T1	2.8	LAS	TSOP−5	3000 / Tape & Reel
NCP551SN28T1G	2.8	LAS	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP551SN29T1G	2.9	LJL	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP551SN30T1	3.0	LAT	TSOP−5	3000 / Tape & Reel
NCP551SN30T1G	3.0	LAT	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP551SN31T1G	3.1	LJM	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP551SN32T1G	3.2	LIV	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP551SN33T1	3.3	LAU	TSOP−5	3000 / Tape & Reel
NCP551SN33T1G	3.3	LAU	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCP551SN50T1	5.0	LAV	TSOP−5	3000 / Tape & Reel
NCP551SN50T1G	5.0	LAV	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV551SN14T1G	1.4	AAT	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV551SN15T1	1.5	LFZ	TSOP−5	3000 / Tape & Reel
NCV551SN15T1G	1.5	LFZ	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV551SN18T1	1.8	LGA	TSOP−5	3000 / Tape & Reel
NCV551SN18T1G	1.8	LGA	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV551SN25T1	2.5	LGB	TSOP−5	3000 / Tape & Reel
NCV551SN25T1G	2.5	LGB	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV551SN27T1	2.7	LGC	TSOP−5	3000 / Tape & Reel
NCV551SN27T1G	2.7	LGC	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV551SN28T1	2.8	LGD	TSOP−5	3000 / Tape & Reel
NCV551SN28T1G	2.8	LGD	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV551SN30T1	3.0	LGE	TSOP−5	3000 / Tape & Reel
NCV551SN30T1G	3.0	LGE	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV551SN31T1G	3.1	LJR	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV551SN32T1	3.2	LFR	TSOP−5	3000 / Tape & Reel
NCV551SN32T1G	3.2	LFR	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV551SN33T1	3.3	LGG	TSOP−5	3000 / Tape & Reel
NCV551SN33T1G	3.3	LGG	TSOP−5 (Pb−Free)	3000 / Tape & Reel
NCV551SN50T1	5.0	LGF	TSOP−5	3000 / Tape & Reel
NCV551SN50T1G	5.0	LGF	TSOP−5 (Pb−Free)	3000 / Tape & Reel

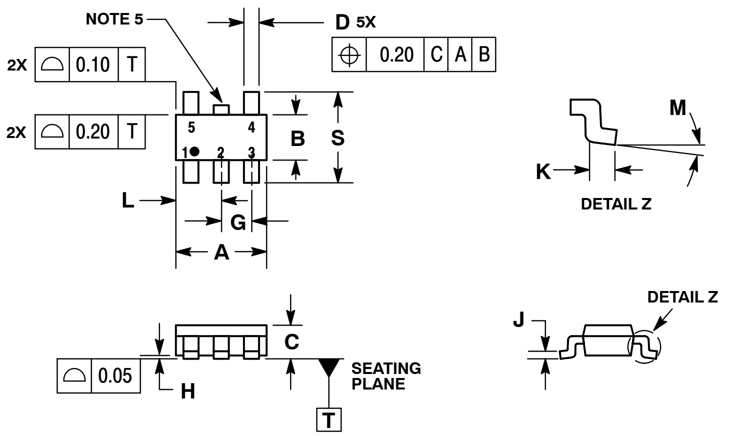
NOTE: Additional voltages in 100 mV steps are available upon request by contacting your ON Semiconductor representative.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

6. NCV551 is qualified for automotive use.

PACKAGE DIMENSIONS

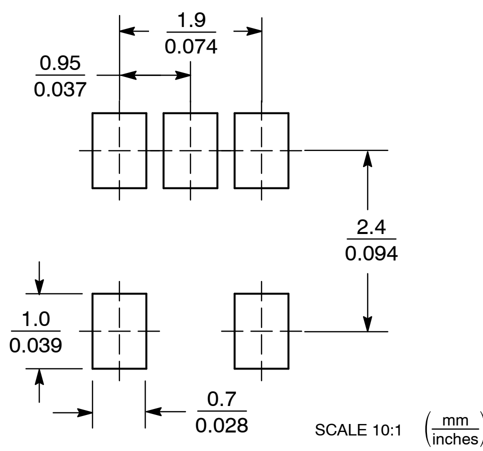
TSOP−5
CASE 483−02
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

	MILLIMETERS	
DIM	MIN	MAX
A	3.00 BSC	
B	1.50 BSC	
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
L	1.25	1.55
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
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