# INTERNAL BLOCK DIAGRAM

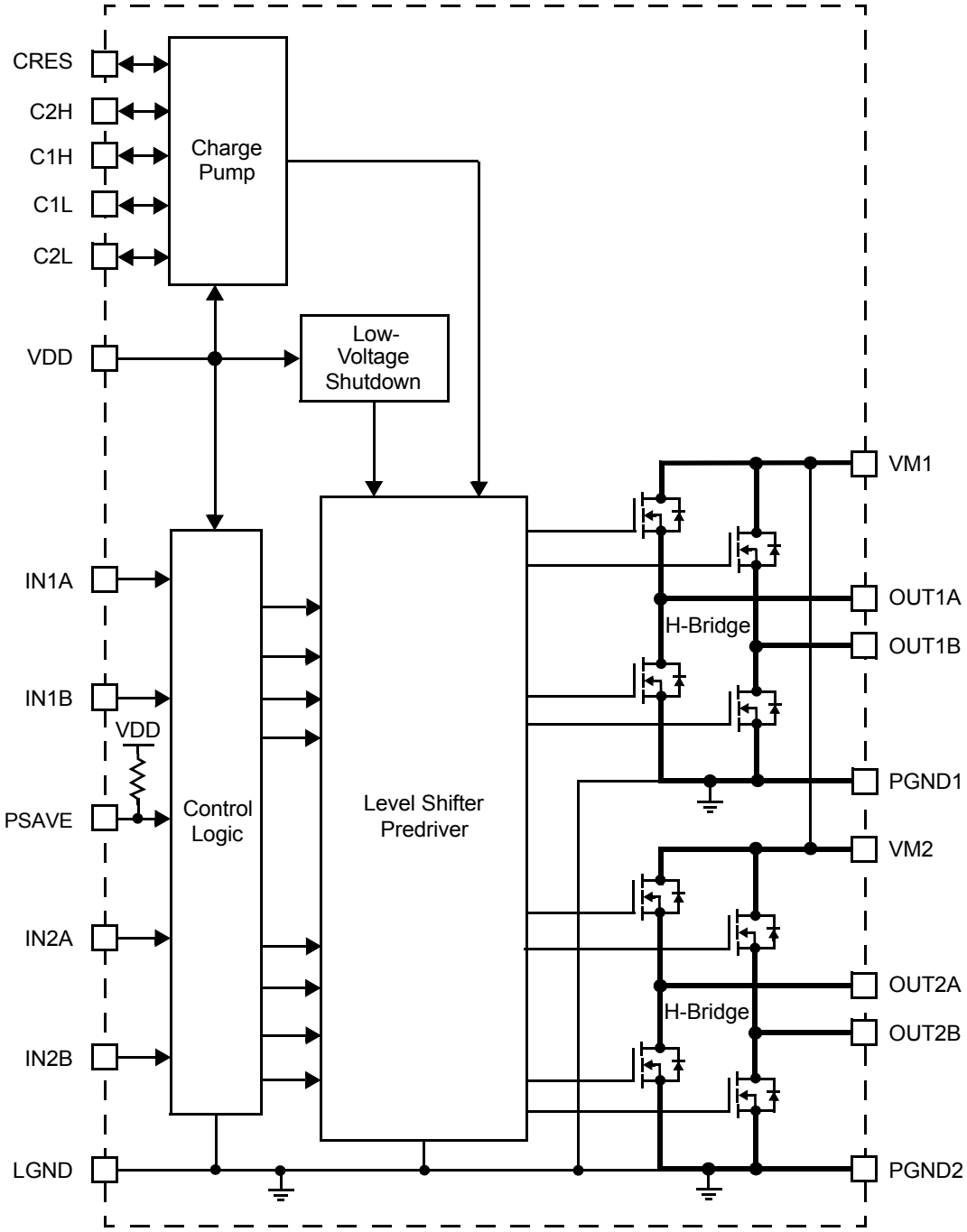



**Figure 2. 17531A Simplified Internal Block Diagram**

# TERMINAL CONNECTIONS

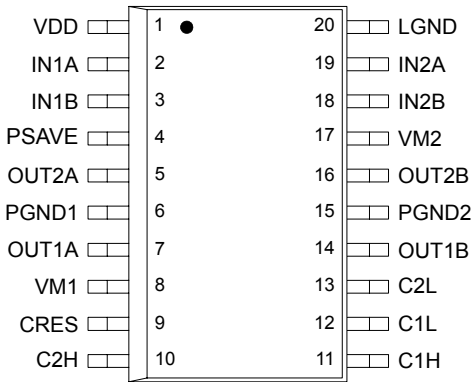



**Figure 3. 17531A, 20-Terminal VMFP Connections**

**Table 1. 17531A, 20-Terminal VMFP Definitions**

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 10.

| Terminal Number | Terminal Name | Formal Name | Definition |
|---|---|---|---|
| 1 | VDD | Logic Supply | Control circuit power supply terminal. |
| 2 | IN1A | Logic Input Control 1A | Logic input control of OUT1A (refer to Table 6. Truth Table, page 9). |
| 3 | IN1B | Logic Input Control 1B | Logic input control of OUT1B (refer to Table 6. Truth Table, page 9). |
| 4 | PSAVE | Power Save | Logic input controlling power save mode. |
| 5 | OUT2A | H-Bridge Output 2A | Output A of H-Bridge channel 2. |
| 6 | PGND1 | Power Ground 1 | High-current power ground 1. |
| 7 | OUT1A | H-Bridge Output 1A | Output A of H-Bridge channel 1. |
| 8 | VM1 | Motor Drive Power Supply 1 | Positive power source connection for H-Bridge 1 (Motor Drive Power Supply). |
| 9 | CRES | Predriver Power Supply | Internal triple charge pump output as predriver power supply. |
| 10 | C2H | Charge Pump 2H | Charge pump bucket capacitor 2 (positive pole). |
| 11 | C1H | Charge Pump 1H | Charge pump bucket capacitor 1 (positive pole). |
| 12 | C1L | Charge Pump 1L | Charge pump bucket capacitor 1 (negative pole). |
| 13 | C2L | Charge Pump 2L | Charge pump bucket capacitor 2 (negative pole). |
| 14 | OUT1B | H-Bridge Output 1B | Output B of H-Bridge channel 1. |
| 15 | PGND2 | Power Ground 2 | High-current power ground 2. |
| 16 | OUT2B | H-Bridge Output 2B | Output B of H-Bridge channel 2. |
| 17 | VM2 | Motor Drive Power Supply 2 | Positive power source connection for H-Bridge 2 (Motor Drive Power Supply). |
| 18 | IN2B | Logic Input Control 2B | Logic input control of OUT2B (refer to Table 6. Truth Table, page 9). |
| 19 | IN2A | Logic Input Control 2A | Logic input control of OUT2A (refer to Table 6. Truth Table, page 9). |
| 20 | LGND | Logic Ground | Low-current logic signal ground. |

**Transparent Top View of Package**

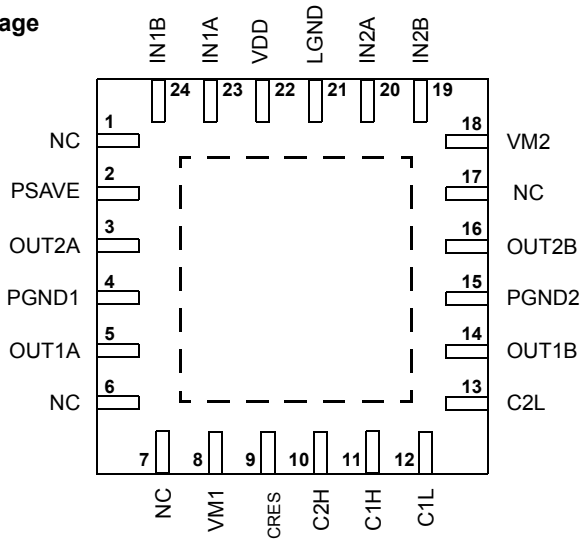



**Figure 4. 17531A, 24-Terminal QFN Connections**

**Table 2. 17531A, 24-Terminal QFN Definitions**

A functional description of each terminal can be found in the Functional Terminal Description section beginning on page 10.

| Terminal Number | Terminal Name | Formal Name | Definition |
|---|---|---|---|
| 1, 6, 7, 17 | NC | No Connect | This terminal is not used. |
| 2 | PSAVE | Power Save | Logic input controlling power save mode. |
| 3 | OUT2A | H-Bridge Output 2A | Output A of H-Bridge channel 2. |
| 4 | PGND1 | Power Ground 1 | High-current power ground 1. |
| 5 | OUT1A | H-Bridge Output 1A | Output A of H-Bridge channel 1. |
| 8 | VM1 | Motor Drive Power Supply 1 | Positive power source connection for H-Bridge 1 (Motor Drive Power Supply). |
| 9 | $C_{RES}$ | Predriver Power Supply | Internal triple charge pump output as pre-driver power supply. |
| 10 | C2H | Charge Pump 2H | Charge pump bucket capacitor 2 (positive pole). |
| 11 | C1H | Charge Pump 1H | Charge pump bucket capacitor 1 (positive pole). |
| 12 | C1L | Charge Pump 1L | Charge pump bucket capacitor 1 (negative pole). |
| 13 | C2L | Charge Pump 2L | Charge pump bucket capacitor 2 (negative pole). |
| 14 | OUT1B | H-Bridge Output 1B | Output B of H-Bridge channel 1. |
| 15 | PGND2 | Power Ground 2 | High-current power ground 2. |
| 16 | OUT2B | H-Bridge Output 2B | Output B of H-Bridge channel 2. |
| 18 | VM2 | Motor Drive Power Supply 2 | Positive power source connection for H-Bridge 2 (Motor Drive Power Supply). |
| 19 | IN2B | Logic Input Control 2B | Logic input control of OUT2B (refer to Table 6, Truth Table, page 9). |
| 20 | IN2A | Logic Input Control 2A | Logic input control of OUT2A (refer to Table 6, Truth Table, page 9). |
| 21 | LGND | Logic Ground | Low-current logic signal ground. |
| 22 | $V_{DD}$ | Logic Supply | Control circuit power supply terminal. |
| 23 | IN1A | Logic Input Control 1A | Logic input control of OUT1A (refer to Table 6, Truth Table, page 9). |
| 24 | IN1B | Logic Input Control 1B | Logic input control of OUT1B (refer to Table 6, Truth Table, page 9). |

# MAXIMUM RATINGS

**Table 3. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

| Ratings | Symbol | Value | Unit |
|---|---|---|---|
| Motor Supply Voltage | $V_M$ | -0.5 to 11.0 | V |
| Charge Pump Output Voltage | $V_{CRES}$ | -0.5 to 14.0 | V |
| Logic Supply Voltage | $V_{DD}$ | -0.5 to 5.0 | V |
| Signal Input Voltage | $V_{IN}$ | -0.5 to $V_{DD}$+0.5 | V |
| Driver Output Current | | | A |
| Continuous | $I_O$ | 0.7 | |
| Peak (1) | $I_{OPK}$ | 1.4 | |
| ESD Voltage | | | V |
| Human Body Model (2) | $V_{ESD1}$ | ±1200 | |
| Machine Model (3) | $V_{ESD2}$ | ±150 | |
| Operating Junction Temperature | $T_J$ | -20 to 150 | °C |
| Operating Ambient Temperature | $T_A$ | -20 to 65 | °C |
| Storage Temperature Range | $T_{STG}$ | -65 to 150 | °C |
| Thermal Resistance (4) | $R_{\theta JA}$ | 50 | °C/W |
| Power Dissipation (5) | $P_D$ | | W |
| WMFP | | 1.0 | |
| QFN | | 2.5 | |
| Terminal Soldering Temperature (6) | $T_{SOLDER}$ | 260 | °C |

Notes

1. $T_A$ = 25°C. Pulse width = 10 ms at 200 ms intervals.
2. ESD1 testing is performed in accordance with the Human Body Model ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω).
3. ESD2 testing is performed in accordance with the Machine Model ($C_{ZAP}$ = 200 pF, $R_{ZAP}$ = 0 Ω).
4. For QFN only, mounted on 37 x 50 Cu area (1.6 mm FR-4 PCB).
5. $T_A$ = 25°C.
6. Terminal soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

# STATIC ELECTRICAL CHARACTERISTICS

**Table 4. Static Electrical Characteristics**

Characteristics noted under conditions $T_A$ = 25°C, $V_{DD}$ = 3.0 V, $V_M$ = 5.0 V, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25°C under nominal conditions unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **POWER INPUT** | | | | | |
| Motor Supply Voltage (Using Internal Charge Pump) (7) | $V_{M\text{-}CP}$ | 2.0 | 5.0 | 8.6 | V |
| Motor Supply Voltage ($V_{CRES}$ Applied Externally) (8) | $V_{M\text{-}NCP}$ | – | – | 10 | V |
| Gate Drive Voltage - Motor Supply Voltage ($V_{CRES}$ Applied Externally) (9) | $V_{CRES-VM}$ | 5.0 | 6.0 | – | V |
| Logic Supply Voltage | $V_{DD}$ | 2.7 | 3.0 | 3.6 | V |
| Driver Quiescent Supply Current | | | | | µA |
| No Signal Input | $I_{QM}$ | – | – | 100 | |
| Power Save Mode | $I_{QM\text{-}PSAVE}$ | – | – | 1.0 | |
| Logic Quiescent Supply Current | | | | | mA |
| No Signal Input (10) | $I_{QVDD}$ | – | – | 1.0 | |
| Power Save Mode | $I_{QVDD\text{-}PSAVE}$ | – | – | 1.0 | |
| Operating Power Supply Current | | | | | mA |
| Logic Supply Current (11) | $I_{VDD}$ | – | – | 3.0 | |
| Charge Pump Circuit Supply Current (12) | $I_{CRES}$ | – | – | 0.7 | |
| Low $V_{DD}$ Detection Voltage (13) | $V_{DDDET}$ | 1.0 | 1.6 | 2.5 | V |
| Driver Output ON Resistance (14) | $R_{DS(ON)}$ | – | 0.8 | 1.2 | Ohms |
| **GATE DRIVE** | | | | | |
| Gate Drive Voltage (12) | $V_{CRES}$ | | | | V |
| No Current Load | | 12 | 13 | 13.5 | |
| Gate Drive Ability (Internally Supplied) | $V_{CRESload}$ | | | | V |
| $I_{C_{RES}}$ = -1.0 mA | | 8.5 | 9.2 | – | |
| Recommended External Capacitance (C1L–C1H, C2L–C2H, $C_{RES}$–GND) | $C_{CP}$ | 0.01 | 0.1 | 1.0 | µF |

Notes

7. Gate drive voltage $V_{C_{RES}}$ is generated internally. 2 x $V_{DD}$ + $V_M$ must be < $V_{C_{RES}}$ max (13.5 V).
8. No internal charge pump used. $V_{C_{RES}}$ is applied from an external source.
9. $R_{DS(ON)}$ is not guaranteed if $V_{C_{RES}} - V_M$ < 5.0 V. Also, function is not guaranteed if $V_{C_{RES}} - V_M$ < 3.0 V.
10. $I_{Q_{VDD}}$ includes the current to pre-driver circuit.
11. $I_{V_{DD}}$ includes the current to predriver circuit at $f_{IN}$ = 100 kHz.
12. At $f_{IN}$ = 20 kHz.
13. Detection voltage is defined as when the output becomes high-impedance after $V_{DD}$ drops below the detection threshold. $V_{C_{RES}}$ is applied from an external source. 2 x $V_{DD}$ + $V_M$ must be < $V_{C_{RES}}$ max (13.5 V).
14. $I_O$ = 0.7 A source + sink.

**Table 4. Static Electrical Characteristics (continued)**

Characteristics noted under conditions $T_A$ = 25°C, $V_{DD}$ = 3.0 V, $V_M$ = 5.0 V, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25°C under nominal conditions unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CONTROL LOGIC | | | | | |
| Logic Input Voltage | $V_{IN}$ | 0 | – | $V_{DD}$ | V |
| Logic Inputs (2.7 V < $V_{DD}$ < 3.3 V) | | | | | |
| High-Level Input Voltage | $V_{IH}$ | $V_{DD}$ x 0.7 | – | – | V |
| Low-Level Input Voltage | $V_{IL}$ | – | – | $V_{DD}$ x 0.3 | V |
| High-Level Input Current | $I_{IH}$ | – | – | 1.0 | µA |
| Low-Level Input Current | $I_{IL}$ | -1.0 | – | – | µA |
| PSAVE Terminal Input Current Low | $I_{IL}$-PSAVE | – | 50 | 100 | µA |

# DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 5. Dynamic Electrical Characteristics**

Characteristics noted under conditions $T_A$ = 25°C, $V_{DD}$ = 3.0 V, $V_M$ = 5.0 V, GND = 0 V unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25°C under nominal conditions unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **INPUT** | | | | | |
| Pulse Input Frequency | $f_{IN}$ | – | – | 200 | kHz |
| Input Pulse Rise Time (15) | $t_R$ | – | – | 1.0 (16) | µs |
| Input Pulse Fall Time (17) | $t_F$ | – | – | 1.0 (16) | µs |
| **OUTPUT** | | | | | |
| Propagation Delay Time (18) | | | | | µs |
| Turn-ON Time | $t_{PLH}$ | – | 0.1 | 0.5 | |
| Turn-OFF Time | $t_{PHL}$ | – | 0.1 | 0.5 | |
| Charge Pump Wake-Up Time (19) | $t_{VGON}$ | – | 1.0 | 3.0 | ms |
| Low-Voltage Detection Time | $t_{VDDDET}$ | – | – | 10 | ms |

Notes

15. Time is defined between 10% and 90%.
16. That is, the input waveform slope must be steeper than this.
17. Time is defined between 90% and 10%.
18. Output load is 8.0 Ω DC.
19. $C_{CP}$ = 0.1 µF.

# TIMING DIAGRAMS

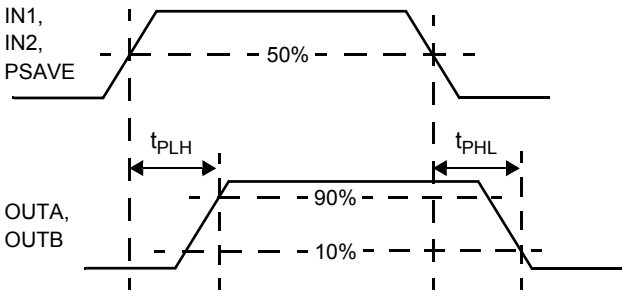



**Figure 5. $t_{PLH}$, $t_{PHL}$, and $t_{PZH}$ Timing**

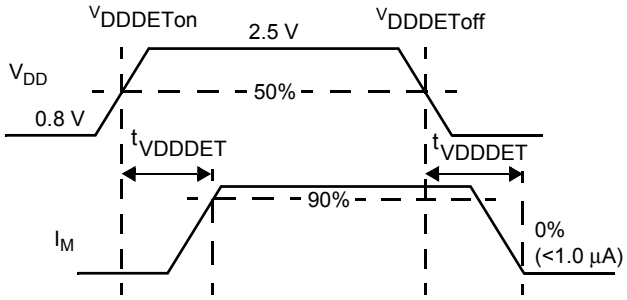



**Figure 6. Low-Voltage Detection Timing**

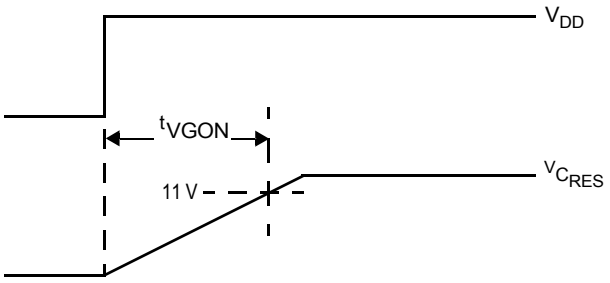



**Figure 7. Charge Pump Timing**

**Table 6. Truth Table**

| INPUT | | | OUTPUT | | Charge Pump and Low Voltage Detector |
|---|---|---|---|---|---|
| PSAVE | IN1A<br>IN2A | IN1B<br>IN2B | OUT1A<br>OUT2A | OUT1B<br>OUT2B | |
| L | L | L | L | L | RUN |
| L | H | L | H | L | RUN |
| L | L | H | L | H | RUN |
| L | H | H | Z | Z | RUN |
| H | X | X | Z | Z | STOP |

H = High.
L = Low.
Z = High impedance.
X = Don't care.
PSAVE terminal is pulled up to $V_{DD}$ with internal resistance.

# FUNCTIONAL DESCRIPTION

## INTRODUCTION

The 17531A is a monolithic dual H-Bridge ideal for portable electronic applications to control bipolar step motors and brush DC motors such as those found in camera len assemblies, camera shutters, and optical disk drives. The device features an on-board charge pump, as well as built-in shoot-through current protection and undervoltage shutdown.

The 17531A has four operating modes: Forward, Reverse, Brake, and Tri-Stated (High Impedance). The MOSFETs comprising the output bridge have a total source + sink $R_{DS(ON)} \leq 1.2\ \Omega$.

The 17531A can simultaneously drive two brush DC motors or one bipolar step motor. The drivers are designed to be PWM'ed at frequencies up to 200 kHz.

## FUNCTIONAL TERMINAL DESCRIPTION

### LOGIC SUPPLY (VDD)

The $V_{DD}$ terminal carries the logic supply voltage and current into the logic sections of the IC. VDD has an undervoltage threshold. If the supply voltage drops below the undervoltage threshold, the output power stage switches to a tri-state condition. When the supply voltage returns to a level that is above the threshold, the power stage automatically resumes normal operation according to the established condition of the input terminals.

### LOGIC INPUT CONTROL (IN1A, IN1B, IN2A, AND IN2B)

These logic input terminals control each H-Bridge output. IN1A logic HIGH = OUT1A HIGH. However, if all inputs are taken HIGH, the outputs bridges are both tri-stated (refer to Table 6, Truth Table, page 9).

### POWER SAVE (PSAVE)

The PSAVE terminal is a HIGH = TRUE power save mode input. When PSAVE = HIGH, all H-Bridge outputs (OUT1A, OUT1B, OUT2A, and OUT2B) are tri-stated (High-Z), regardless of logic inputs (IN1A, IN1B, IN2A, and IN2B) states, and the internal charge pump and low voltage detection current are shut off to save power.

### H-BRIDGE OUTPUT (OUT1A, OUT1B, OUT2A, AND OUT2B)

These terminals provide connection to the outputs of each of the internal H-Bridges (see Figure 2, 17531A Simplified Internal Block Diagram, page 2).

### MOTOR DRIVE POWER SUPPLY (VM1 AND VM2)

The VM terminals carry the main supply voltage and current into the power sections of the IC. This supply then becomes controlled and/or modulated by the IC as it delivers the power to the loads attached between the OUTput terminals. All VM terminals must be connected together on the printed circuit board.

### CHARGE PUMP (C1L AND C1H, C2L AND C2H)

These two pairs of terminals, the C1L and C1H and the C2L and C2H, connect to the external bucket capacitors required by the internal charge pump. The typical value for the bucket capacitors is 0.1 μF.

### PREDRIVER POWER SUPPLY (CRES)

The CRES terminal is the output of the internal charge pump. Its output voltage is approximately three times of VDD voltage. The VCRES voltage is power supply for the internal predriver circuit of H-Bridges.

### POWER GROUND (PGND)

Power ground terminals. They must be tied together on the PCB.

### LOGIC GROUND (LGND)

Logic ground terminal.

# TYPICAL APPLICATIONS

Figure 8 shows a typical application for the 17531A. When applying the gate voltage to the CRES terminal from an external source, be sure to connect it via a resistor equal to, or greater than, $R_G = {}^{V}C_{RES}/0.02\ \Omega$.

The internal charge pump of this device is generated from the VDD supply; therefore, care must be taken to provide sufficient gate-source voltage for the high-side MOSFETs when $V_M >> V_{DD}$ (e.g., $V_M$ = 5.0 V, $V_{DD}$ = 3.3 V), in order to ensure full enhancement of the high-side MOSFET channels.

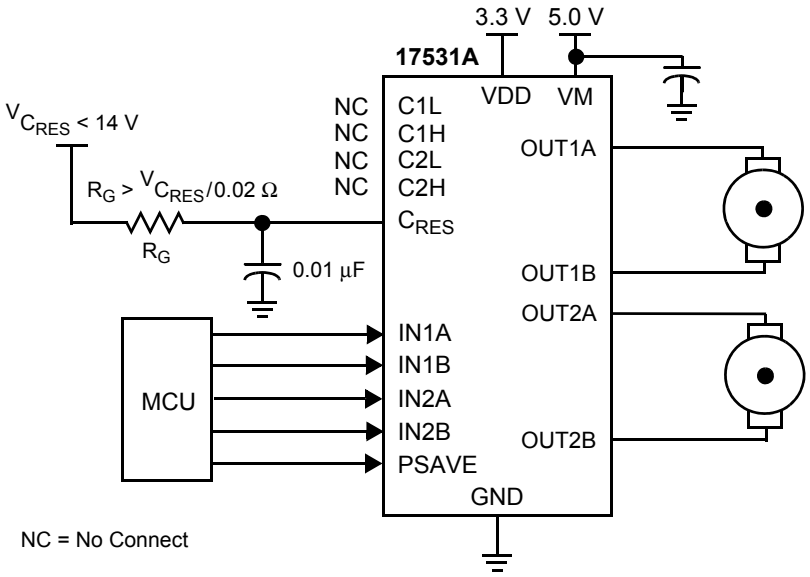



**Figure 8. 17531A Typical Application Diagram**

## CEMF SNUBBING TECHNIQUES

Care must be taken to protect the IC from potentially damaging CEMF spikes induced when commutating currents in inductive loads. Typical practice is to provide snubbing of voltage transients via placing a capacitor or zener at the supply terminal (VM) (see Figure 9).

## PCB LAYOUT

When designing the printed circuit board (PCB), connect sufficient capacitance between power supply and ground terminals to ensure proper filtering from transients. For all high-current paths, use wide copper traces and shortest possible distances.

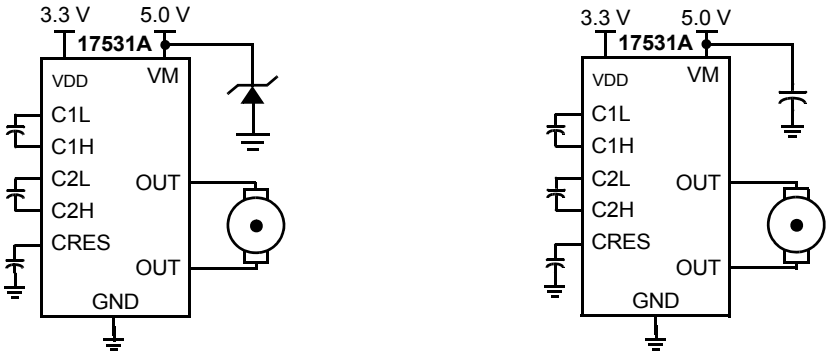


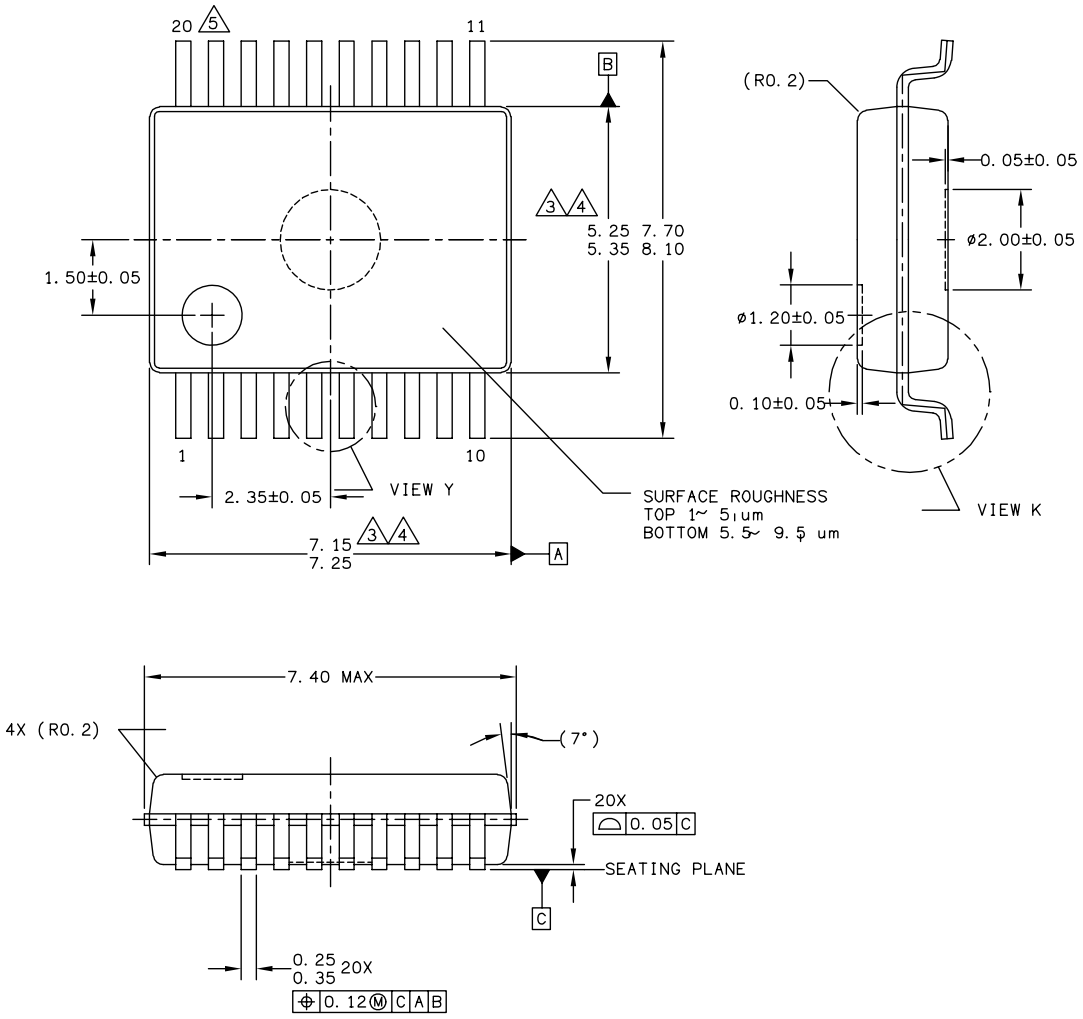

**Figure 9. CEMF Snubbing Techniques**

# PACKAGING

## *PACKAGE DIMENSIONS*

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the “98A” drawing number listed below.

**EV (Pb-FREE) SUFFIX**
20-LEAD VMFP
PLASTIC PACKAGE
98ASA10816D
ISSUE A

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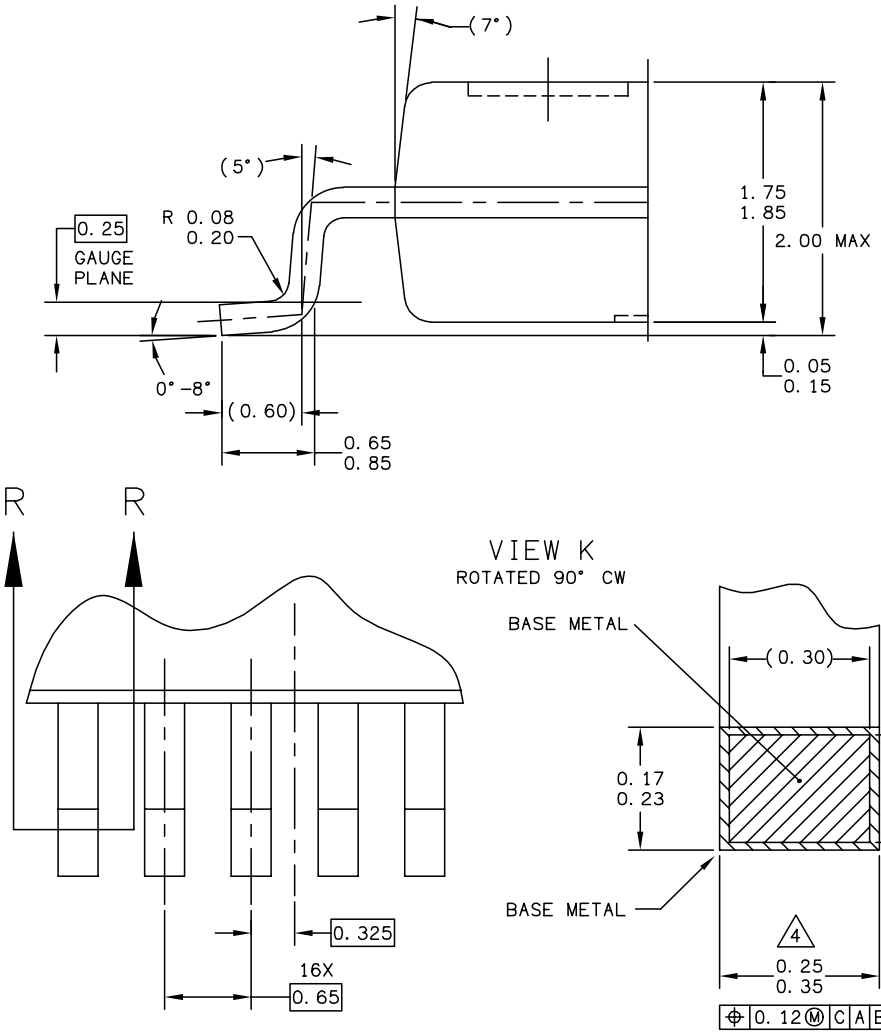
| TITLE: EIAJ VMFP 20LD, 0. 65 PITCH | DOCUMENT NO: 98ASA10616D | | REV: A |
| | CASE NUMBER: 1569-01 | | 20 JUN 2005 |
| | STANDARD: NON-JEDEC | | |

**17531A**

**EV (Pb-FREE) SUFFIX**
20-LEAD VMFP
PLASTIC PACKAGE
98ASA10816D
ISSUE A

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| | CASE NUMBER: 1569-01 | 20 JUN 2005 |
| | STANDARD: NON-JEDEC | |

**17531A**

**EV (Pb-FREE) SUFFIX**
20-LEAD VMFP
PLASTIC PACKAGE
98ASA10816D
ISSUE A

NOTES:

1 DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.

2 ALL DIMENSIONS ARE IN MILLIMETERS.

3 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.10 ANY SIDE. DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 PER SIDE.

4 DIMENSIONS ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS, AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

5 TERMINAL NUMBER ARE SHOWN FOR REFERENCE ONLY.

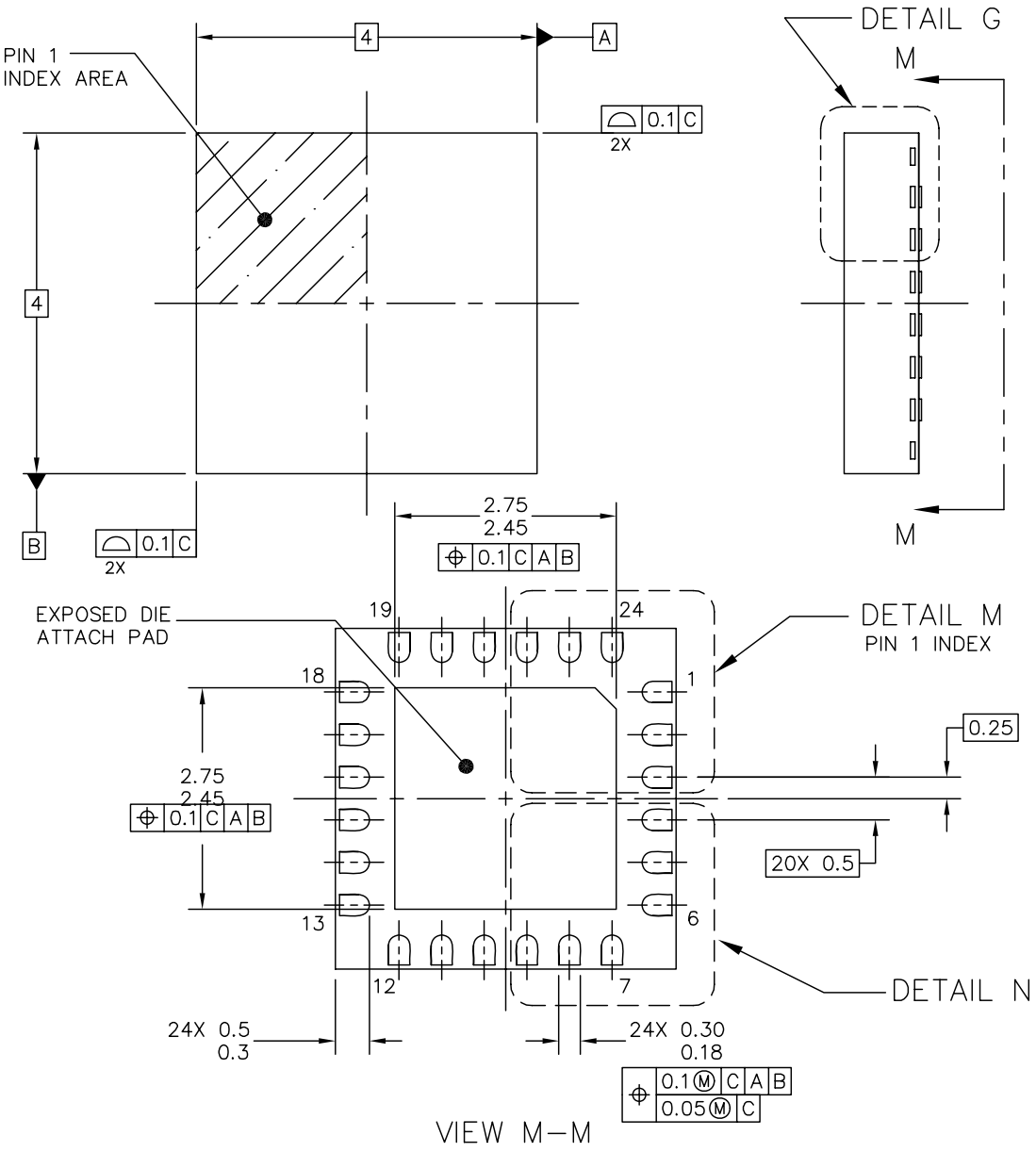


| MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
|---|---|

| TITLE: | DOCUMENT NO: 98ASA10616D | REV: A |
|---|---|---|
| EIAJ VMFP 20LD, 0.65 PITCH | CASE NUMBER: 1569-01 | 20 JUN 2005 |
| | STANDARD: NON-JEDEC | |

**17531A**

**EP (Pb-FREE) SUFFIX**
24-LEAD QFN
PLASTIC PACKAGE
98ARL10577D
ISSUE A

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| TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 24 TERMINAL, 0.5 PITCH (4 X 4 X 1) | DOCUMENT NO: 98ARL10577D | REV: A |
| | CASE NUMBER: 1508–01 | 03 AUG 2005 |
| | STANDARD: NON–JEDEC | |

**17531A**

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24-LEAD QFN
PLASTIC PACKAGE
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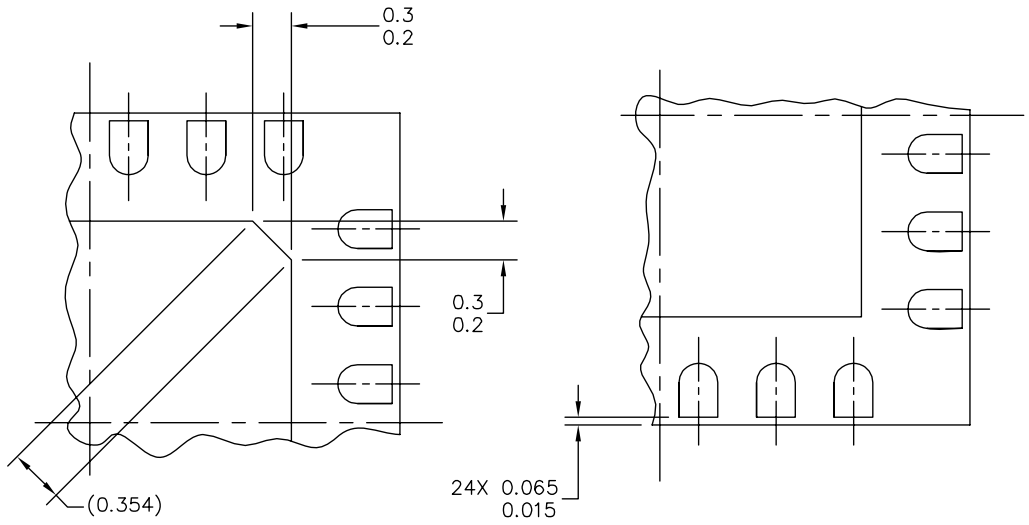


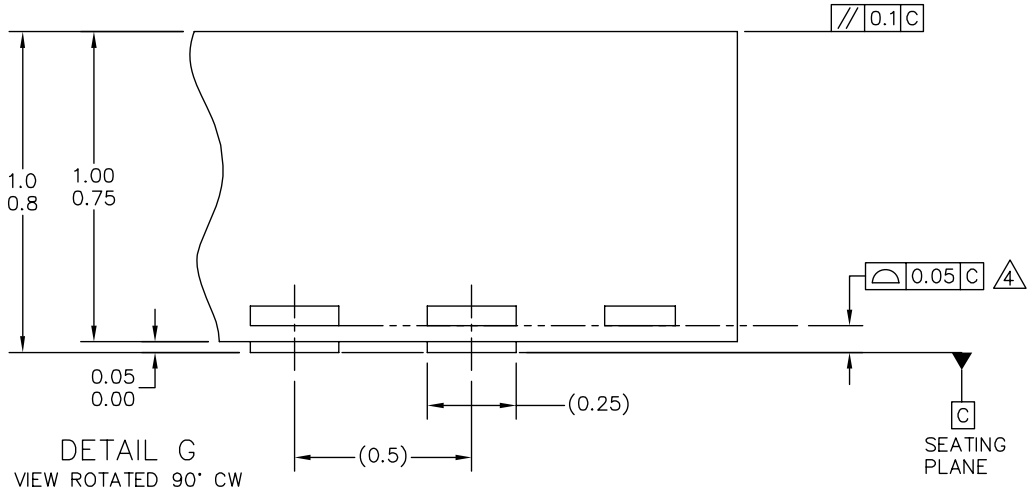


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| | CASE NUMBER: 1508–01 | 03 AUG 2005 |
| | STANDARD: NON–JEDEC | |

**17531A**

**EP (Pb-FREE) SUFFIX**
24-LEAD QFN
PLASTIC PACKAGE
CASE 1508-01
ISSUE A

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFP–N.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH PAD.

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|---|---|---|
|  | **MECHANICAL OUTLINE** | PRINT VERSION NOT TO SCALE |
| TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 24 TERMINAL, 0.5 PITCH (4 X 4 X 1) | DOCUMENT NO: 98ARL10577D | REV: A |
| | CASE NUMBER: 1508–01 | 03 AUG 2005 |
| | STANDARD: NON–JEDEC | |

**17531A**

# REVISION HISTORY

| REVISION | DATE | DESCRIPTION OF CHANGES |
|---|---|---|
| 2.0 | 9/2005 | • Implemented Revision History page<br>• Converted to Freescale format |
| 3.0 | 2/2008 | • Corrected Table 2, Pin Definitions on page 4. |
| 4.0 | 5/2009 | • Corrected Note 7, in Static Electrical Characteristics table. |

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