

September 1983 Revised May 2005

MM74HC273 Octal D-Type Flip-Flops with Clear

General Description

The MM74HC273 edge triggered flip-flops utilize advanced silicon-gate CMOS technology to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 8 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the LOW-to-HIGH transition of the CLOCK input. The CLEAR input when LOW, sets all outputs to a low state.

Each output can drive 10 low power Schottky TTL equivalent loads. The MM74HC273 is functionally as well as pin compatible to the 74LS273. All inputs are protected from damage due to static discharge by diodes to $V_{\mbox{\footnotesize CC}}$ and ground.

Features

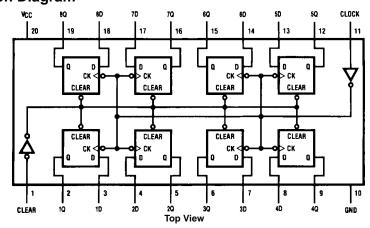
- Typical propagation delay: 18 ns
- Wide operating voltage range
- Low input current: 1 µA maximum
- Low quiescent current: 80 µA (74 Series)
- Output drive: 10 LS-TTL loads

Ordering Code:

Order Number	Package Number	Package Description
MM74HC273WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC273SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC273N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



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Truth Table

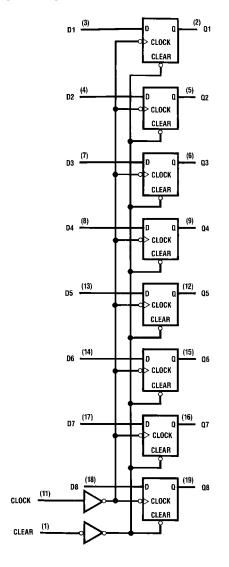
(Each Flip-Flop)

	Inputs		Outputs
Clear	Clock	D	Q
L	Х	Х	L
Н	↑	Н	Н
Н	↑	L	L
Н	L	Х	Q_0

- H = HIGH Level (Steady State)
 L = LOW Level (Steady State)
 X = Don't Care

 ↑ = Transition from LOW-to-HIGH level
 Q₀ = The level of Q before the indicated steady state input conditions were established

Logic Diagram



Absolute Maximum Ratings(Note 1) (Note 2)

DC V $_{CC}$ or GND Current, per pin (I $_{CC}$) ± 50 mA Storage Temperature Range (T $_{STG}$) -65° C to +150 $^{\circ}$ C

Power Dissipation (P_D)

 (Note 3)
 600 mW

 S.O. Package only
 500 mW

Lead Temperature (T_L)

(Soldering 10 seconds) 260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T _A)	-40	+85	°C
Input Rise or Fall Times			
$(t_r, t_f) V_{CC} = 2.0V$		1000	ns
V _{CC} = 4.5V		500	ns
V _{CC} = 6.0V		400	ns

 $\ensuremath{\text{Note 1:}}$ Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: – 12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{CC}	$T_A = 25^{\circ}C$		T _A = -40 to 85°C	T _A = -55 to 125°C	Units
			*cc	Тур		Guaranteed Limits		
V _{IH}	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V
	Input Voltage		4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V _{IL}	Maximum LOW Level		2.0V		0.5	0.5	0.5	V
	Input Voltage		4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V _{OH}	Minimum HIGH Level	$V_{IN} = V_{IH}$ or V_{IL}						
	Output Voltage	$ I_{OUT} \leq 20~\mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	5.7	5.48	5.34	5.2	V
V _{OL}	Maximum LOW Level	$V_{IN} = V_{IH}$ or V_{IL}						
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN} = V_{IH}$ or V_{IL}						
		$ I_{OUT} \le 4 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μА
	Current							
I _{CC}	Maximum Quiescent	V _{IN} = V _{CC} or GND	6.0V		8	80	160	μА
	Supply Current	I _{OUT} = 0 μA						

Note 4: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

 $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

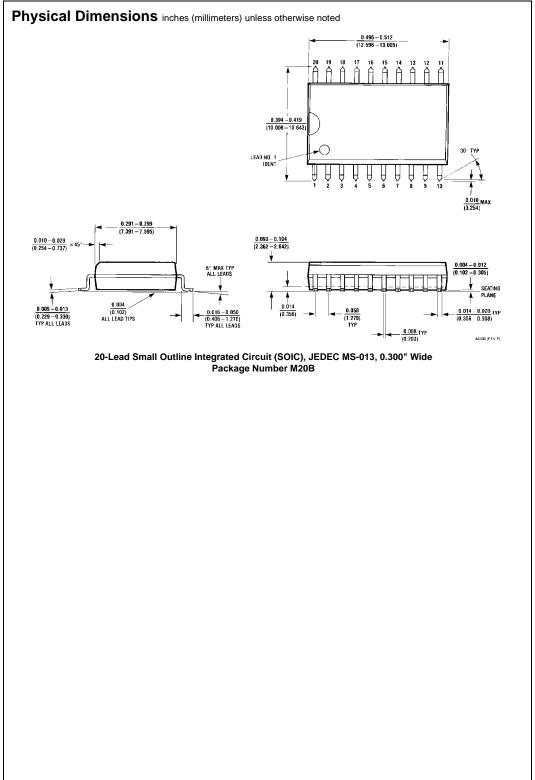
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
f _{MAX}	Maximum Operating Frequency		50	30	MHz
t _{PHL} , t _{PLH}	Maximum Propagation		18	27	ns
	Delay, Clock to Output				
t _{PHL}	Maximum Propagation		18	27	ns
	Delay, Clear to Output				
t _{REM}	Minimum Removal Time,		10	20	ns
	Clear to Clock				
t _s	Minimum Setup Time		10	20	ns
	Data to Clock				
t _H	Minimum Hold Time		-2	0	ns
	Clock to Data				
t _W	Minimum Pulse Width		10	16	ns
	Clock or Clear				

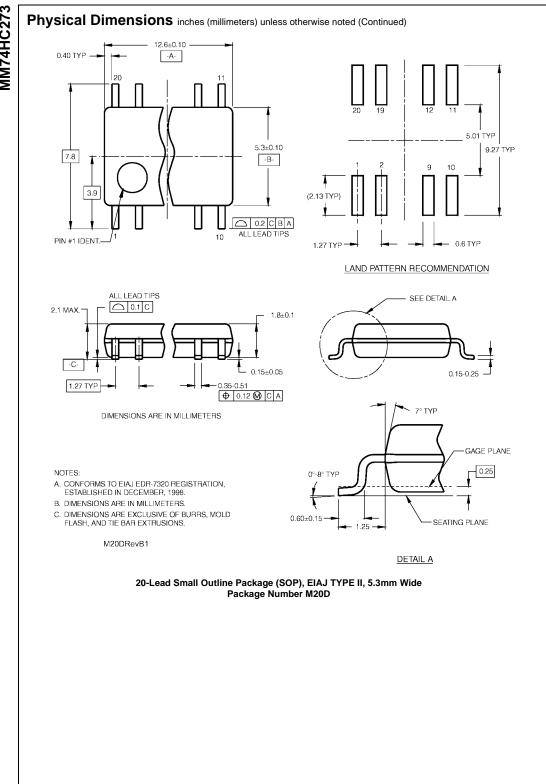
AC Electrical Characteristics

 $C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns} \text{ (unless otherwise specified)}$

Parameter	Conditions	v _{cc}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units
			Тур		Guaranteed Limits		
Maximum Operating		2.0V	16	5	4	3	MHz
Frequency		4.5V	74	27	21	18	MHz
		6.0V	78	31	24	20	MHz
Maximum Propagation		2.0V	38	135	170	205	ns
Delay, Clock to Output		4.5V	14	27	34	41	ns
		6.0V	12	23	29	35	ns
Maximum Propagation		2.0V	42	135	170	205	ns
Delay, Clear to Output		4.5V	19	27	34	41	ns
		6.0V	18	23	29	35	ns
Minimum Removal Time		2.0V	0	25	32	37	ns
Clear to Clock		4.5V	0	5	6	7	ns
		6.0V	0	4	5	6	ns
Minimum Setup Time		2.0V	26	100	125	150	ns
Data to Clock		4.5V	7	20	25	30	ns
		6.0V	5	17	21	25	ns
Minimum Hold Time		2.0V	-15	0	0	0	ns
Clock to Data		4.5V	-6	0	0	0	ns
		6.0V	-4	0	0	0	ns
Minimum Pulse Width		2.0V	34	80	100	120	ns
Clock or Clear		4.5V	11	16	20	24	ns
		6.0V	10	14	18	20	ns
Maximum Input Rise and		2.0V		1000	1000	1000	ns
Fall Time, Clock		4.5V		500	500	500	ns
		6.0V		400	400	400	ns
Maximum Output Rise		2.0V	28	75	95	110	ns
and Fall Time		4.5V	11	15	19	22	ns
		6.0V	9	13	16	19	ns
Power Dissipation	(per flip-flop)		45				pF
Capacitance (Note 5)							
Maximum Input			7	10	10	10	pF
Capacitance							
	Maximum Operating Frequency Maximum Propagation Delay, Clock to Output Maximum Propagation Delay, Clear to Output Minimum Removal Time Clear to Clock Minimum Setup Time Data to Clock Minimum Hold Time Clock to Data Minimum Pulse Width Clock or Clear Maximum Input Rise and Fall Time, Clock Maximum Output Rise and Fall Time Power Dissipation Capacitance (Note 5) Maximum Input	Maximum Operating Frequency Maximum Propagation Delay, Clock to Output Maximum Propagation Delay, Clear to Output Minimum Removal Time Clear to Clock Minimum Setup Time Data to Clock Minimum Hold Time Clock to Data Minimum Pulse Width Clock or Clear Maximum Input Rise and Fall Time, Clock Maximum Output Rise and Fall Time Power Dissipation Capacitance (Note 5) Maximum Input	Maximum Operating 2.0V Frequency 4.5V 6.0V Maximum Propagation 2.0V Delay, Clock to Output 4.5V 6.0V Maximum Propagation 2.0V Delay, Clear to Output 4.5V 6.0V Minimum Removal Time 2.0V Clear to Clock 4.5V Minimum Setup Time 2.0V Data to Clock 4.5V 6.0V Minimum Hold Time 2.0V Clock to Data 4.5V 6.0V Minimum Pulse Width 2.0V Clock or Clear 4.5V 6.0V Maximum Input Rise and 2.0V Fall Time, Clock 4.5V 6.0V Maximum Output Rise 2.0V and Fall Time 4.5V 6.0V Power Dissipation (per flip-flop) Capacitance (Note 5) Maximum Input	Parameter Conditions V _{CC} Typ Maximum Operating Frequency 2.0V 16 Frequency 4.5V 74 6.0V 78 Maximum Propagation Delay, Clock to Output 4.5V 14 6.0V 12 Maximum Propagation Delay, Clear to Output 4.5V 19 6.0V 18 Minimum Removal Time Clear to Clock 2.0V 0 Minimum Setup Time Data to Clock 2.0V 26 Minimum Hold Time Clock 4.5V 7 Minimum Pulse Width 2.0V -15 Clock to Data 4.5V -6 Minimum Pulse Width 2.0V 34 Clock or Clear 4.5V 11 Maximum Input Rise and Fall Time 2.0V 28 Ausimum Output Rise and Fall Time 2.0V 28 Power Dissipation Capacitance (Note 5) (per flip-flop) 45 Maximum Input 7	Parameter Conditions V _{CC} Typ Maximum Operating Frequency 2.0V 16 5 Frequency 4.5V 74 27 6.0V 78 31 Maximum Propagation Delay, Clock to Output 4.5V 14 27 6.0V 12 23 Maximum Propagation Delay, Clear to Output 2.0V 42 135 Delay, Clear to Output 4.5V 19 27 6.0V 18 23 Minimum Removal Time Clock 2.0V 0 25 Clear to Clock 4.5V 0 5 6.0V 0 4 4 Minimum Setup Time Data to Clock 2.0V 26 100 Data to Clock 4.5V 7 20 6.0V 5 17 Minimum Hold Time Clock 2.0V -15 0 Clock to Data 4.5V -6 0 Minimum Pulse Width Clock or Clear 4.5V 11 16 Clo	Maximum Operating 2.0V 16 5 4	Parameter Conditions Vcc Typ Guaranteed Limits

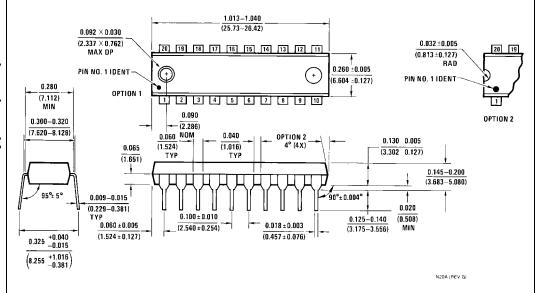
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} \ f + I_{CC}$.





Physical Dimensions inches (millimeters) unless otherwise noted (Continued) -0.20 64 4.4±0.1 -B-0.65 PIN #1 IDENT. LAND PATTERN RECOMMENDATION O.1 C ALL LEAD TIPS SEE DETAIL A -0.90^{+0.15} 0.09-0.20 0.65 0.19-0.30 | \$\dag{0.10\dag{A} R\$ 0\$ R0.09mir GAGE PLANE DIMENSIONS ARE IN MILLIMETERS NOTES: A. CONFORMS TO JEDEC REGISTRATION MD-153, VARIATION AC, REF NOTE 6, DATE 7/93. 0.6±0.1 R0.09min -1.00 B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND THE BAR EXTRUSIONS. DETAIL A D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. MTC20REVD1 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N20A

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