

March 2015

MM74HC02 Quad 2-Input NOR Gate

Features

- Typical Propagation Delay: 8 ns
- · Wide Power Supply Range: 2 V to 6 V
- Low Quiescent Supply Current: 20 μA Maximum (74HC Series)
- Moisture Level Sensitivity 1
- Low Input Current: 1 μA Maximum
- · High Output Current: 4 mA Minimum

General Description

The MM74HC02 NOR gates utilize advanced silicongate CMOS technology to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to $V_{\rm CC}$ and ground.

Ordering Information

Part Number	Top Mark	Package	Packing Method
MM74HC02M	MM74HC02M	SOIC 14L	Rail
MM74HC02MX	MM74HC02M	SOIC 14L	Tape and Reel
MM74HC02MTC	HC02	TSSOP 14L	Rail
MM74HC02MTCX	HC02	TSSOP 14L	Tape and Reel



All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

Pin Assignment for SOIC, TSSOP VCC Y4 B4 A4 Y3 B3 A3 14 13 12 11 10 9 8 1 1 2 3 4 5 6 7 Y1 A1 B1 Y2 A2 B2 GND Top View

Logic Diagram



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Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Unit	
V _{CC}	Supply Voltage	-0.5 to +7.0	V	
V _{IN}	DC Input Voltage		-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage	-0.5 to V _{CC} +0.5	V	
I _{IK} , I _{OK}	Clamp Diode Current	±20	mA	
I _{OUT}	DC Output Current, per pin	±25	mA	
I _{CC}	DC V _{CC} or GND Current, per pin	±50	mA	
T _{STG}	Storage Temperature Range	-65 to +150	°C	
D	Power Dissipation	(2)	600	mW
P_{D}	Tower Dissipation	S.O. Package only	500] '''۷
TL	Lead Temperature (Soldering 10 seconds)	260	°C	

Notes:

- 1. Unless otherwise specified all voltages are referenced to ground.
- 2. Power dissipation temperature derating plastic "N" package: -12 mW/°C from 65°C to 85°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit		
V _{CC}	Supply Voltage	2	6	V		
V _{IN} , V _{OUT}	DC Input or Output Voltage	0	V _{CC}	V		
T_A	Operating Temperature Range		-40	85	°C	
t _r , t _f	V _{CC}	c = 2.0 V		1000	ns	
	Input Rise or Fall Times	c = 4.5 V		500		
	V _{CC}		400			

DC Electrical Characteristics(3)

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C			T _A =-55 to 125°C	Unit
				Тур.	Gua	ranteed L	imits	
	Minimum HIGH Level	2.0			1.50	1.50	1.50	
V_{IH}		4.5			3.15	3.15	3.15	V
	Input Voltage	6.0			4.20	4.20	4.20	
		2.0			0.50	0.50	0.50	
V_{IL}	Maximum LOW Level	4.5			1.35	1.35	1.35	V
	Input Voltage	6.0			1.80	1.80	1.80	
		2.0	V _{IN} = V _{II} ,	2.0	1.9	1.9	1.9	
	Minimum HIGH Level Output Voltage	4.5	ν _{IN} – ν _{IL} , Ι _{ΟUT} ≤ 20 μΑ	4.5	4.4	4.4	4.4	
		6.0	I _{OUT} ≥ 20 μA	6.0	5.9	5.9	5.9	
V _{OH}		4.5	$V_{IN} = V_{IL},$ $ I_{OUT} \le 4.0 \text{ mA}$	4.20	3.98	3.84	3.70	V
		6.0	$V_{IN} = V_{IL},$ $ I_{OUT} \le 5.2 \text{ mA}$	5.70	5.48	5.34	5.20	
	Minimum LOW Level Output Voltage	2.0	\/ =\/ or\/	0	0.1	0.1	0.1	
1		4.5	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $ I_{OUT} \le 20 \mu\text{A}$	0	0.1	0.1	0.1	
		6.0	1001 = 20 μΑ	0	0.1	0.1	0.1	
V _{OL}		4.5	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $ I_{OUT} \le 4.0 \text{ mA}$	0.20	0.26	0.33	0.40	V
		6.0	$V_{IN} = V_{IH} \text{ or } V_{IL},$ $ I_{OUT} \le 5.2 \text{ mA}$	0.20	0.26	0.33	0.40	
I _{IN}	Maximum Input Current	6.0	$V_{IN} = V_{CC}$ or GND		±0.1	±0.1	±0.1	μА
I _{CC}	Maximum Quiescent Supply Current	6.0	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$		2.0	20	40	μА

Note:

3. For a power supply of 5 V $\pm 10\%$ the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

AC Electrical Characteristics

 $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}, C_L = 15 \text{ pF}, t_r = t_f = 6 \text{ ns}$

Symbol	Parameter	Conditions	Тур.	Guaranteed Limit	Unit
t_{PHL},t_{PLH}	Maximum Propagation Delay		8	15	ns

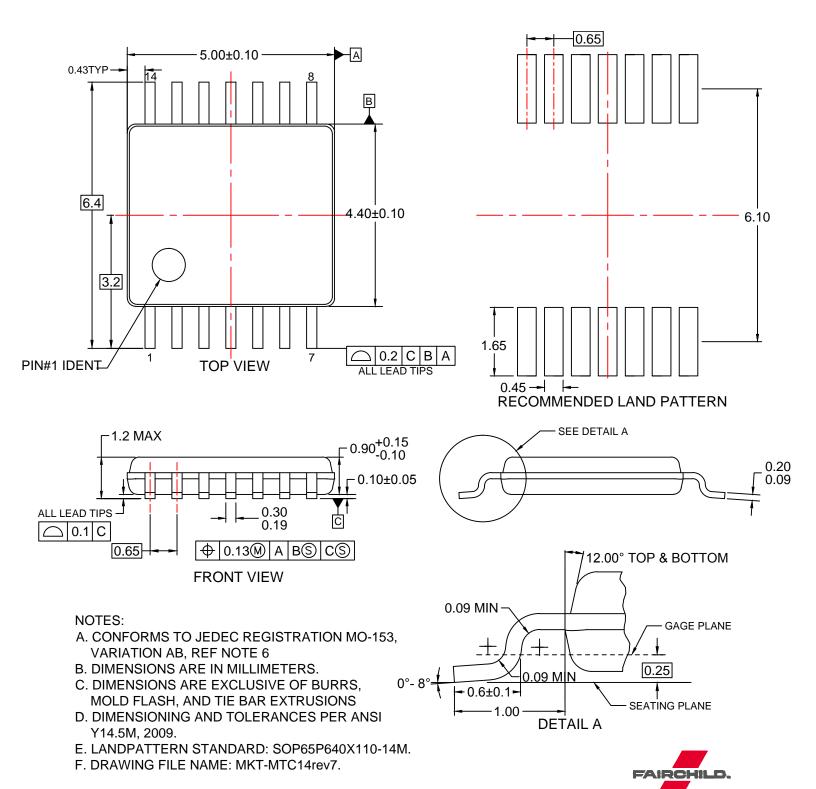
AC Electrical Characteristics

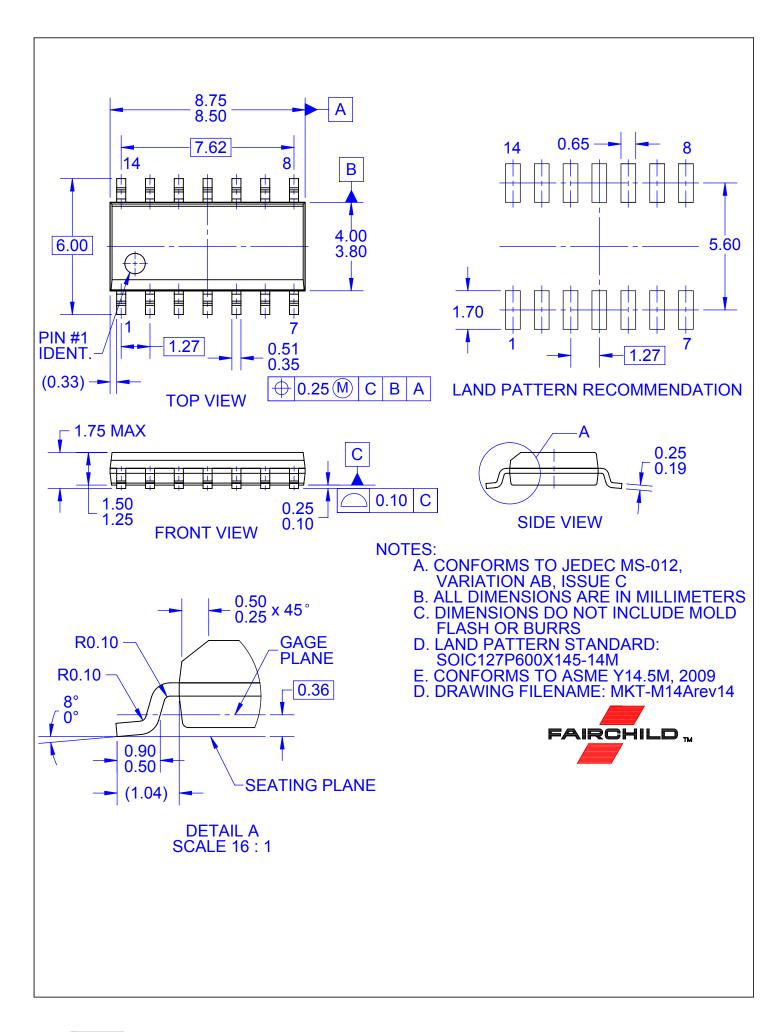
 V_{CC} = 2.0 V to 6.0 V, C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25°C		T _A =-40 to 85°C	T _A =-55 to 125°C	Unit
				Тур.	o. Guaranteed Limits			
	Maximum Propagation Delay	2.0		45	90	113	134	
t_{PHL}, t_{PLH}		4.5		9	18	23	27	ns
		6.0		8	15	19	23	
	Maximum Output Rise and Fall Time	2.0		30	75	95	110	
t _{TLH} , t _{THL}		4.5		8	15	19	22	ns
		6.0		7	13	16	19	
C _{PD}	Power Dissipation Capacitance ⁽⁴⁾		(per gate)	20				pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note:

4. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \, V_{CC}^{\ 2} \, f + I_{CC} \, V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \, V_{CC} \, f + I_{CC}$.





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