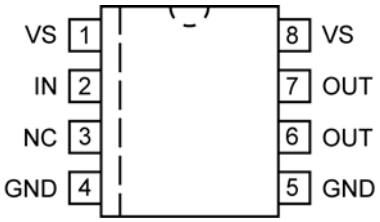
Ordering Information

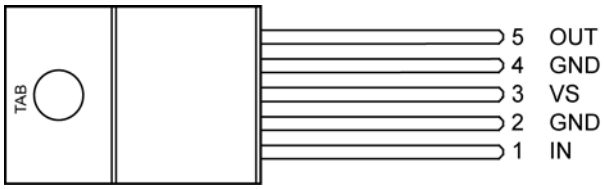
Part Number	Configuration	Temperature Range	Package
MIC4421AXM*	Inverting	–55° to +125°C	8-Pin SOIC
MIC4421AYM	Inverting	–40° to +85°C	8-Pin SOIC
MIC4421AZM	Inverting	0° to +70°C	8-Pin SOIC
MIC4421AYN	Inverting	–40° to +85°C	8-Pin PDIP
MIC4421AZN	Inverting	0° to +70°C	8-Pin PDIP
MIC4421AZT	Inverting	0° to +70°C	5-Pin TO-220
MIC4422AXM*	Non-Inverting	–55° to +125°C	8-Pin SOIC
MIC4422AYM	Non-Inverting	–40° to +85°C	8-Pin SOIC
MIC4422AZM	Non-Inverting	0° to +70°C	8-Pin SOIC
MIC4422AYN	Non-Inverting	–40° to +85°C	8-Pin PDIP
MIC4422AZN	Non-Inverting	0° to +70°C	8-Pin PDIP
MIC4422AZT	Non-Inverting	0° to +70°C	5-Pin TO-220

***** Special order. Contact factory.

Pin Configuration



8-Pin PDIP (N)
8-Pin SOIC (M)



5-Pin TO-220 (T)

Pin Description

Pin Number DIP, SOIC	Pin Number TO-220-5	Pin Name	Pin Name
2	1	IN	Control Input.
4, 5	2, 4	GND	Ground: Duplicate pins must be externally connected together.
1, 8	3, TAB	VS	Supply Input: Duplicate pins must be externally connected together.
6, 7	5	OUT	Output: Duplicate pins must be externally connected together.
3	—	NC	Not connected.

Absolute Maximum Ratings[1]

Supply Voltage (V_S) ..... +20V
Control Input Voltage (V_{IN}) ..... V_S + 0.3V to GND – 5V
Control Input Current (V_{IN} > V_S) 50mA
Power Dissipation, $T_A \leq +25°C$[4]
PDIP (θ_{JA}) 1478mW
SOIC (θ_{JA}) 767mW
TO-220 (θ_{JA}) 1756W
Lead Temperature (soldering, 10sec.) ..... 300°C
Storage Temperature (T_s) ..... –65°C to +150°C
ESD Rating[3] 2kV

Operating Ratings[2]

Supply Voltage (V_S) ..... +4.5V to +18V
Ambient Temperature (T_A)
X Version ..... –55°C to +125°C
Y Version ..... –40°C to +85°C
Z Version ..... 0°C to +70°C
Junction Temperature (T_J) ..... 150°C
Package Thermal Resistance[4]
PDIP (θ_{JA}) ..... 84.6°C/W
SOIC (θ_{JA}) ..... 163.0°C/W
TO-220 (θ_{JA}) ..... 71.2°C/W
PDIP (θ_{JC}) ..... 41.2°C/W
SOIC (θ_{JC}) ..... 38.8°C/W
TO-220 (θ_{JC}) ..... 6.5°C/W

Electrical Characteristics

T_A = 25°C with 4.5V ≤ V_S ≤ 18V, **bold** values indicate for X Version: –55°C≤ T_A ≤ +125°C, for Y Version: –40°C≤ T_A ≤ +85°C, and for Z Version: 0°C≤ T_A ≤ +70°C, unless noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
Power Supply						
V_S	Operating Input Voltage		**4.5**		**18**	V
I_S	High Output Quiescent Current	V_{IN} = 3V (MIC4422A), V_{IN} = 0 (MIC4421A)		0.5	1.5 **3**	mA mA
	Low Output Quiescent Current	V_{IN} = 0V (MIC4422A), V_{IN} = 3V (MIC4421A)		50	150 **200**	µA µA
Input						
V_{IH}	Logic 1 Input Voltage	See Figure 3	**3.0**	2.1		V
V_{IL}	Logic 0 Input Voltage	See Figure 3		1.5	**0.8**	V
V_{IN}	Input Voltage Range		**–5**		**V_S+0.3**	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	**–10**		**10**	µA
Output						
V_{OH}	High Output Voltage	See Figure 1	**V_S+.025**			V
V_{OL}	Low Output Voltage	See Figure 1			**0.025**	V
R_O	Output Resistance, Output High	I_{OUT} = 10mA, V_S = 18V		0.6	1.0 **3.6**	Ω Ω
	Output Resistance, Output Low	I_{OUT} = 10mA, V_S = 18V		0.8	1.7 **2.7**	Ω Ω
I_{PK}	Peak Output Current	V_S = 18V (See Figure 8)		9		A
I_{DC}	Continuous Output Current			2		A
I_R	Latch-Up Protection Withstand Reverse Current	Duty Cycle ≤ 2% t ≤ 300µs[5]	>1500			mA
Switching Time[5]						
t_R	Rise Time	Test Figure 1, C_L = 10,000pF		20	75 **120**	ns ns
t_F	Fall Time	Test Figure 1, C_L = 10,000pF		24	75 **120**	ns ns
t_{D1}	Delay Time	Test Figure 1		15	68 **80**	ns ns

Symbol	Parameter	Condition	Min	Typ	Max	Units
Switching Time[5] ***continued***						
t_{D2}	Delay Time	Test Figure 1		35	60 **80**	ns ns
t_{PW}	Minimum Input Pulse Width	See Figure 1 and Figure 2.		50		ns
f_{max}	Maximum Input Frequency	See Figure 1 and Figure 2.		1		MHz

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5kΩ in series with 100pF.
4. Minimum footprint.
5. Guaranteed by design.

Test Circuit

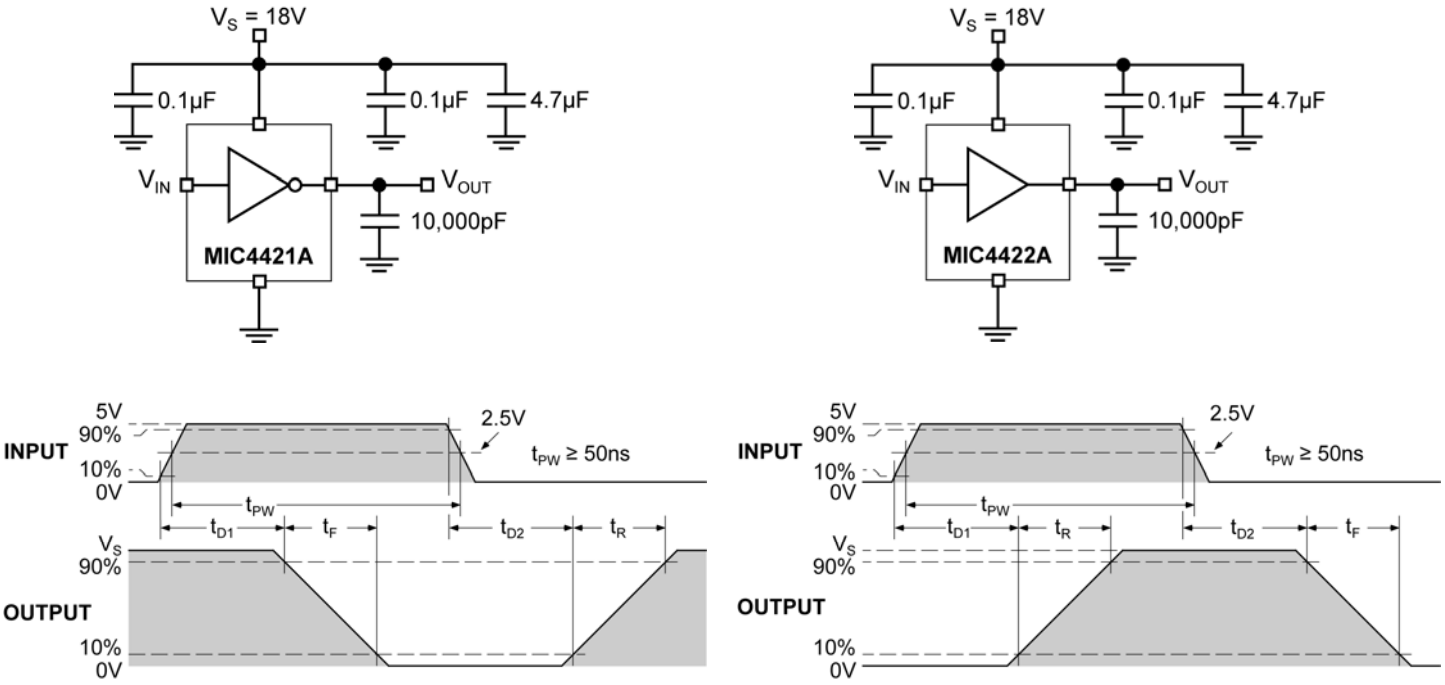


Figure 1. Inverting Driver Switching Time

Figure 2. Non-Inverting Driver Switching Time

Control Input Behavior

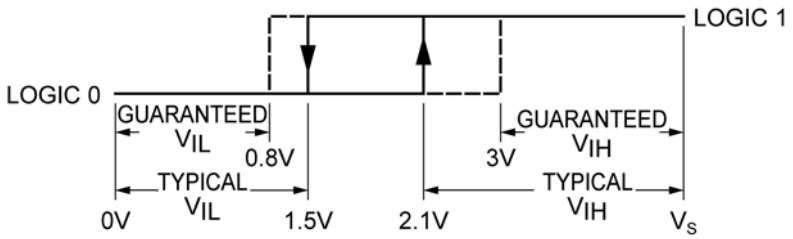
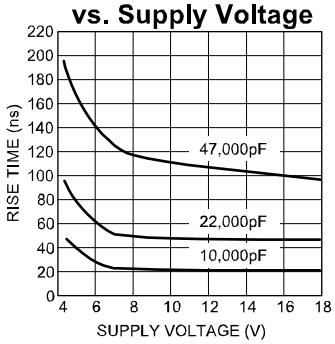


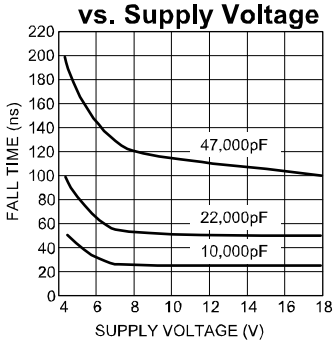
Figure 3. Input Hysteresis

Typical Characteristics

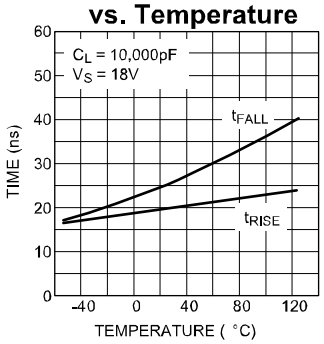
Rise Time vs. Supply Voltage



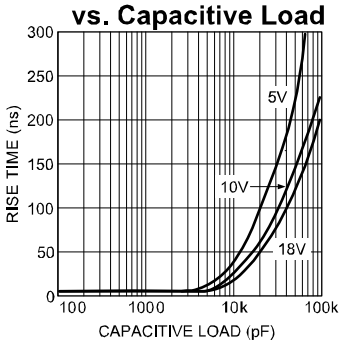
Fall Time vs. Supply Voltage



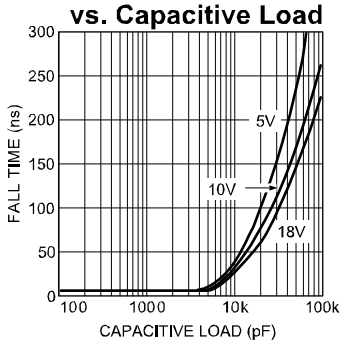
Rise and Fall Times vs. Temperature



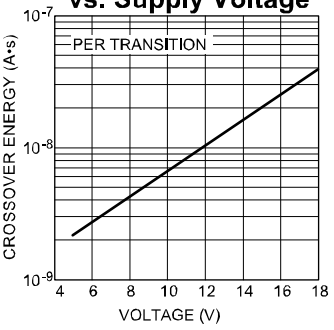
Rise Time vs. Capacitive Load



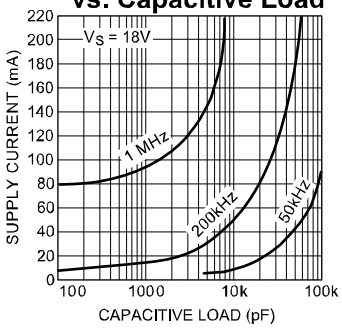
Fall Time vs. Capacitive Load



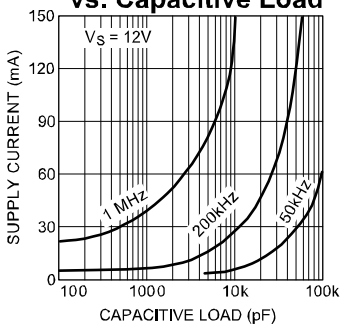
Crossover Energy vs. Supply Voltage



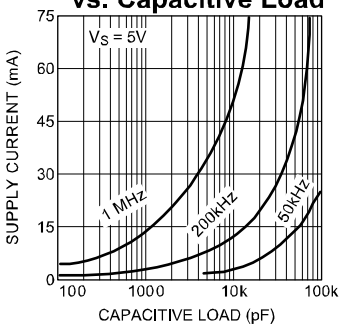
Supply Current vs. Capacitive Load



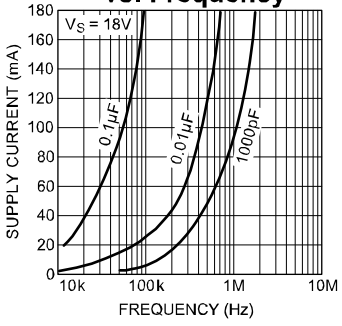
Supply Current vs. Capacitive Load



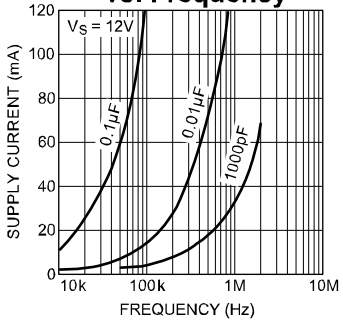
Supply Current vs. Capacitive Load



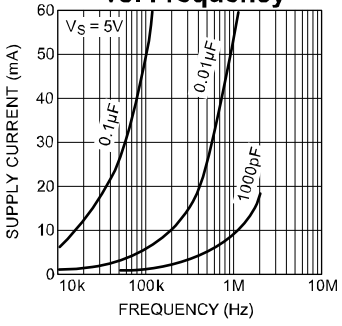
Supply Current vs. Frequency



Supply Current vs. Frequency

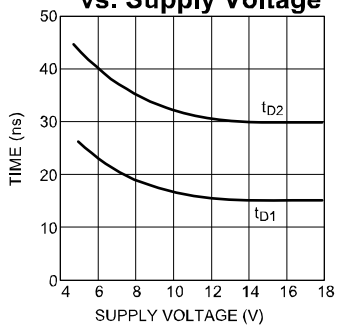


Supply Current vs. Frequency

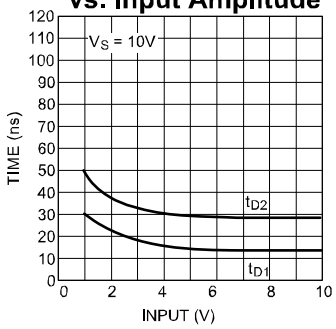


Typical Characteristics (continued)

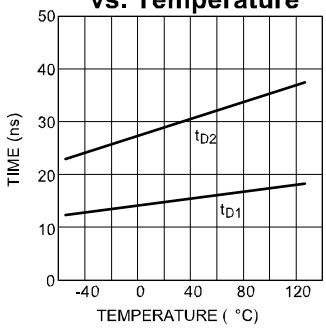
Propagation Delay vs. Supply Voltage



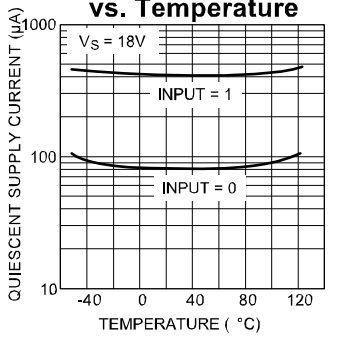
Propagation Delay vs. Input Amplitude



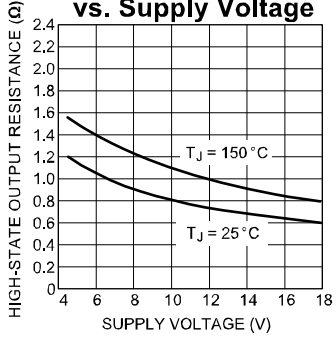
Propagation Delay vs. Temperature



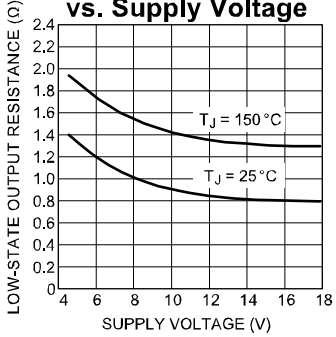
Quiescent Supply Current vs. Temperature



High-State Output Resist. vs. Supply Voltage



Low-State Output Resis vs. Supply Voltage



Functional Diagram

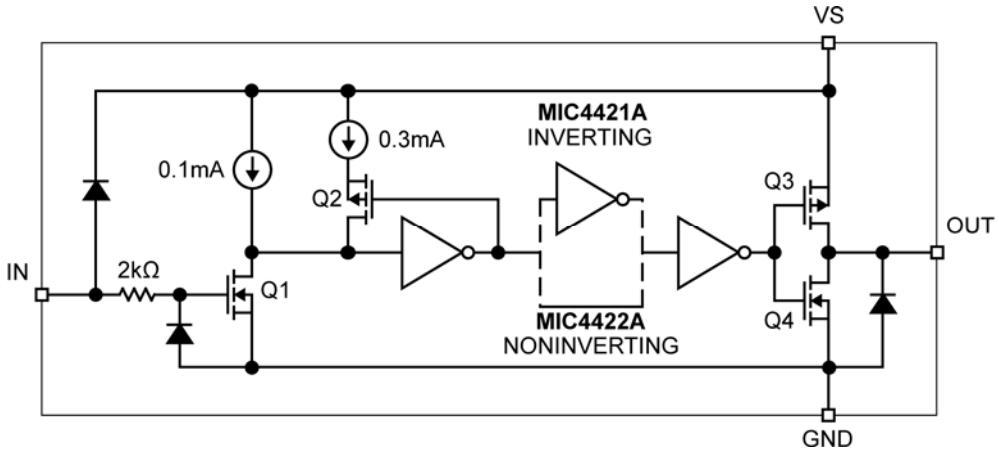


Figure 4. MIC4421A/22A Block Diagram

Functional Description

Refer to the functional diagram.

The MIC4422A is a non-inverting driver. A logic high on the IN produces gate drive output. The MIC4421A is an inverting driver. A logic low on the IN produces gate drive output. The output is used to turn on an external N-channel MOSFET.

Supply

V_S (supply) is rated for +4.5V to +18V. External capacitors are recommended to decouple noise.

Input

IN (control) is a TTL-compatible input. IN must be forced high or low by an external signal. A floating input will cause unpredictable operation.

A high input turns on Q1, which sinks the output of the 0.1mA and the 0.3mA current source, forcing the input of the first inverter low.

Hysteresis

The control threshold voltage, when IN is rising, is slightly higher than the control threshold voltage when CTL is falling.

When IN is low, Q2 is on, which applies the additional 0.3mA current source to Q1. Forcing IN high turns on Q1 which must sink 0.4mA from the two current sources. The higher current through Q1 causes a larger drain-to-source voltage drop across Q1. A slightly higher control voltage is required to pull the input of the first inverter down to its threshold.

Q2 turns off after the first inverter output goes high. This reduces the current through Q1 to 0.1mA. The lower current reduces the drain-to-source voltage drop across Q1. A slightly lower control voltage will pull the input of the first inverter up to its threshold.

Drivers

The second (optional) inverter permits the driver to be manufactured in inverting and non-inverting versions.

The last inverter functions as a driver for the output MOSFETs Q3 and Q4.

Output

OUT is designed to drive a capacitive load. V_{OUT} (output voltage) is either approximately the supply voltage or approximately ground, depending on the logic state applied to IN.

If IN is high, and V_S (supply) drops to zero, the output will be floating (unpredictable).

Application Information

Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 10,000pF load to 18V in 50ns requires 3.6A.

The MIC4421A/4422A has double bonding on the supply pins, the ground pins and output pins. This reduces parasitic lead inductance. Low inductance enables large currents to be switched rapidly. It also reduces internal ringing that can cause voltage breakdown when the driver is operated at or near the maximum rated voltage.

Internal ringing can also cause output oscillation due to feedback. This feedback is added to the input signal since it is referenced to the same ground.

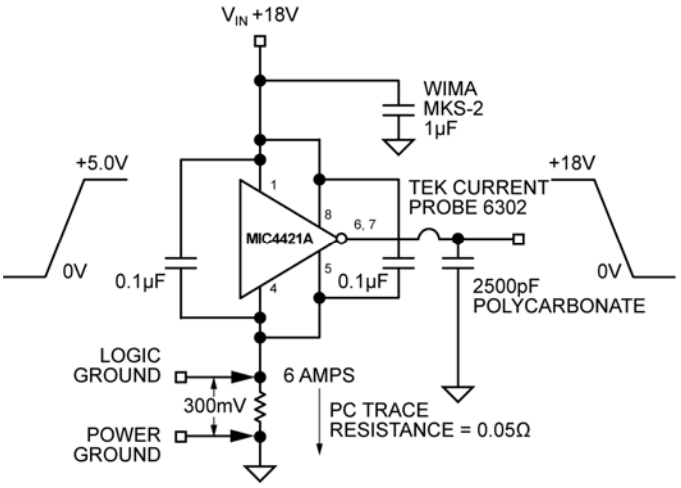


Figure 5. Switching Time Due to Negative Feedback

Table 1. MIC4421A Maximum Operating Frequency

V_S	Max Frequency
18V	220kHz
15V	300kHz
10V	640kHz
5V	2MHz

Conditions:

1. θ_{JA} = 150°C/W
2. T_A = 25°C
3. C_L = 10,000pF

To guarantee low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low inductance ceramic disk capacitor with short lead lengths (< 0.5 inch) should be used. A 1µF low ESR film capacitor in parallel with two 0.1µF low ESR ceramic capacitors, (such as AVX RAM Guard®), provides adequate bypassing. Connect one ceramic capacitor directly between pins 1 and 4. Connect the second ceramic capacitor directly between pins 8 and 5.

Grounding

The high current capability of the MIC4421A/4422A demands careful PC board layout for best performance. Since the MIC4421A is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. Feedback is especially noticeable with slow-rise time inputs. The MIC4421A input structure includes about 600mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 5 shows the feedback effect in detail. As the MIC4421A input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the MIC4421A ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillation may result.

To insure optimum performance, separate ground traces should be provided for the logic and power connections. Connecting the logic ground directly to the MIC4421A GND pins will ensure full logic drive to the input and ensure fast output switching. Both of the MIC4421A GND pins should, however, still be connected to power ground.

Input Stage

The input voltage level of the MIC4421A changes the quiescent supply current. The N-Channel MOSFET input stage transistor drives a 320µA current source load. With a logic "1" input, the quiescent supply current is typically 500µA. Logic "0" input level signals reduce quiescent current to 80µA typical.

The MIC4421A/4422A input is designed to provide 600mV of hysteresis. This provides clean transitions, reduces noise sensitivity, and minimizes output stage current spiking when changing states. Input voltage threshold level is approximately 1.5V, making the device TTL compatible over the full temperature and operating supply voltage ranges. Input current is less than ±10µA.

The MIC4421A can be directly driven by the TL494, SG1526/1527, SG1524, TSC170, MIC38C42, and similar switch mode power supply integrated circuits. By off loading the power-driving duties to the MIC4421A/4422A, the power supply controller can operate at lower dissipation. This can improve performance and reliability.

The input can be greater than the V_S supply, however, current will flow into the input lead. The input currents can be as high as 30mA p-p (6.4mARMS) with the input. No damage will occur to MIC4421A/4422A however, and it will not latch.

The input appears as a 7pF capacitance and does not change even if the input is driven from an AC source. While the device will operate and no damage will occur up to 25V below the negative rail, input current will increase up to 1mA/V due to the clamping action of the input, ESD diode, and 1kΩ resistor.

Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as 4000 and 74C have outputs which can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The MIC4421A/4422A on the other hand, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

The supply current vs. frequency and supply current vs. capacitive load characteristic curves aid in determining power dissipation calculations. Table 1 lists the maximum safe operating frequency for several power supply voltages when driving a 10,000pF load. More accurate power dissipation figures can be obtained by summing the three dissipation sources.

Given the power dissipation in the device, and the thermal resistance of the package, junction operating temperature for any ambient is easy to calculate. For example, the thermal resistance of the 8-pin plastic DIP package, from the data sheet, is 84.6°C/W. In a 25°C ambient, then, using a maximum junction temperature of 150°C, this package will dissipate 1478mW.

Accurate power dissipation numbers can be obtained by summing the three sources of power dissipation in the device:

- Load Power Dissipation (PL)
- Quiescent power dissipation (PQ)
- Transition power dissipation (PT)

Calculation of load power dissipation differs depending on whether the load is capacitive, resistive or inductive.

Resistive Load Power Dissipation

Dissipation caused by a resistive load can be calculated as:

$$P_L = I^2 R_O D$$

where:

I = the current drawn by the load

R_O = the output resistance of the driver when the output is high, at the power supply voltage used. (See data sheet)

D = fraction of time the load is conducting (duty cycle).

Capacitive Load Power Dissipation

Dissipation caused by a capacitive load is simply the energy placed in, or removed from, the load capacitance by the driver. The energy stored in a capacitor is described by the equation:

$$E = 1/2\ C\ V^2$$

As this energy is lost in the driver each time the load is charged or discharged, for power dissipation calculations the 1/2 is removed. This equation also shows that it is good practice not to place more voltage in the capacitor than is necessary, as dissipation increases as the square of the voltage applied to the capacitor. For a driver with a capacitive load:

$$PL = f\ C\ (V_S)^2$$

where:

f = Operating Frequency

C = Load Capacitance

V_S = Driver Supply Voltage

Inductive Load Power Dissipation

For inductive loads the situation is more complicated. For the part of the cycle in which the driver is actively forcing current into the inductor, the situation is the same as it is in the resistive case:

$$P_{L1} = I^2 R_O D$$

However, in this instance the R_O required may be either the on-resistance of the driver when its output is in the high state, or its on-resistance when the driver is in the low state, depending on how the inductor is connected, and this is still only half the story. For the part of the cycle when the inductor is forcing current through the driver, dissipation is best described as:

$$P_{L2} = I\ V_D\ (1 - D)$$

where V_D is the forward drop of the clamp diode in the driver (generally around 0.7V). The two parts of the load dissipation must be summed in to produce P_L:

$$P_L = P_{L1} + P_{L2}$$

Quiescent Power Dissipation

Quiescent power dissipation (PQ, as described in the input section) depends on whether the input is high or low. A low input will result in a maximum current drain (per driver) of ≤ 0.2mA; logic high will result in a current drain of ≤ 3.0mA.

Quiescent power can therefore be found from:

$$P_Q = V_S\ [D\ I_H + (1 - D)\ I_L]$$

where:

I_H = Quiescent current with input high

I_L = Quiescent current with input low

D = Fraction of time input is high (duty cycle)

V_S = Power supply voltage

Transition Power Dissipation

Transition power is dissipated in the driver each time its output changes state, because during the transition, for a very brief interval, both the N- and P-Channel MOSFETs in the output totem-pole are ON simultaneously, and a current is conducted through them from V_S to ground. The transition power dissipation is approximately:

$$P_T = 2\ f\ V_S\ (A \bullet s)$$

where (A•s) is a time-current factor derived from the typical characteristic curve “Crossover Energy vs. Supply Voltage.”

Total power (P_D) then, as previously described is just:

$$P_D = P_L + P_Q + P_T$$

Definitions

C_L = Load Capacitance in Farads.

D = Duty Cycle expressed as the fraction of time the input to the driver is high.

f = Operating Frequency of the driver in Hertz.

I_H = Power supply current drawn by a driver when both inputs are high and neither output is loaded.

I_L = Power supply current drawn by a driver when both inputs are low and neither output is loaded.

I_D = Output current from a driver in Amps.

P_D = Total power dissipated in a driver in Watts.

P_L = Power dissipated in the driver due to the driver’s load in Watts.

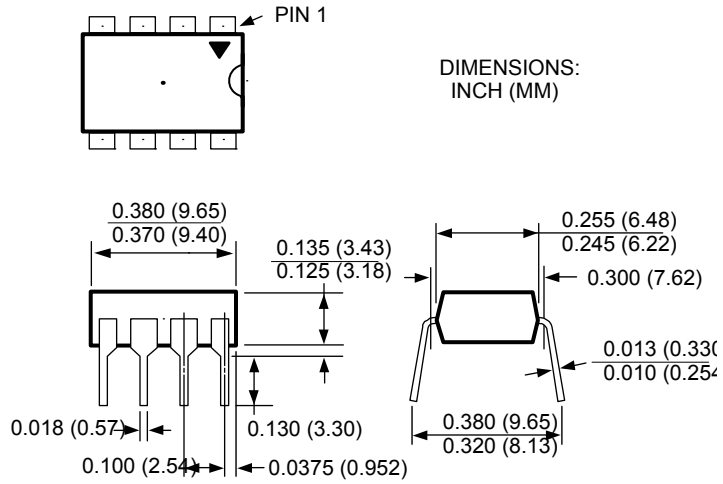
P_Q = Power dissipated in a quiescent driver in Watts.

P_T = Power dissipated in a driver when the output changes states (“shoot-through current”) in Watts.

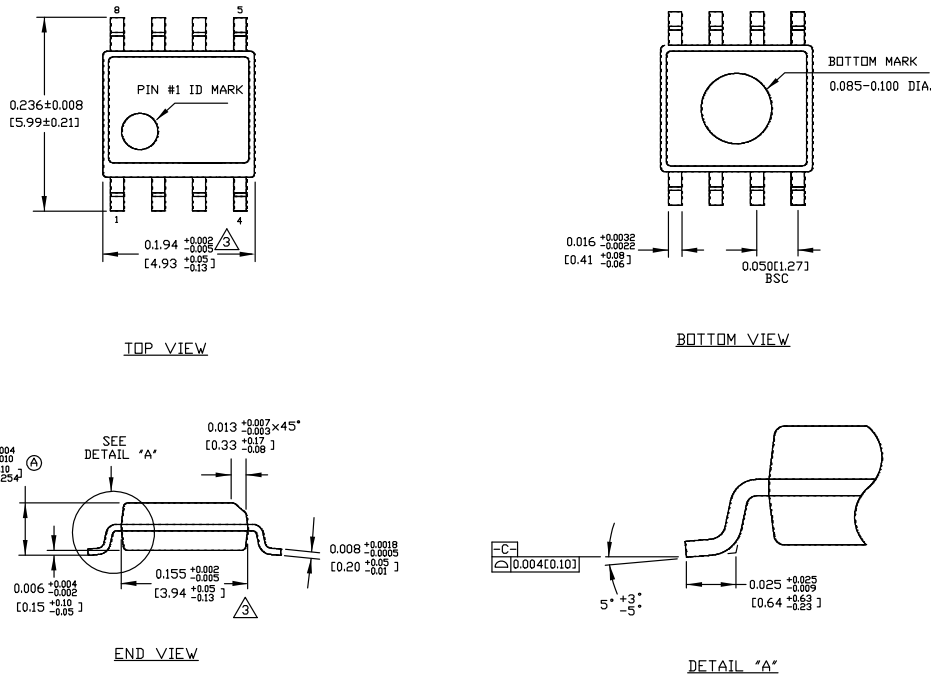
R_O = Output resistance of a driver in Ohms.

V_S = Power supply voltage to the IC in Volts.

Package Information

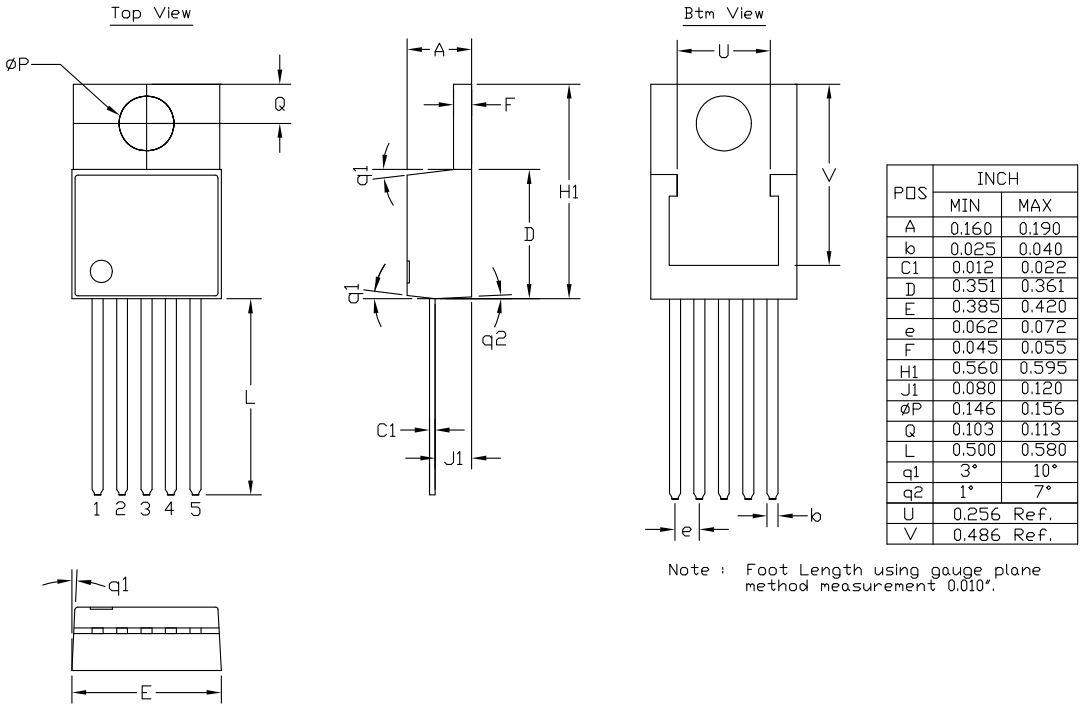


8-Pin Plastic DIP (N)



NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

8-Pin SOIC (M)



POS	INCH	
	MIN	MAX
A	0.160	0.190
b	0.025	0.040
C1	0.012	0.022
D	0.351	0.361
E	0.385	0.420
e	0.062	0.072
F	0.045	0.055
H1	0.560	0.595
J1	0.080	0.120
øP	0.146	0.156
Q	0.103	0.113
L	0.500	0.580
q1	3°	10°
q2	1°	7°
U	0.256 Ref.	
V	0.486 Ref.	

5-Pin TO-220 (T)

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