MCP2003/4/3A/4A

MCP2003/2003A Block Diagram
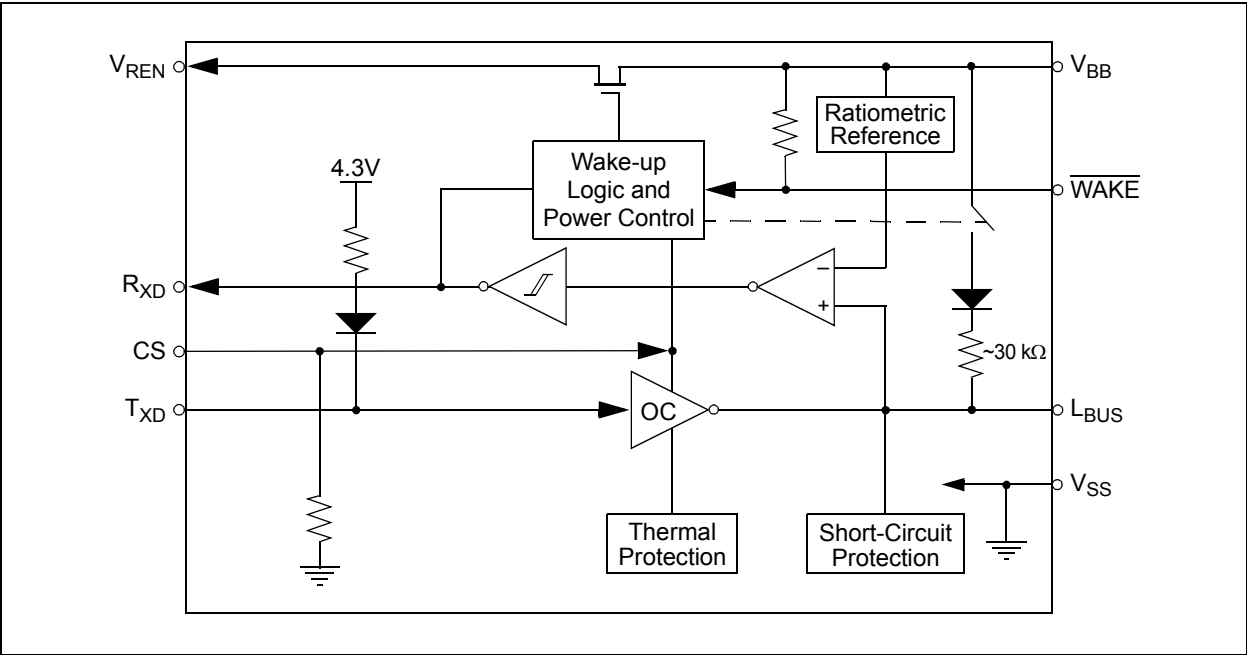
MCP2004/2004A Block Diagram

© 2010-2016 Microchip Technology Inc.
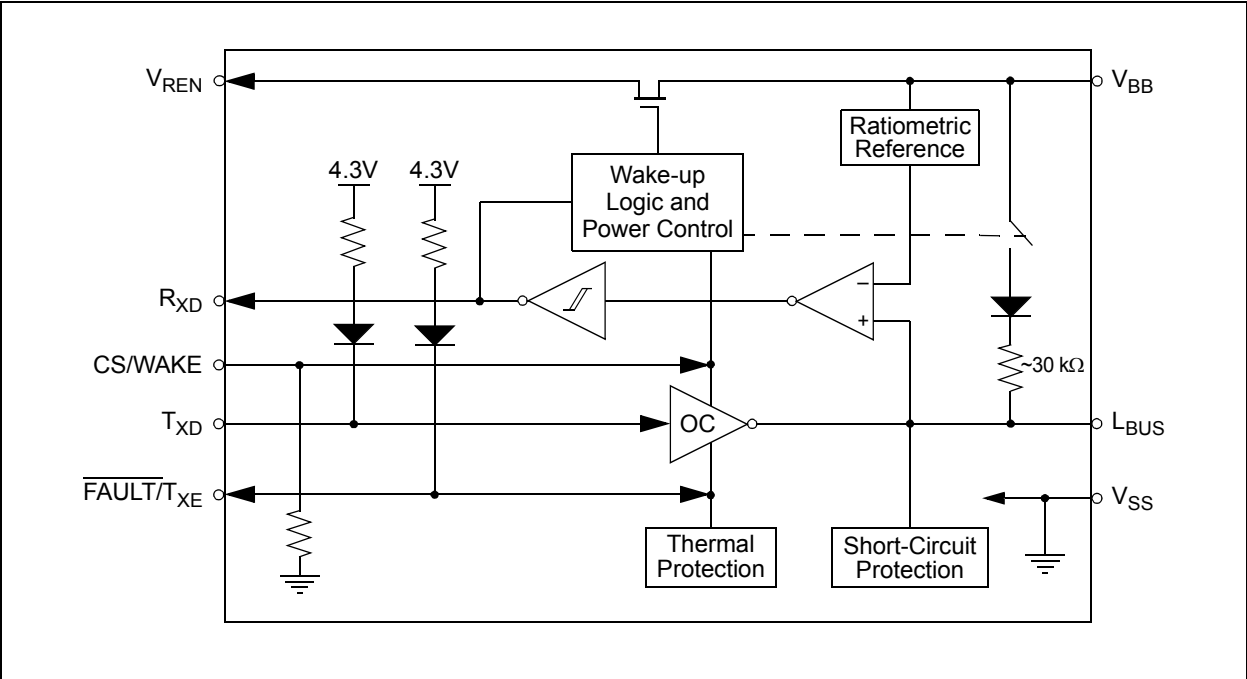
1.0   DEVICE OVERVIEW

The MCP2003/4/3A/4A devices provide a physical interface between a microcontroller and a LIN bus. These devices will translate the CMOS/TTL logic levels to the LIN logic level and vice versa. It is intended for automotive and industrial applications with serial bus speeds up to 20 Kbaud.

LIN Bus Specification Revision 2.1 requires that the transceiver of all nodes in the system is connected via the LIN pin, referenced to ground, and with a maximum external termination resistance load of 510Ω from LIN bus to battery supply. The 510Ω corresponds to 1 master and 15 slave nodes.

The V_{REN} pin can be used to drive the logic input of an external voltage regulator. This pin is high in all modes except for Power-Down mode.

1.1   External Protection

1.1.1   REVERSE BATTERY PROTECTION

An external reverse battery blocking diode should be used to provide polarity protection (see Example 1-1).

1.1.2   TRANSIENT VOLTAGE PROTECTION (LOAD DUMP)

An external 43V Transient Suppressor (TVS) diode, between V_{BB} and ground with a 50Ω Transient Protection Resistor (RTP) in series with the battery supply and the V_{BB} pin, serve to protect the device from power transients (see Example 1-1) and ESD events. While this protection is optional, it is considered good engineering practice.

1.2   Internal Protection

1.2.1   ESD PROTECTION

For component-level ESD ratings, please refer to the maximum operation specifications.

1.2.2   GROUND LOSS PROTECTION

The LIN Bus Specification states that the LIN pin must transition to the Recessive state when the ground is disconnected. Therefore, a loss of ground effectively forces the LIN line to a high-impedance level.

1.2.3   THERMAL PROTECTION

The thermal protection circuit monitors the die temperature and is able to shut down the LIN transmitter.

There are two causes for a thermal overload. A thermal shutdown can be triggered by either, or both, of the following thermal overload conditions:

* LIN bus output overload
* Increase in die temperature due to increase in environment temperature

Driving the T_{XD} pin and checking the R_{XD} pin makes it possible to determine whether there is a bus contention (R_{XD} = low, T_{XD} = high) or a thermal overload condition (R_{XD} = high, T_{XD} = low). After a thermal overload event, the device will automatically recover once the die temperature has fallen below the recovery temperature threshold (see Figure 1-1).

FIGURE 1-1:   THERMAL SHUTDOWN STATE DIAGRAM

Shorted LIN Bus to V_{BB}

Operation Mode — Transmitter Shutdown

Temp < ShutdownTEMP
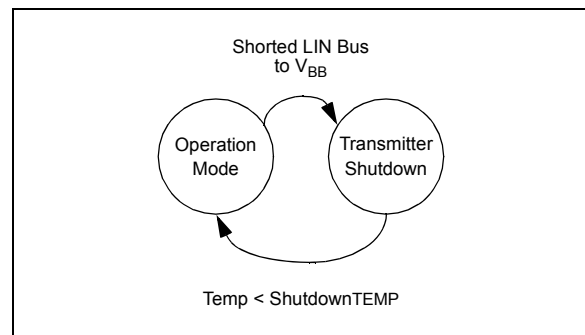
1.3 Modes of Operation

For an overview of all operational modes, refer to Table 1-1.

1.3.1 POWER-DOWN MODE

In Power-Down mode, everything is off except the wake-up section. This is the lowest power mode. The receiver is off, thus its output is open-drain.

On CS going to a high level or a falling edge on $\overline{\text{WAKE}}$ (MCP2003/MCP2003A only), the device will enter Ready mode as soon as the internal voltage stabilizes. Refer to **Section 2.4 "AC Specifications"** for further information. In addition, LIN bus activity will change the device from Power-Down mode to Ready mode; MCP2003/4 wakes up on a falling edge on L_{BUS}, followed by a low level lasting at least 20 µs. MCP2003A/4A wakes up on a rising edge on L_{BUS}, followed by a high level lasting 70 µs, typically. See Figures 1-2 to 1-5 about remote wake-up. If CS is held high as the device transitions from Power-Down to Ready mode, the device will transition to either Operation or Transmitter Off mode, depending on the T_{XD} input, as soon as internal voltages stabilize.

1.3.2 READY MODE

Upon entering Ready mode, V_{REN} is enabled and the receiver detect circuit is powered up. The transmitter remains disabled and the device is ready to receive data but not to transmit.

Upon V_{BB} supply pin power-on, the device will remain in Ready mode as long as CS is low. When CS transitions high, the device will either enter Operation mode, if the T_{XD} pin is held high, or the device will enter Transmitter Off mode, if the T_{XD} pin is held low.

1.3.3 OPERATION MODE

In this mode, all internal modules are operational.

The device will go into Power-Down mode on the falling edge of CS. For the MCP2003/4 device, a specific process should be followed to put all nodes into Power-Down mode. Refer to **Section 1.6 "MCP2003/4 and MCP2003A/4A Difference Details"** and Figure 1-6. The device will enter Transmitter Off mode in the event of a Fault condition, such as thermal overload, bus contention and T_{XD} timer expiration.

The MCP2004/2004A device can also enter Transmitter Off mode if the $\overline{\text{FAULT}}/T_{XE}$ pin is pulled low. The V_{BB} to L_{BUS} pull-up resistor is connected only in Operation mode.

1.3.4 TRANSMITTER OFF MODE

Transmitter Off mode is reached whenever the transmitter is disabled, either due to a Fault condition or pulling the $\overline{\text{FAULT}}/T_{XE}$ pin low on the MCP2004/2004A. The Fault conditions include: thermal overload, bus contention, R_{XD} monitoring or T_{XD} timer expiration.

The device will go into Power-Down mode on the falling edge of CS or return to Operation mode if all Faults are resolved and the $\overline{\text{FAULT}}/T_{XE}$ pin on the MCP2004/2004A is high.

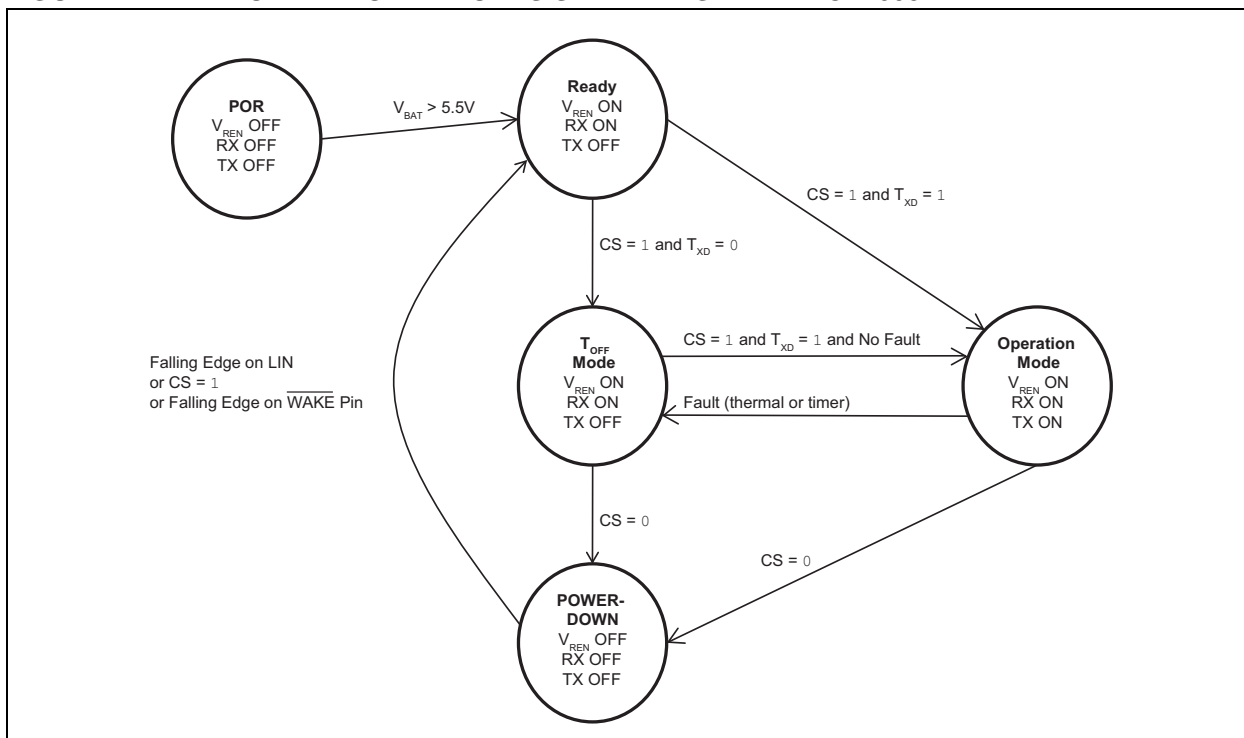**FIGURE 1-2:** **OPERATIONAL MODES STATE DIAGRAM – MCP2003**

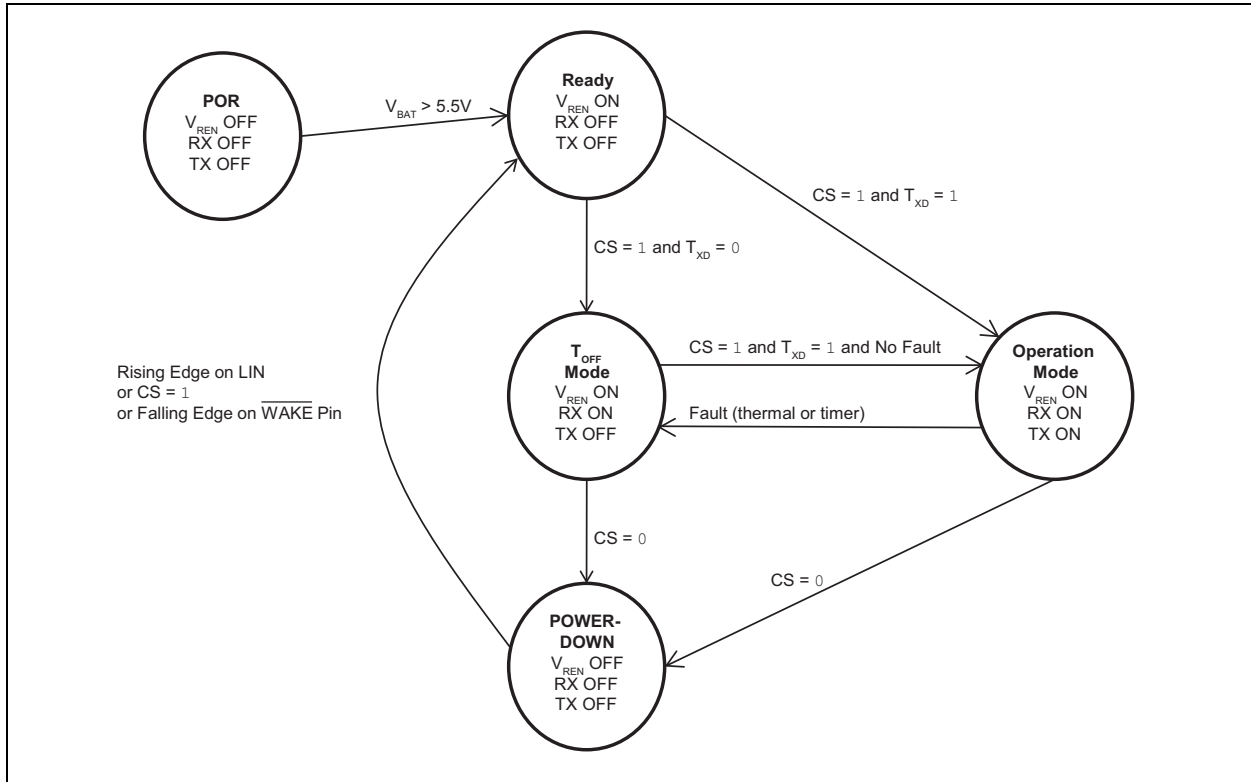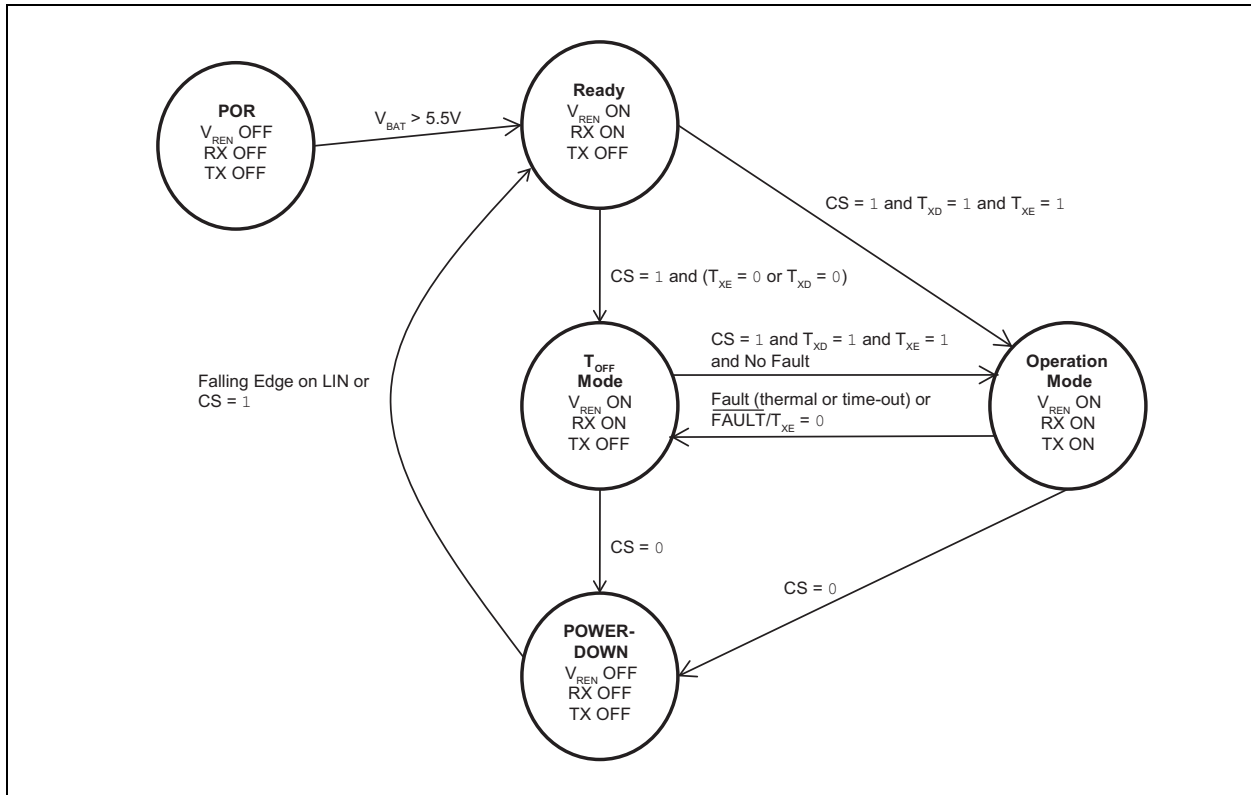**FIGURE 1-3:** **OPERATIONAL MODES STATE DIAGRAM – MCP2003A**

FIGURE 1-4: **OPERATIONAL MODES STATE DIAGRAM – MCP2004**

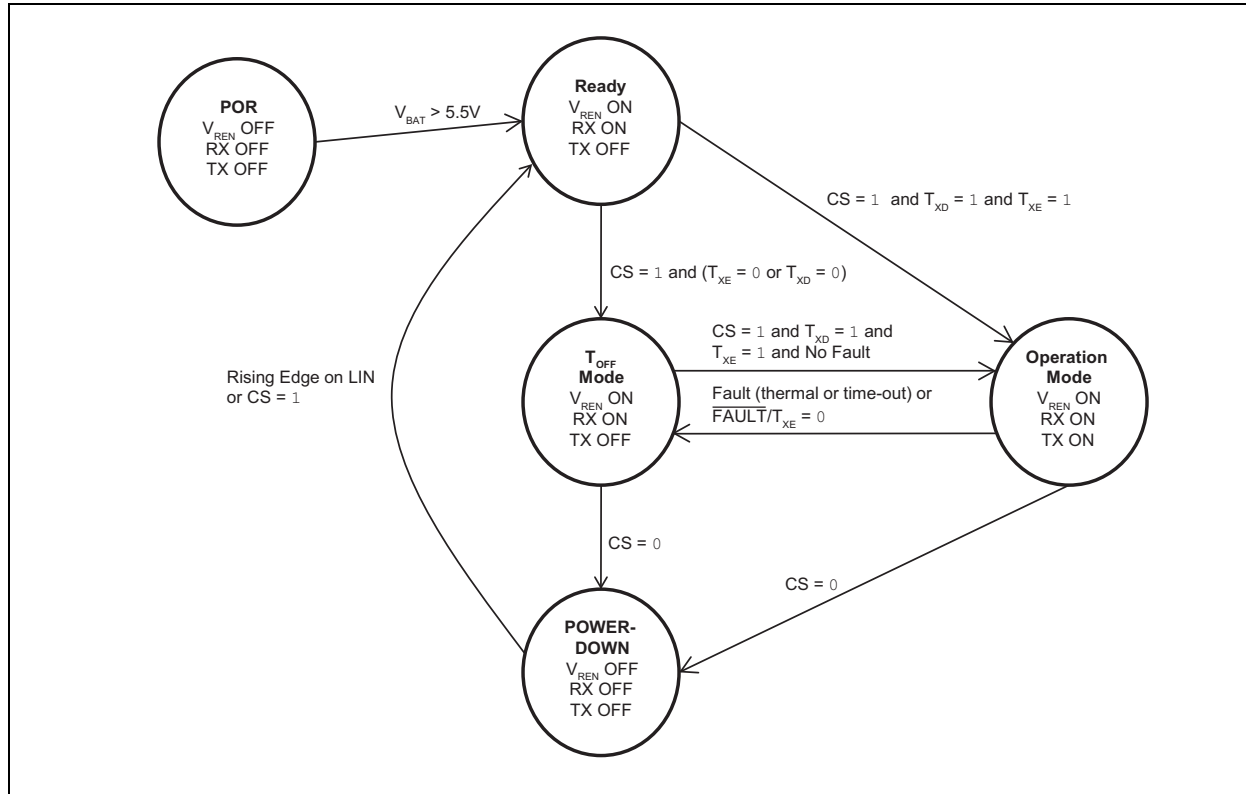**FIGURE 1-5:** **OPERATIONAL MODES STATE DIAGRAM – MCP2004A**

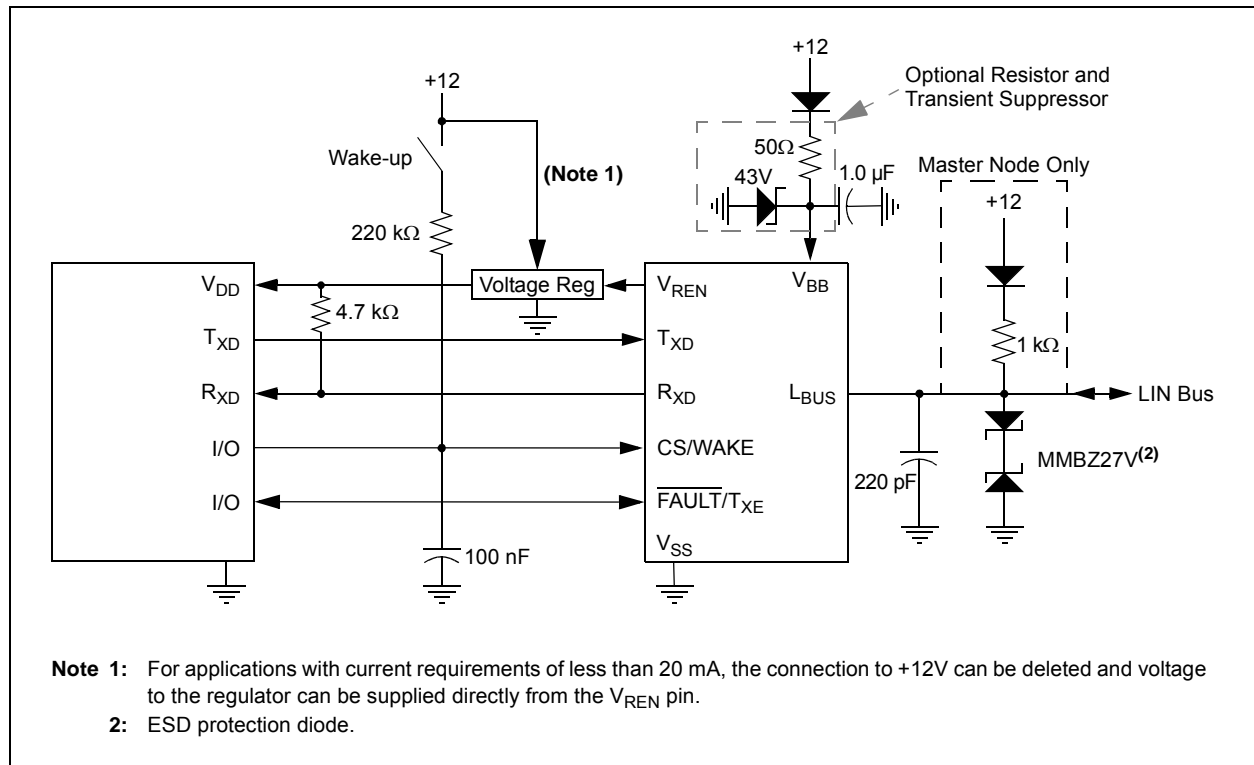**TABLE 1-1:** **OVERVIEW OF OPERATIONAL MODES**

State	Transmitter	Receiver	V_{REN}	Operation	Comments
POR	OFF	OFF	OFF	Check CS; if low, then proceed to Ready mode. If high, transitions to either T_{OFF} or Operation mode, depending on T_{XD} (MCP2003/A), or T_{XD} and $\overline{FAULT}/T_{XE}$ (MCP2004/A).	$V_{BB} > V_{BB(MIN)}$ and internal supply is stable
Ready	OFF	ON	ON	If CS is a high level, then proceed to Operation or T_{OFF} mode.	Bus Off state
Operation	ON	ON	ON	If CS is a low level, then proceed to Power-Down mode. If $\overline{FAULT}/T_{XE}$ is a low level, then proceed to Transmitter Off mode.	Normal Operation mode
Power-Down	OFF	Activity Detect	OFF	On CS high level, proceed to Ready mode; then proceed to either Operation mode or T_{OFF} mode. MCP2003/2003A: Falling edge on $\overline{WAKE}$ will put the device into Ready mode. MCP2003/MCP2004: Falling edge on LIN bus will put the device into Ready mode. MCP2003A/MCP2004A: Rising edge on LIN bus will put the device into Ready mode.	Low-Power mode
Transmitter Off	OFF	ON	ON	If CS is a low level, then proceed to Power-Down mode. If $\overline{FAULT}/T_{XE}$ and T_{XD} are high, then proceed to Operation mode.	$\overline{FAULT}/T_{XE}$ is only available on MCP2004/2004A

1.4   Typical Applications

EXAMPLE 1-1:   TYPICAL MCP2003/2003A APPLICATION

Note 1: For applications with current requirements of less than 20 mA, the connection to +12V can be deleted and voltage to the regulator can be supplied directly from the V_{REN} pin.

2: ESD protection diode.
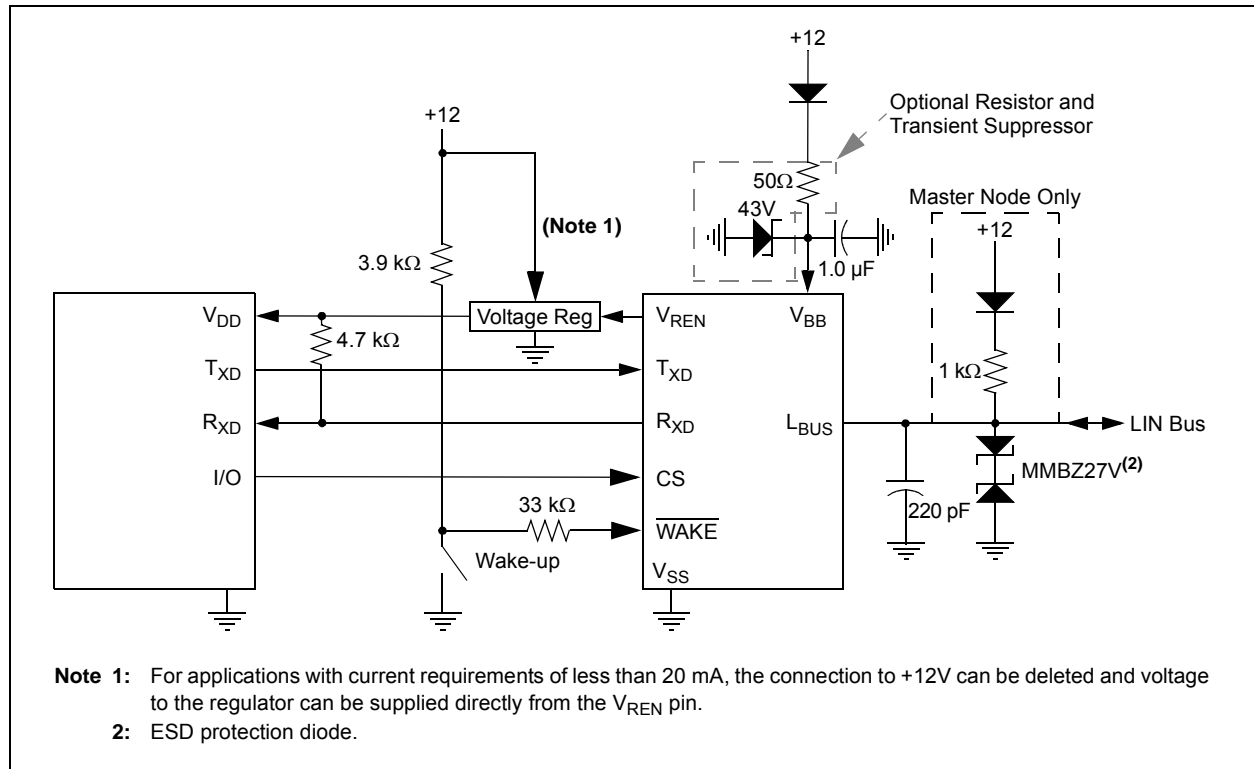
EXAMPLE 1-2:   TYPICAL MCP2004/2004A APPLICATION

Note 1: For applications with current requirements of less than 20 mA, the connection to +12V can be deleted and voltage to the regulator can be supplied directly from the V_{REN} pin.

2: ESD protection diode.

EXAMPLE 1-3:   TYPICAL LIN NETWORK CONFIGURATION
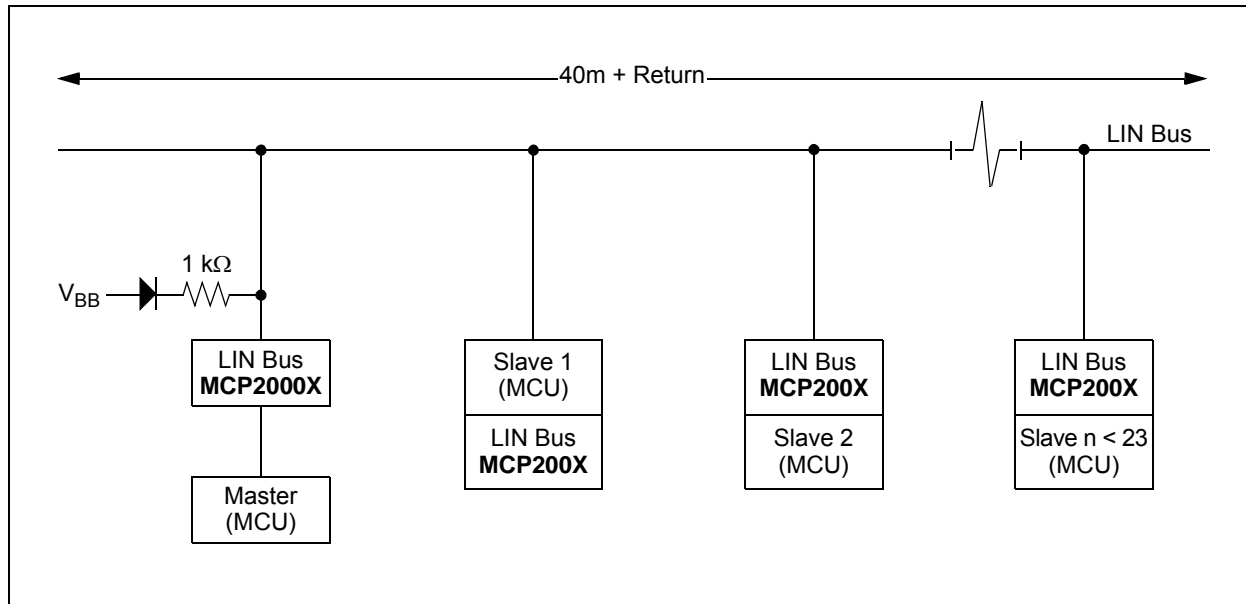
1.5 Pin Descriptions

TABLE 1-2: PINOUT DESCRIPTIONS

Pin Name	8-Lead PDIP, SOIC	4x4 DFN	MCP2003/2003A	MCP2004/2004A
			Normal Operation	**Normal Operation**
R_{XD}	1	1	Receive Data Output (OD), HV tolerant	Receive Data Output (OD), HV tolerant
CS	2	2	Chip Select (TTL), HV tolerant	Chip Select/Local $\overline{WAKE}$ (TTL), HV tolerant
$\overline{WAKE}$ (MCP2003/2003A only) $\overline{FAULT}/T_{XE}$ (MCP2004/2004A only)	3	3	Wake-up, HV tolerant	Fault Detect Output (OD), Transmitter Enable (TTL), HV tolerant
T_{XD}	4	4	Transmit Data Input (TTL), HV tolerant	Transmit Data Input (TTL), HV tolerant
V_{SS}	5	5	Ground	Ground
L_{BUS}	6	6	LIN Bus (bidirectional)	LIN Bus (bidirectional)
V_{BB}	7	7	Battery Positive	Battery Positive
V_{REN}	8	8	Voltage Regulator Enable Output	Voltage Regulator Enable Output
EP	—	9	Exposed Thermal Pad; do not electrically connect or connect to V_{SS}	Exposed Thermal Pad; do not electrically connect or connect to V_{SS}

Legend: TTL = TTL Input Buffer; OD = Open-Drain Output

1.5.1 RECEIVE DATA OUTPUT (R_{XD})

The Receive Data Output pin is an Open-Drain (OD) output and follows the state of the LIN pin, except in Power-Down mode.

1.5.1.1 R_{XD} Monitoring

The R_{XD} pin is internally monitored. It has to be at a high level (> 2.5V typical) while L_{BUS} is recessive. Otherwise, an internal Fault will be created and the device will transition to Transmitter Off mode. On the MCP2004/2004A, the $\overline{FAULT}/T_{XE}$ pin will be driven low to indicate the Transmitter Off state.

1.5.2 CHIP SELECT (CS)

This is the Chip Select input pin. An internal pull-down resistor will keep the CS pin low. This is done to ensure that no disruptive data will be present on the bus while the microcontroller is executing a Power-on Reset and an I/O initialization sequence. The pin must detect a high level to activate the transmitter. An internal low-pass filter, with a typical time constant of 10 µs, prevents unwanted wake-up (or transition to Power-Down mode) on glitches.

If CS = 0 when the V_{BB} supply is turned on, the device goes to Ready mode as soon as internal voltages stabilize and stays there as long as the CS pin is held low (0). In Ready mode, the receiver is on and the LIN transmitter driver is off.

If CS = 1 when the V_{BB} supply is turned on, the device will proceed to Operation mode or T_{OFF} mode (refer to Figures 1-2 to 1-5) as soon as internal voltages stabilize.

This pin may also be used as a local wake-up input (refer to Example 1-1). In this implementation, the microcontroller I/O controlling the CS should be converted to a high-impedance input, allowing the internal pull-down resistor to keep CS low. An external switch, or other source, can then wake-up both the transceiver and the microcontroller (if powered). Refer to **Section 1.3 "Modes of Operation"**, for detailed operation of CS.

Note:	It is not recommended to tie CS high as this can result in the device entering Operation mode before the microcontroller is initialized and may result in unintentional LIN traffic.

1.5.3 WAKE-UP INPUT ($\overline{WAKE}$)

This pin is only available on the MCP2003/2003A.

The $\overline{WAKE}$ pin has an internal 800 kΩ pull-up to V_{BB}. A falling edge on the $\overline{WAKE}$ pin causes the device to wake from Power-Down mode. Upon waking, the MCP2003/3A will enter Ready mode.

1.5.4 $\overline{\text{FAULT}}$/T$_{XE}$

This pin is only available on the MCP2004/2004A. This pin is bidirectional and allows disabling of the transmitter, as well as Fault reporting related to disabling the transmitter. This pin is an open-drain output with states as defined in Table 1-3. The transmitter is disabled whenever this pin is low ('0'), either from an internal

Fault condition or by an external drive. While the transmitter is disabled, the internal 30 kΩ pull-up resistor on the L$_{BUS}$ pin is also disconnected to reduce current.

> **Note:** The $\overline{\text{FAULT}}$/T$_{XE}$ pin is true ('0') whenever the internal circuits have detected a short or thermal excursion and have disabled the L$_{BUS}$ output driver.

TABLE 1-3: $\overline{\text{FAULT}}$/T$_{XE}$ TRUTH TABLE

T$_{XD}$ In	R$_{XD}$ Out	LIN$_{BUS}$ I/O	Thermal Override	$\overline{\text{FAULT}}$/T$_{XE}$ External Input	Driven Output	Definition
L	H	V$_{BB}$	OFF	H	L	**FAULT**, T$_{XD}$ driven low, L$_{BUS}$ shorted to V$_{BB}$ (**Note 1**)
H	H	V$_{BB}$	OFF	H	H	**OK**
L	L	GND	OFF	H	H	**OK**
H	L	GND	OFF	H	H	**OK**, data is being received from L$_{BUS}$
x	x	V$_{BB}$	ON	H	L	**FAULT**, transceiver in thermal shutdown
x	x	V$_{BB}$	x	L	x	**NO FAULT**, the CPU is commanding the transceiver to turn off the transmitter driver

Legend: x = don't care.
Note 1: The $\overline{\text{FAULT}}$/T$_{XE}$ is valid after approximately 25 µs after the T$_{XD}$ falling edge. This is to eliminate false Fault reporting during bus propagation delays.

1.5.5 TRANSMIT DATA INPUT (T$_{XD}$)

The Transmit Data input pin has an internal pull-up. The LIN pin is low (dominant) when T$_{XD}$ is low and high (recessive) when T$_{XD}$ is high.

For extra bus security, T$_{XD}$ is internally forced to '1' whenever the transmitter is disabled, regardless of the external T$_{XD}$ voltage.

1.5.5.1 T$_{XD}$ Dominant Time-out

If T$_{XD}$ is driven low for longer than approximately 25 ms, the L$_{BUS}$ pin is switched to Recessive mode and the part enters T$_{OFF}$ mode. This is to prevent the LIN node from permanently driving the LIN bus dominant. The transmitter is reenabled on the T$_{XD}$ rising edge.

1.5.6 GROUND (V$_{SS}$)

This is the Ground pin.

1.5.7 LIN BUS (L$_{BUS}$)

The bidirectional LIN Bus pin (L$_{BUS}$) is controlled by the T$_{XD}$ input. L$_{BUS}$ has a current-limited open-collector output. To reduce EMI, the edges, during the signal changes, are slope controlled, and include corner rounding control for both falling and rising edges.

The internal LIN receiver observes the activities on the LIN bus and matches the output signal, R$_{XD}$, to follow the state of the L$_{BUS}$ pin.

1.5.7.1 Bus Dominant Timer

The Bus Dominant Timer is an internal timer that deactivates the L$_{BUS}$ transmitter after approximately 25 ms of Dominant state on the L$_{BUS}$ pin. The timer is reset on any recessive L$_{BUS}$ state.

The LIN bus transmitter will be reenabled after a Recessive state on the L$_{BUS}$ pin as long as CS is high. Disabling can be caused by the LIN bus being externally held dominant or by T$_{XD}$ being driven low. Additionally, on the MCP2004/2004A, the $\overline{\text{FAULT}}$ pin will be driven low to indicate the Transmitter Off state.

1.5.8 BATTERY (V$_{BB}$)

This is the Battery Positive Supply Voltage pin.

1.5.9 VOLTAGE REGULATOR ENABLE OUTPUT (V$_{REN}$)

This is the External Voltage Regulator Enable pin. The open source output is pulled high to V$_{BB}$ in all modes, except Power-Down.

1.5.10 EXPOSED THERMAL PAD (EP)

Do not electrically connect or connect to V$_{SS}$.

1.6 MCP2003/4 and MCP2003A/4A Difference Details

The differences between the MCP2003/4 and the MCP2003A/4A devices are isolated to the wake-up functionality. The changes were implemented to make the device more robust to LIN bus conditions outside of the normal operating conditions. The MCP2003/4 will wake-up from Power-Down mode during any LIN falling edge held low longer than 20 µs.

In the case where a LIN system is designed to minimize standby current by disconnecting all bus pull-up resistors (including the external master pull-up resistor to V_{BB}), the original MCP2003/4 could wake-up if the floating bus drifted to a valid low level. The MCP2003A/4A revisions were modified to require a rising edge after a valid low level. This will prevent an undesired system wake-up in this scenario, while maintaining functional capability with the original version.

It should be noted that the original MCP2003/4 meets all LIN transceiver specification requirements and modules can be designed to pass all LIN system requirements. However, when all bus pull-up resistors are disconnected, the MCP2003/4 requires the module designer to write firmware to monitor the LIN bus, after any wake-up event, to prevent the transceiver from automatically transitioning from Ready mode to Operational mode.

If the MCP2003/4 is placed into Operational mode, the V_{BB} to L_{BUS} pull-up resistor is automatically connected, which will raise the LIN bus to a Recessive level; then putting the device into Power-Down mode may cause L_{BUS} to be floating, and thus, wake-up all bus nodes. To prevent this, the designer should ensure T_{XD} (MCP2003) or T_{XE} (MCP2004) is held low until valid bus activity is verified (see Figure 1-6). This will ensure the transceiver transitions from Ready mode to Transmitter Off mode until bus activity can be verified.

In the case of valid bus activity, the transceiver can shift to Operation mode; while if there is no bus activity, the device can again be placed into Power-Down mode. The design practices needed to accomplish this are fully detailed in Tech Brief TB3067, "*MCP2003 Power-Down Mode and Wake-up Handling in the Case of LIN Bus Loss*" (DS93067).

The revised MCP2003A/4A devices now eliminate the need for firmware to prevent system wide wake-up. The revised devices now require a longer valid bus low (see updated t_{BDB} value in **Section 2.3 "DC Specifications"** and Figure 2-7), which enables a rising edge detect circuit. The device will now only wake-up after a rising edge, following a low longer than t_{BDB}. While the module designer can still hold T_{XD} (MCP2003) or T_{XE} (MCP2004) low during wake-up to enter Transmitter Off mode from Ready mode, it is not required to prevent an advertent system wake-up.

In addition to the longer t_{BDB} value, the time from wake-up detect to V_{REN} enable is shortened, as documented in **Section 2.3 "DC Specifications"**.

FIGURE 1-6: MCP2003/2004 SWITCHING TIMING DIAGRAM FOR THE FORCED POWER-DOWN MODE SEQUENCE
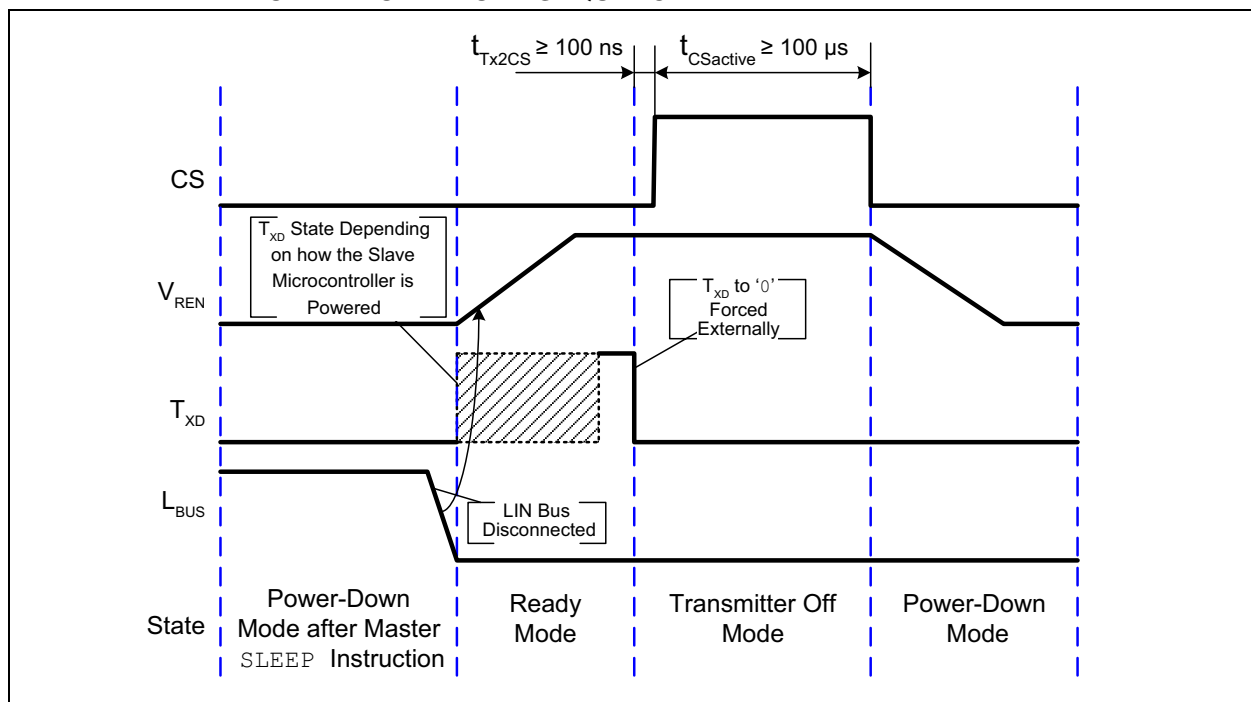
2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings†

V_{IN} DC Voltage on R_{XD}, T_{XD}, $\overline{FAULT}$/T_{XE}, CS .... -0.3 to +43V

V_{IN} DC Voltage on $\overline{WAKE}$ and V_{REN} .... -0.3 to +V_{BB}

V_{BB} Battery Voltage, Continuous, Non-Operating **(Note 1)** .... -0.3 to +40V

V_{BB} Battery Voltage, Non-Operating (LIN bus recessive) **(Note 2)** .... -0.3 to +43V

V_{BB} Battery Voltage, Transient ISO 7637 Test 1 .... -200V

V_{BB} Battery Voltage, Transient ISO 7637 Test 2a .... +150V

V_{BB} Battery Voltage, Transient ISO 7637 Test 3a .... -300V

V_{BB} Battery Voltage, Transient ISO 7637 Test 3b .... +200V

V_{LBUS} Bus Voltage, Continuous .... -18 to +40V

V_{LBUS} Bus Voltage, Transient **(Note 3)** .... -27 to +43V

I_{LBUS} Bus Short-Circuit Current Limit .... 200 mA

ESD Protection on LIN, V_{BB}, $\overline{WAKE}$ (IEC 61000-4-2) **(Note 4)** .... ±8 KV

ESD Protection on LIN, V_{BB} (Human Body Model) **(Note 5)** .... ±8 KV

ESD Protection on All Other Pins (Human Body Model) **(Note 5)** .... ±4 KV

ESD Protection on All Pins (Charge Device Model) **(Note 6)** .... ±2 KV

ESD Protection on All Pins (Machine Model) **(Note 7)** .... ±200V

Maximum Junction Temperature .... 150°C

Storage Temperature .... -65 to +150°C

> **† NOTICE**: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device, at those or any other conditions above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: LIN 2.x compliant specification.
  2: SAE J2602 compliant specification.
  3: ISO 7637/1 load dump compliant (t < 500 ms).
  4: According to IEC 61000-4-2, 330 ohm, 150 pF and Transceiver EMC Test Specifications [2] to [4]. For $\overline{WAKE}$ pin to meet the specification, a series resistor must be in place (refer to Example 1-2).
  5: According to AEC-Q100-002/JESD22-A114.
  6: According to AEC-Q100-011B.
  7: According to AEC-Q100-003/JESD22-A115.

2.2 Nomenclature Used in This Document

Some terms and names used in this data sheet deviate from those referred to in the LIN specifications. Equivalent values are shown below.

LIN 2.1 Name	Term Used in the Following Tables	Definition
V_{BAT}	*not used*	ECU operating voltage
V_{SUP}	V_{BB}	Supply voltage at device pin
I_{BUS_LIM}	I_{SC}	Current limit of driver
V_{BUSREC}	$V_{IH(LBUS)}$	Recessive state
V_{BUSDOM}	$V_{IL(LBUS)}$	Dominant state

2.3   DC Specifications

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for V_{BB} = 6.0V to 30.0V, T_A = -40°C to +125°C					
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power						
V_{BB} Quiescent Operating Current	I_{BBQ}	—	90	150	µA	Operating mode, bus is Recessive **(Note 1)**
V_{BB} Transmitter Off Current	I_{BBTO}	—	75	120	µA	Transmitter off, bus is Recessive **(Note 1)**
V_{BB} Power-Down Current	I_{BBPD}	—	5	15	µA	
V_{BB} Current with V_{SS} Floating	$I_{BBNOGND}$	-1	—	1	mA	V_{BB} = 12V, GND to V_{BB}, V_{LIN} = 0-27V
Microcontroller Interface						
High-Level Input Voltage (T_{XD}, $\overline{FAULT}/T_{XE}$)	V_{IH}	2.0	—	30	V	
Low-Level Input Voltage (T_{XD}, $\overline{FAULT}/T_{XE}$)	V_{IL}	-0.3	—	0.8	V	
High-Level Input Current (T_{XD}, $\overline{FAULT}/T_{XE}$)	I_{IH}	-2.5	—	—	µA	Input voltage = 4.0V
Low-Level Input Current (T_{XD}, $\overline{FAULT}/T_{XE}$)	I_{IL}	-10	—	—	µA	Input voltage = 0.5V
High-Level Voltage (V_{REN})	V_{HVREN}	-0.3	—	V_{BB} + 0.3	V	
High-Level Output Current (V_{REN})	I_{HVREN}	-40	—	-10	mA	Output voltage = V_{BB} – 0.5V
		-125	—	-35		Output voltage = V_{BB}-2.0V
High-Level Input Voltage (CS)	V_{IH}	2.0	—	30	V	Through a current-limiting resistor
Low-Level Input Voltage (CS)	V_{IL}	-0.3	—	0.8	V	
High-Level Input Current (CS)	I_{IH}	—	—	10.0	µA	Input voltage = 4.0V
Low-Level Input Current (CS)	I_{IL}	—	—	5.0	µA	Input voltage = 0.5V
Low-Level Input Voltage ($\overline{WAKE}$)	V_{IL}	V_{BB} – 4.0V	—	—	V	
Low-Level Output Voltage (R_{XD})	V_{OL}	—	—	0.4	V	I_{IN} = 2 mA
High-Level Output Current (R_{XD})	I_{OH}	-1	—	-1	µA	V_{LIN} = V_{BB}, V_{RXD} = 5.5V

Note 1:   Internal current limited; 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, TX = 0.4 V_{REG}, V_{LBUS} = V_{BB}).

2:    Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

2.3 DC Specifications (Continued)

DC Specifications	**Electrical Characteristics:** Unless otherwise indicated, all limits are specified for V_{BB} = 6.0V to 30.0V, T_A = -40°C to +125°C					
Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Bus Interface						
High-Level Input Voltage	$V_{IH(LBUS)}$	0.6 V_{BB}	—	—	V	Recessive state
Low-Level Input Voltage	$V_{IL(LBUS)}$	-8	—	0.4 V_{BB}	V	Dominant state
Input Hysteresis	V_{HYS}	—	—	0.175 V_{BB}	V	$V_{IH(LBUS)} - V_{IL(LBUS)}$
Low-Level Output Current	$I_{OL(LBUS)}$	40	—	200	mA	Output voltage = 0.1 V_{BB}, V_{BB} = 12V
High-Level Output Current	$I_{OH(LBUS)}$	—	—	20	µA	
Pull-up Current on Input	$I_{PU(LBUS)}$	5	—	180	µA	~30 kΩ internal pull-up @ $V_{IH(LBUS)}$ = 0.7 V_{BB}
Short-Circuit Current Limit	I_{SC}	50	—	200	mA	**(Note 1)**
High-Level Output Voltage	$V_{OH(LBUS)}$	0.9 V_{BB}	—	V_{BB}	V	
Driver Dominant Voltage	$V_{\_LOSUP}$	—	—	1.2	V	V_{BB} = 7V, R_{LOAD} = 500Ω
Driver Dominant Voltage	$V_{\_HISUP}$	—	—	2.0	V	V_{BB} = 18V, R_{LOAD} = 500Ω
Driver Dominant Voltage	$V_{\_LOSUP}$ – 1k	0.6	—	—	V	V_{BB} = 7V, R_{LOAD} = 1 kΩ
Driver Dominant Voltage	$V_{\_HISUP}$ – 1k	0.8	—	—	V	V_{BB} = 18V, R_{LOAD} = 1 kΩ
Input Leakage Current (at the receiver during Dominant bus level)	$I_{BUS\_PAS\_DOM}$	-1	-0.4	—	mA	Driver off, V_{BUS} = 0V, V_{BB} = 12V
Input Leakage Current (at the receiver during Recessive bus level)	$I_{BUS\_PAS\_REC}$	—	12	20	µA	Driver off, 8V < V_{BB} < 18V, 8V < V_{BUS} < 18V, $V_{BUS} \geq V_{BB}$
Leakage Current (disconnected from ground)	$I_{BUS\_NO\_GND}$	-10	1.0	+10	µA	GND_{DEVICE} = V_{BB}, 0V < V_{BUS} < 18V, V_{BB} = 12V
Leakage Current (disconnected from V_{BB})	$I_{BUS\_NO\_VBB}$	—	—	10	µA	V_{BB} = GND, 0 < V_{BUS} < 18V **(Note 2)**
Receiver Center Voltage	V_{BUS_CNT}	0.475 V_{BB}	0.5 V_{BB}	0.525 V_{BB}	V	V_{BUS_CNT} = ($V_{IL(LBUS)}$ + $V_{IH(LBUS)}$)/2
Slave Termination	R_{SLAVE}	20	30	47	kΩ	
Capacitance of Slave Node	C_{SLAVE}	—	—	50	pF	

Note 1: Internal current limited; 2.0 ms maximum recovery time (R_{LBUS} = 0Ω, TX = 0.4 V_{REG}, V_{LBUS} = V_{BB}).

2: Node has to sustain the current that can flow under this condition; bus must be operational under this condition.

2.4   AC Specifications

AC Characteristics	Electrical Characteristics: Unless otherwise indicated, all limits are specified for V_{BB} = 6.0V to 27.0V; T_A = -40°C to +125°C					
Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Bus Interface – Constant Slope Time Parameters						
Slope Rising and Falling Edges	t_{SLOPE}	3.5	—	22.5	µs	$7.3V \leq V_{BB} \leq 18V$
Propagation Delay of Transmitter	$t_{TRANSPD}$	—	—	4.0	µs	$t_{TRANSPD}$ = max ($t_{TRANSPDR}$ or $t_{TRANSPDF}$)
Propagation Delay of Receiver	t_{RECPD}	—	—	6.0	µs	t_{RECPD} = max (t_{RECPDR} or t_{RECPDF})
Symmetry of Propagation Delay of Receiver Rising Edge w.r.t. Falling Edge	t_{RECSYM}	-2.0	—	2.0	µs	t_{RECSYM} = max ($t_{RECPDF} - t_{RECPDR}$) R_{RXD} 2.4Ω to V_{CC}, C_{RXD} 20 pF
Symmetry of Propagation Delay of Transmitter Rising Edge w.r.t. Falling Edge	$t_{TRANSSYM}$	-2.0	—	2.0	µs	$t_{TRANSSYM}$ = max ($t_{TRANSPDF} - t_{TRANSPDR}$)
Time to Sample $\overline{FAULT}$/T_{XE} for Bus Conflict Reporting	t_{FAULT}	—	—	32.5	µs	t_{FAULT} = max ($t_{TRANSPD} + T_{SLOPE} + t_{RECPD}$)
Duty Cycle 1 @ 20.0 kbit/sec		0.396	—	—	—	C_{BUS}; R_{BUS} Conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω, $TH_{REC(MAX)}$ = 0.744 x V_{BB}, $TH_{DOM(MAX)}$ = 0.581 x V_{BB}, V_{BB} = 7.0V – 18V, t_{BIT} = 50 µs, D1 = $t_{BUS\_REC(MIN)}$/2 x t_{BIT})
Duty Cycle 2 @ 20.0 kbit/sec		—	—	0.581	—	C_{BUS}; R_{BUS} Conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω, $TH_{REC(MAX)}$ = 0.284 x V_{BB}, $TH_{DOM(MAX)}$ = 0.422 x V_{BB}, V_{BB} = 7.6V – 18V, t_{BIT} = 50 µs, D2 = $t_{BUS\_REC(MAX)}$/2 x t_{BIT}
Duty Cycle 3 @ 10.4 kbit/sec		0.417	—	—	—	C_{BUS}; R_{BUS} Conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω, $TH_{REC(MAX)}$ = 0.778 x V_{BB}, $TH_{DOM(MAX)}$ = 0.616 x V_{BB}, V_{BB} = 7.0V – 18V, t_{BIT} = 96 µs, D3 = $t_{BUS\_REC(MIN)}$/2 x t_{BIT})
Duty Cycle 4 @ 10.4 kbit/sec		—	—	0.590	—	C_{BUS}; R_{BUS} Conditions: 1 nF; 1 kΩ | 6.8 nF; 660Ω | 10 nF; 500Ω, $TH_{REC(MAX)}$ = 0.251 x V_{BB}, $TH_{DOM(MAX)}$ = 0.389 x V_{BB}, V_{BB} = 7.6V – 18V, t_{BIT} = 96 µs, D4 = $t_{BUS\_REC(MAX)}$/2 x t_{BIT}
Wake-up Timing						
Bus Activity Debounce Time	t_{BDB}	5	—	20	µs	MCP2003/2004
		30	70	125	µs	MCP2003A/2004A
Bus Activity to V_{REN} On	t_{BACTVE}	35	—	150	µs	MCP2003/2004
		10	30	90	µs	MCP2003A/2004A
$\overline{WAKE}$ to V_{REN} On	t_{WAKE}	—	—	150	µs	
Chip Select to V_{REN} On	t_{CSOR}	—	—	150	µs	V_{REN} floating
Chip Select to V_{REN} Off	t_{CSPD}	—	—	80	µs	V_{REN} floating

2.5 Thermal Specifications[1]

Parameter	Symbol	Typ.	Max.	Units	Test Conditions
Recovery Temperature	$\theta_{RECOVERY}$	+140	—	°C	
Shutdown Temperature	$\theta_{SHUTDOWN}$	+150	—	°C	
Short-Circuit Recovery Time	t_{THERM}	1.5	5.0	ms	
Thermal Package Resistances					
Thermal Resistance, 8L-DFN	θ_{JA}	35.7	—	°C/W	
Thermal Resistance, 8L-PDIP	θ_{JA}	89.3	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	149.5	—	°C/W	

Note 1: The maximum power dissipation is a function of T_{JMAX}, θ_{JA} and ambient temperature, T_A. The maximum allowable power dissipation at an ambient temperature is $P_D = (T_{JMAX} - T_A) \theta_{JA}$. If this dissipation is exceeded, the die temperature will rise above +150°C and the device will go into thermal shutdown.

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2.6   Typical Performance Curves

> **Note:**   The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{BB} = 6.0V to 18.0V, T_A = -40°C to +125°C.

FIGURE 2-1:   TYPICAL I_{BBQ}
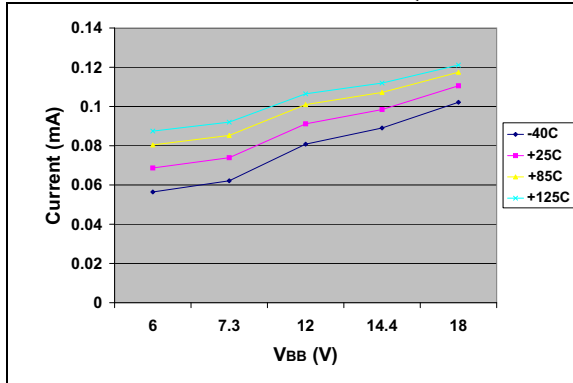
FIGURE 2-3:   TYPICAL I_{BBTO}
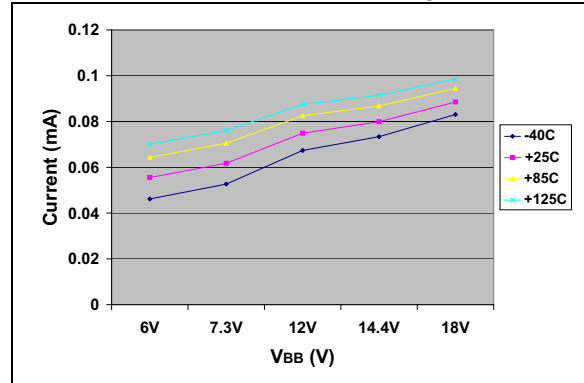
FIGURE 2-2:   TYPICAL I_{BBPD}
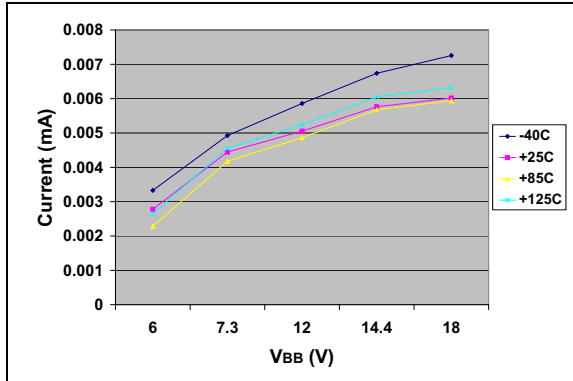
2.7 Timing Diagrams and Specifications

FIGURE 2-4: BUS TIMING DIAGRAM
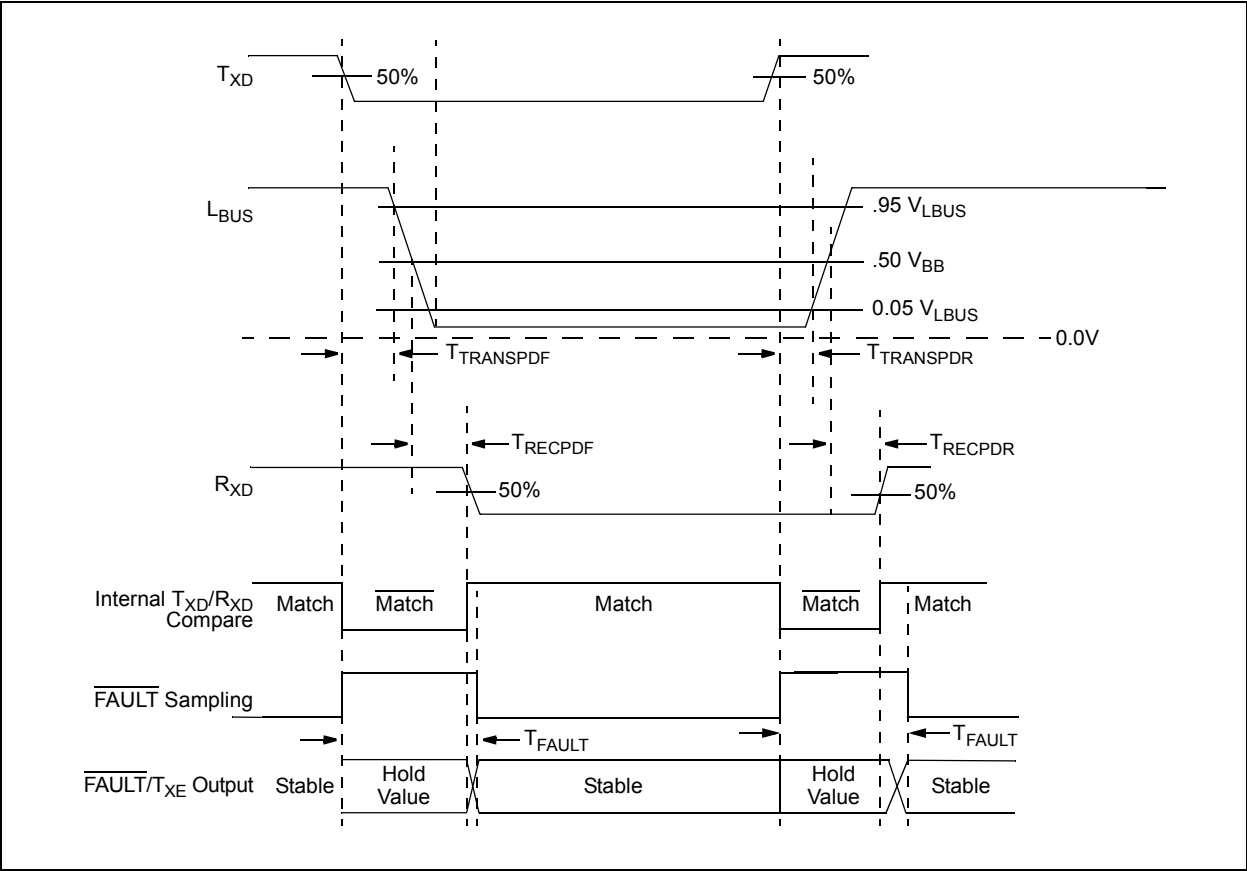
FIGURE 2-5: CS TO V$_{REN}$ TIMING DIAGRAM
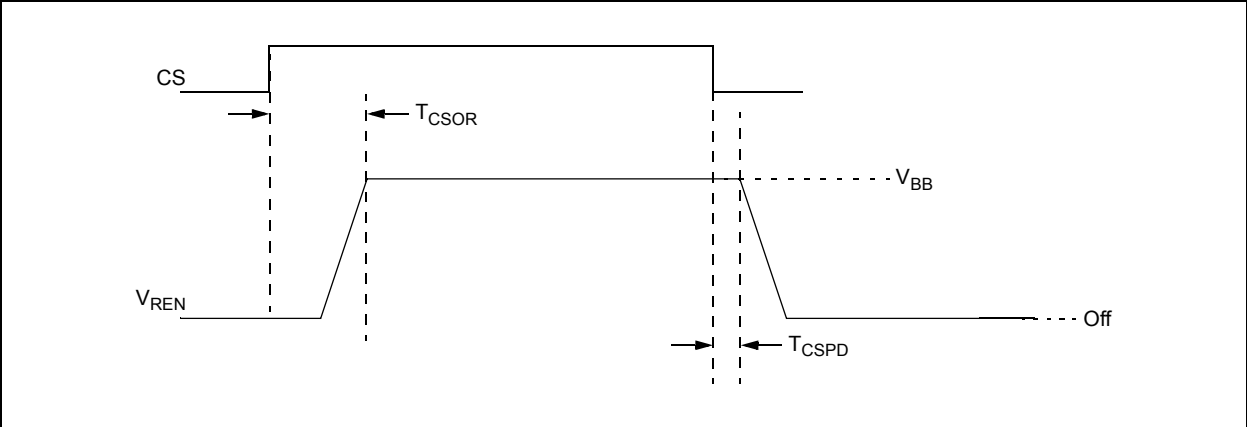
FIGURE 2-6: **MCP2003/4 REMOTE WAKE-UP**
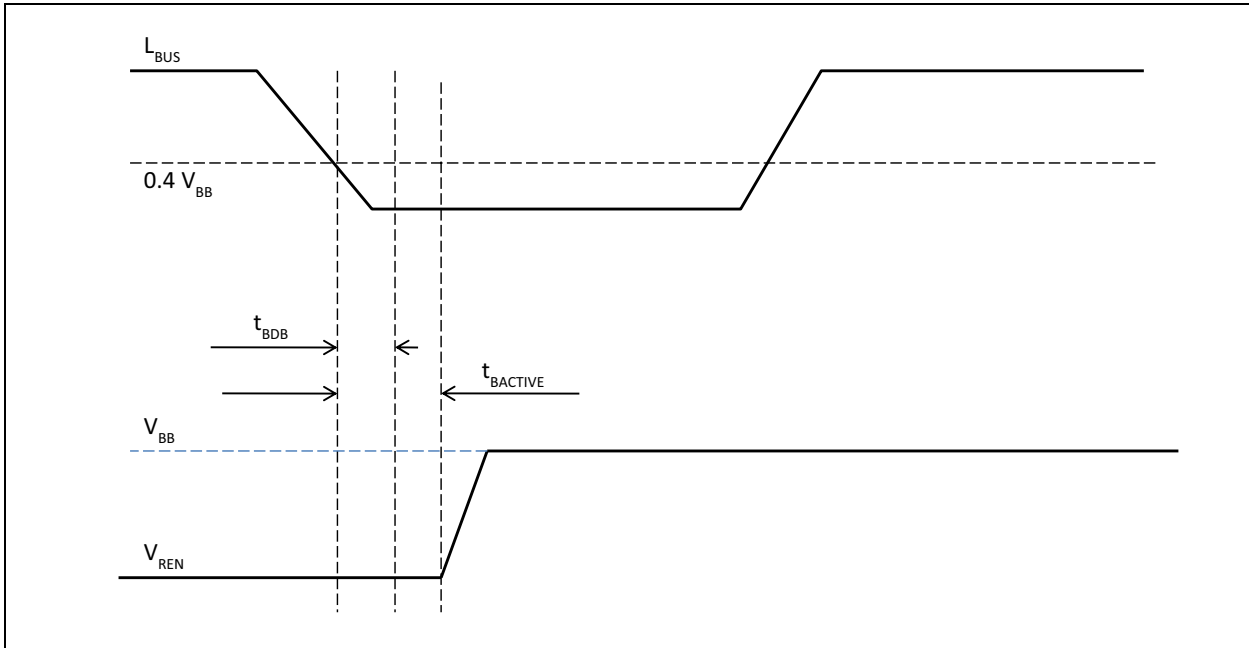
FIGURE 2-7: **MCP2003A/4A REMOTE WAKE-UP**
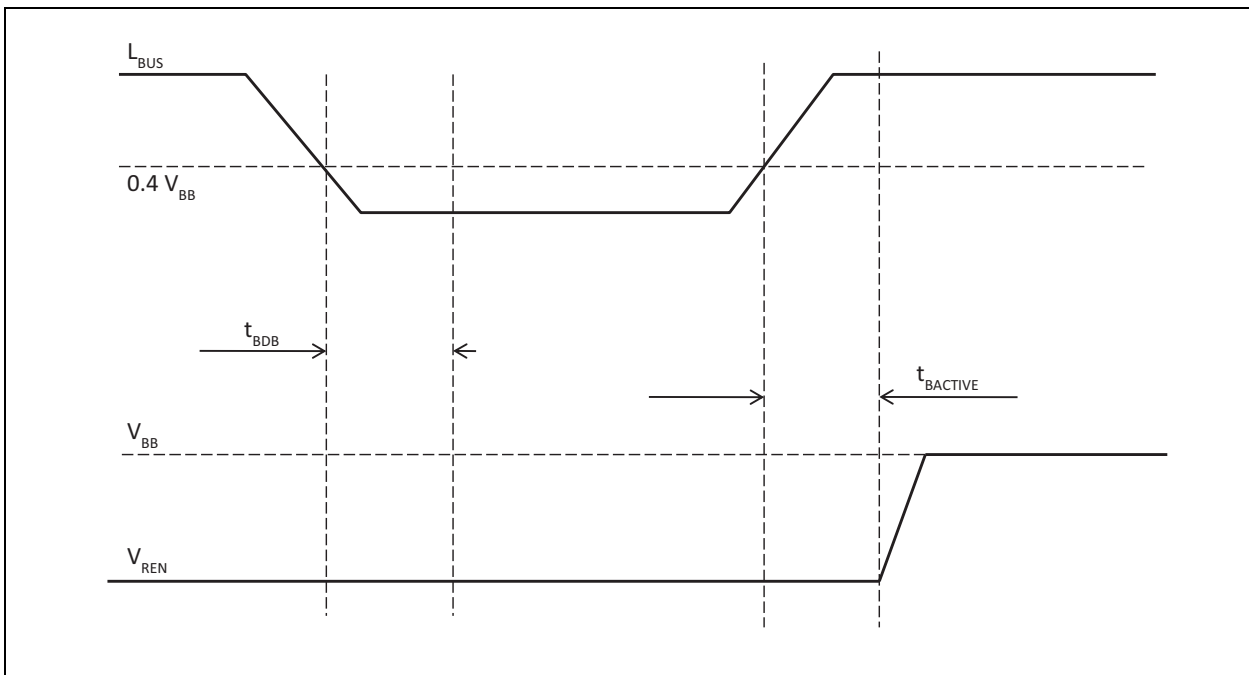
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

8-Lead DFN (4x4x0.9 mm)

XXXXXX
XXXXXX
YYWW
● NNN

PIN 1

Example:

2003
E/MD (e3)
1642
● 256

PIN 1

8-Lead PDIP (300 mil)

XXXXXXXX
XXXXXNNN
○ YYWW

Example:

MCP2003
E/P (e3) 256
○ 1642

8-Lead SOIC (150 mil)

XXXXXXXX
XXXXYYWW
○ NNN

Example:

MCP2003E
SN (e3) 1642
○ 256
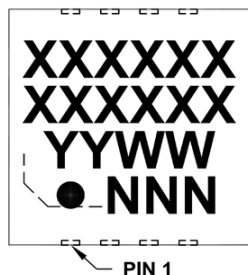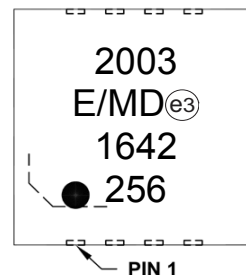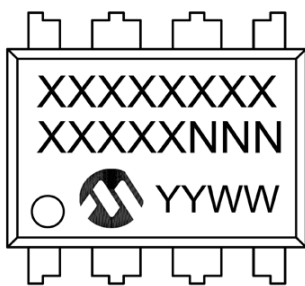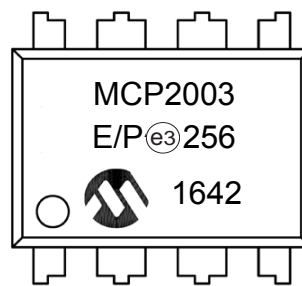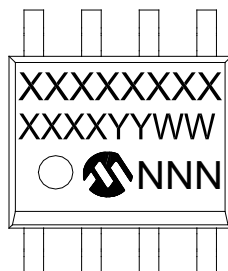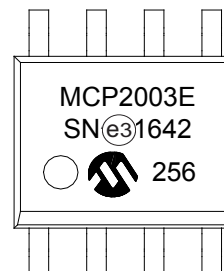
Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

BOTTOM VIEW

Microchip Technology Drawing C04-131E Sheet 1 of 2

8-Lead Plastic Dual Flat, No Lead Package (MD) – 4x4x0.9 mm Body [DFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

NOTE 2
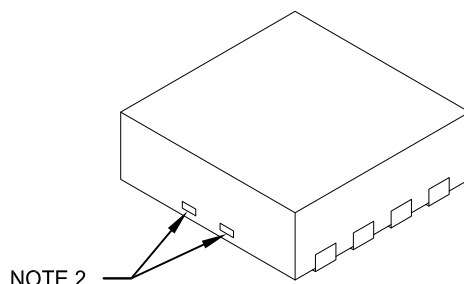
	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.80 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Width	E2	2.60	2.70	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Length	D2	3.40	3.50	3.60
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated
4. Dimensioning and tolerancing per ASME Y14.5M
    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-131E Sheet 2 of 2

8-Lead Plastic Dual Flat, No Lead Package (MD) - 4x4x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
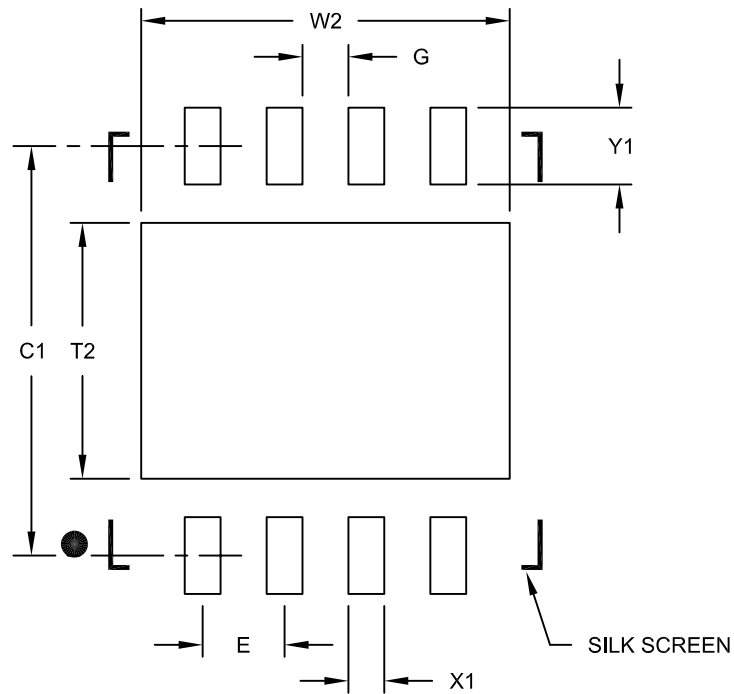
RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.80 BSC		
Optional Center Pad Width	W2			3.60
Optional Center Pad Length	T2			2.50
Contact Pad Spacing	C1		4.00	
Contact Pad Width (X8)	X1			0.35
Contact Pad Length (X8)	Y1			0.75
Distance Between Pads	G	0.45		

Notes:
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2131C

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

D

A

N

B

E1

NOTE 1

1   2

TOP VIEW

C   A

PLANE

A1

A2

L

e

8X b1

8X b

⊕ .010 Ⓜ C

SIDE VIEW

E

c

eB

END VIEW

Microchip Technology Drawing No. C04-018D Sheet 1 of 2

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8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

ALTERNATE LEAD DESIGN
(VENDOR DEPENDENT)

DATUM A

DATUM A

b

$\frac{e}{2}$

e

b

$\frac{e}{2}$

e
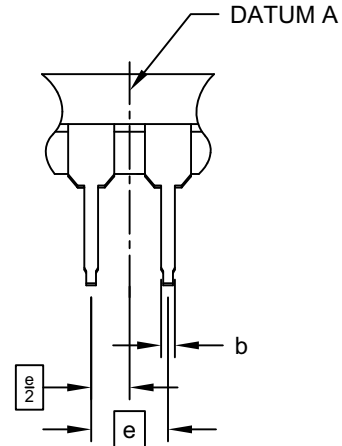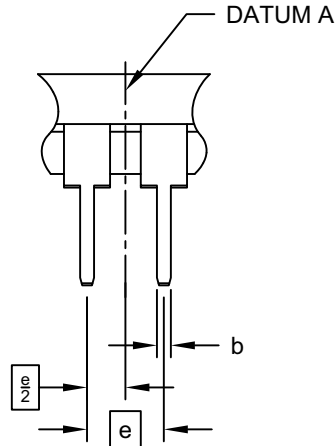
	Units	INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

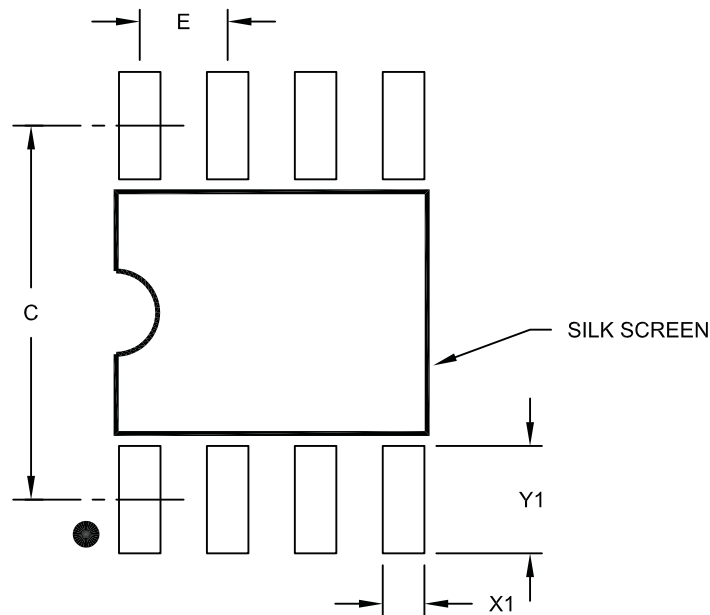   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-018D Sheet 2 of 2

MCP2003/4/3A/4A

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

SIDE VIEW

VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

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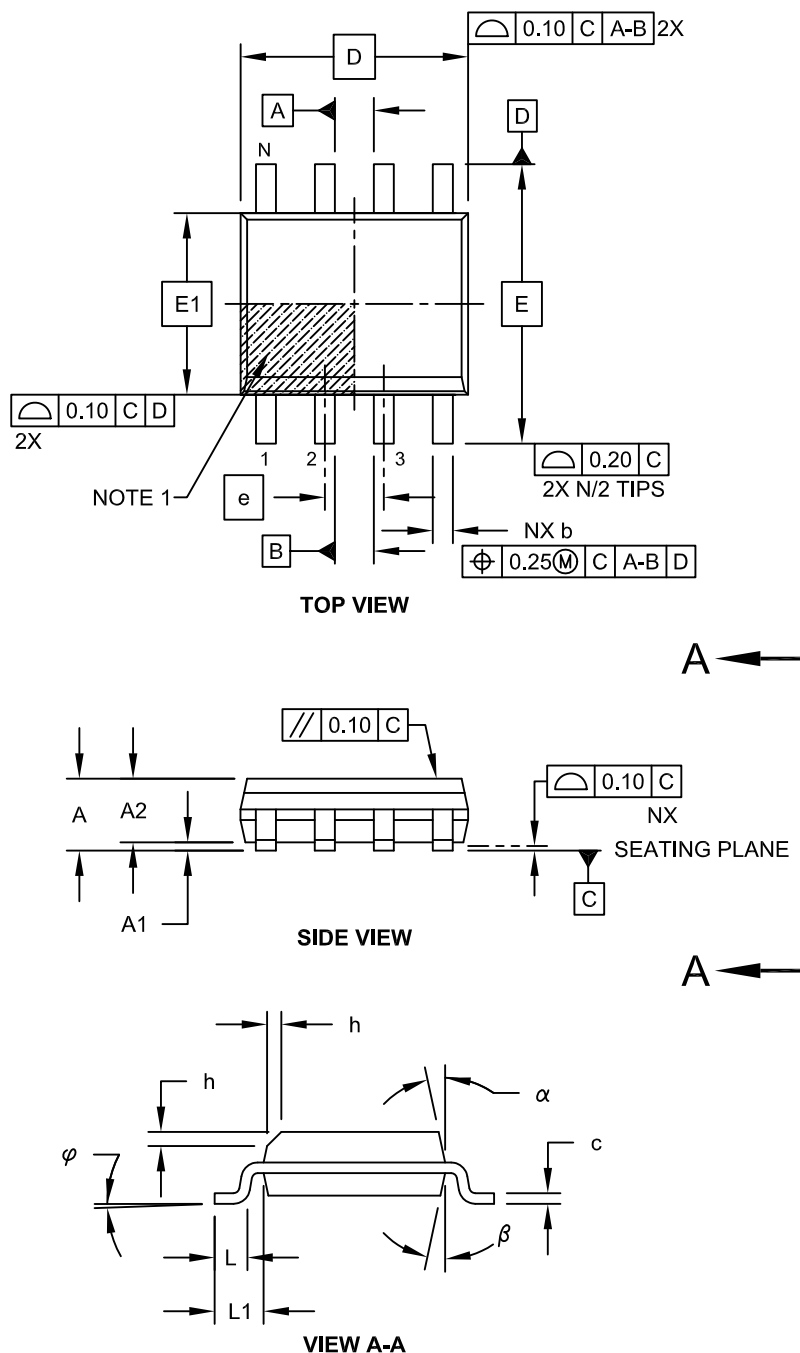
8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
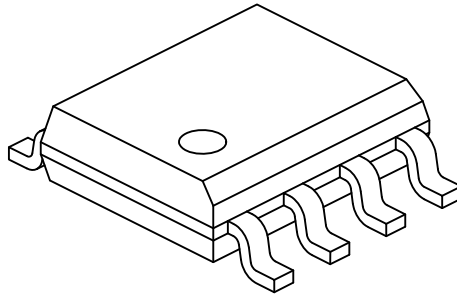
	Units	MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

SILK SCREEN

Y1

X1

RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

APPENDIX A: REVISION HISTORY

Revision G (December 2016)

The following is the list of modifications"

1. Added note to page 1 header: "Not recommended for new designs".
2. Updated **Section 3.1 "Package Marking Information"**.
3. Minor typographical corrections.

Revision F (November 2014)

The following is the list of modifications:

1. Updated typical application circuits with values used during ESD tests.

Revision E (October 2013)

The following is the list of modifications:

1. Added additional specification for I_{HVREN} in **Section 2.3 "DC Specifications"**.
2. Clarified wake-up on L_{BUS} functionality.
3. Added R_{XD} monitoring description.

Revision D (December 2011)

The following is the list of modifications:

1. Added the MCP2003A and MCP2004A devices and related information throughout the document.
2. Updated Figures 1.2, 1.3, 1.4, 1.5, 2.6, 2.7.

Revision C (August 2010)

The following is the list of modifications:

1. Updated all references of Sleep mode to Power-Down mode, and updated the Max. parameter for Duty Cycle 2 in **Section 2.4 "AC Specifications"**.

Revision B (July 2010)

The following is the list of modifications:

1. Added **Section 2.2 "Nomenclature Used in This Document"**, and added the "Capacitance of Slave Node" parameter to **Section 2.3 "DC Specifications"**.

Revision A (March 2010)

• Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX
Device	Temperature Range	Package

Device:

MCP2003: LIN Transceiver with $\overline{\text{WAKE}}$ pins, wake-up on falling edge of L_{BUS}

MCP2003T: LIN Transceiver with $\overline{\text{WAKE}}$ pins, wake-up on falling edge of L_{BUS} (Tape and Reel) (DFN and SOIC only)

MCP2003A: LIN Transceiver with $\overline{\text{WAKE}}$ pins, wake-up on rising edge of L_{BUS}

MCP2003AT: LIN Transceiver with $\overline{\text{WAKE}}$ pins, wake-up on rising edge of L_{BUS} (Tape and Reel) (DFN and SOIC only)

MCP2004: LIN Transceiver with $\overline{\text{FAULT}}/T_{XE}$ pins, wake-up on falling edge of L_{BUS}

MCP2004T: LIN Transceiver with $\overline{\text{FAULT}}/T_{XE}$ pins, wake-up on falling edge of L_{BUS} (Tape and Reel) (DFN and SOIC only)

MCP2004A: LIN Transceiver with $\overline{\text{FAULT}}/T_{XE}$ pins, wake-up on rising edge of L_{BUS}

MCP2004AT: LIN Transceiver with $\overline{\text{FAULT}}/T_{XE}$ pins, wake-up on rising edge of L_{BUS} (Tape and Reel) (DFN and SOIC only)

Temperature Range: E = -40°C to +125°C

Package:
MD = Plastic Dual Flat, No Lead Package – 4x4x0.9mm Body, 8-Lead
P = Plastic Dual In-Line – 300 mil Body, 8-Lead
SN = Plastic Small Outline – Narrow 3.90 mm Body, 8-Lead

Examples:

a) MCP2003A-E/MD: Extended Temperature, 8L-DFN package

b) MCP2003A-E/P: Extended Temperature, 8L-PDIP package

c) MCP2003A-E/SN: Extended Temperature, 8L-SOIC package

d) MCP2003AT-E/MD: Tape and Reel, Extended Temperature, 8L-DFN package

e) MCP2003AT-E/SN: Tape and Reel, Extended Temperature, 8L-SOIC package

a) MCP2004-E/MD: Extended Temperature, 8L-DFN package

b) MCP2004-E/P: Extended Temperature, 8L-PDIP package

c) MCP2004A-E/SN: Extended Temperature, 8L-SOIC package

d) MCP2004AT-E/MD: Tape and Reel, Extended Temperature, 8L-DFN package

e) MCP2004AT-E/SN: Tape and Reel, Extended Temperature, 8L-SOIC package

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.

- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.

- Microchip is willing to work with the customer who is concerned about the integrity of their code.

- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

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