## INTERNAL BLOCK DIAGRAM

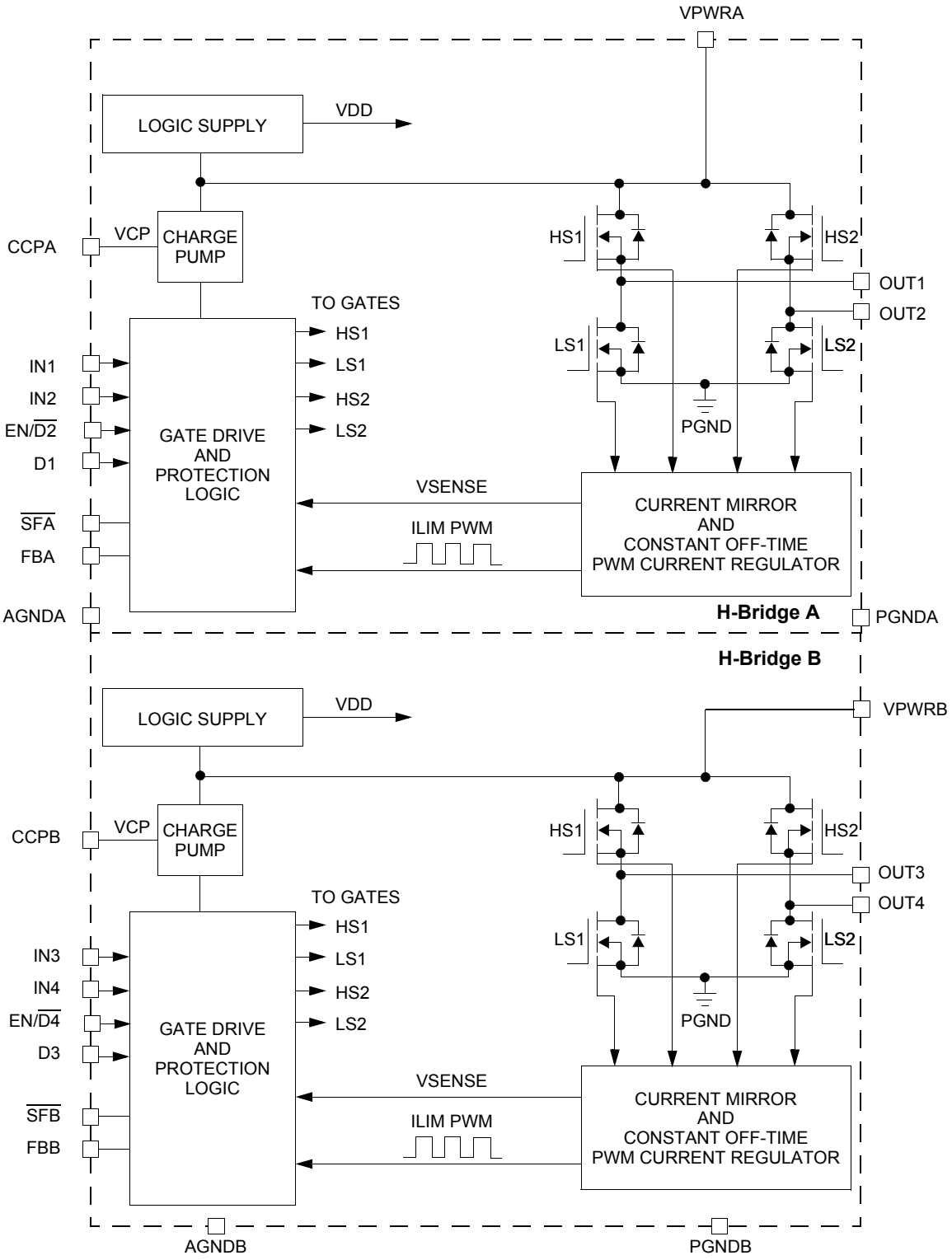
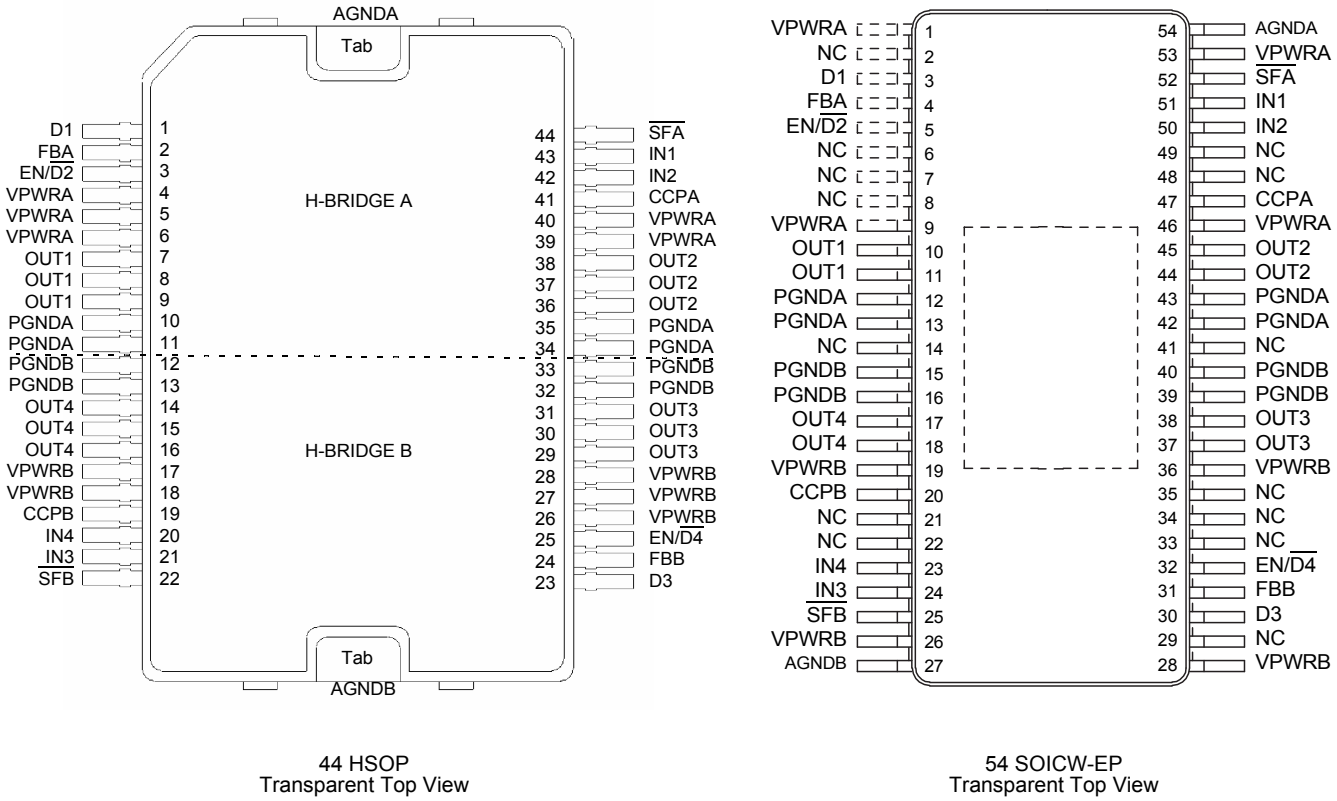



**Figure 2. 33932 Simplified Internal Block Diagram**

# PIN CONNECTIONS




44 HSOP
Transparent Top View

54 SOICW-EP
Transparent Top View

**Figure 3. 33932 Pin Connections**

A functional description of each pin can be found in the Functional Description section beginning on Functional Description.

**Table 1. 33932 Pin Definitions**

| Pin HSOP (VW) | Pin SOICW-EP (EK) | Pin Name | Pin Function | Formal Name | Definition |
|---|---|---|---|---|---|
| 1 | 3 | D1 | Logic Input | Disable Input 1 (Active High) | When D1 is logic HIGH, both OUT1 and OUT2 are tri-stated. Schmitt trigger input with ~80 μA source so default condition = disabled. |
| 2 | 4 | FBA | Analog Output | Feedback | H-Bridge A load current feedback output provides ground referenced 0.24% of the high side output current. (Tie to GND through a resistor if not used.) |
| 3 | 5 | EN/$\overline{D2}$ | Logic Input | Enable Input | When EN/$\overline{D2}$ is logic HIGH, H-Bridge A is operational. When EN/$\overline{D2}$ is logic LOW, the H-Bridge A outputs are tri-stated and H-Bridge A is placed in Sleep Mode. (logic input with ~80 μA sink so default condition = Sleep Mode.) |
| 4-6, 39, 40 | 1, 9, 46, 53 | VPWRA | Power Input | Positive Power Supply | These pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance supply plane on the PCB. |
| 7-9 | 10, 11 | OUT1 | Power Output | H-Bridge Output 1 | H-Bridge A source of HS1 and drain LS1. |

**Table 1. 33932 Pin Definitions (continued)**

| Pin HSOP (VW) | Pin SOICW-EP (EK) | Pin Name | Pin Function | Formal Name | Definition |
|---|---|---|---|---|---|
| 10, 11, 34, 35 | 12, 13, 42, 43 | PGNDA | Power Ground | Power Ground | High-current power ground pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance ground plane on the PCB. PGNDA should be connected to PGNDB with a low-impedance path. |
| 12, 13, 32, 33 | 15, 16, 39, 40 | PGNDB | Power Ground | Power Ground | High-current power ground pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance ground plane on the PCB. PGNDB should be connected to PGNDA with a low-impedance path. |
| 14-16 | 17, 18 | OUT4 | Power Output | H-Bridge Output 4 | H-Bridge B Source of HS2 and drain of LS2. |
| 17, 18, 26-28 | 19, 26, 28, 36 | VPWRB | Power Input | Positive Power Supply | These pins must be connected together physically as close as possible and directly soldered down to a wide, thick, low resistance supply plane on the PCB. |
| 19 | 20 | CCPB | Analog Output | Charge Pump Capacitor | External reservoir capacitor connection for H-Bridge B internal charge pump; connected to VPWRB. Allowable values are 30 to 100 nF. **Note:** This capacitor is required for the proper performance of the device. |
| 20 | 23 | IN4 | Logic Input | Input 4 | Logic input control of OUT4. |
| 21 | 24 | IN3 | Logic Input | Input 3 | Logic input control of OUT3. |
| 22 | 25 | $\overline{SFB}$ | Logic Output - Open Drain | Status Flag B (Active Low) | H-Bridge B open drain active LOW Status Flag output (requires an external pull-up resistor to $V_{DD}$. Maximum permissible load current < 0.5 mA. Maximum $V_{\overline{SF}LOW}$ < 0.4 V at 0.3 mA. Maximum permissible pull-up voltage < 7.0 V.) |
| 23 | 30 | D3 | Logic Input | Disable Input 3 (Active High) | When D3 is logic HIGH, both OUT3 and OUT4 are tri-stated. Schmitt trigger input with ~80 μA source so default condition = disabled. |
| 24 | 31 | FBB | Analog Output | Feedback B | H-Bridge B load current feedback output provides ground referenced 0.24% of the high side output current. (Tie to GND through a resistor if not used.) |
| 25 | 32 | EN/$\overline{D4}$ | Logic Input | Enable Input | When EN/$\overline{D4}$ is logic HIGH, H-Bridge B is operational. When EN/$\overline{D4}$ is logic LOW, the H-Bridge B outputs are tri-stated and H-Bridge B is placed in Sleep Mode. (logic input with ~80μA sink so default condition = Sleep Mode.) |
| 29-31 | 37, 38 | OUT3 | Power Output | H-Bridge Output 3 | H-Bridge B Source of HS1 and drain of LS1. |
| 36-38 | 44, 45 | OUT2 | Power Output | H-Bridge Output 2 | H-Bridge A source of HS2 and drain of LS2. |
| 41 | 47 | CCPA | Analog Output | Charge Pump Capacitor | External reservoir capacitor connection for H-Bridge A internal charge pump; connected to VPWRA. Allowable values are 30 to 100 nF. **Note:** This capacitor is required for the proper performance of the device. |
| 42 | 50 | IN2 | Logic Input | Input 2 | Logic input control of OUT2. |
| 43 | 51 | IN1 | Logic Input | Input 1 | Logic input control of OUT1; e.g., when IN1 is logic HIGH, OUT1 is set to VPWRA, and when IN1 is logic LOW, OUT1 is set to PGNDA. (Schmitt trigger Input with ~80 μA source so default condition = OUT1 HIGH.) |

**Table 1. 33932 Pin Definitions (continued)**

| Pin HSOP (VW) | Pin SOICW-EP (EK) | Pin Name | Pin Function | Formal Name | Definition |
|---|---|---|---|---|---|
| 44 | 52 | $\overline{SFA}$ | Logic Output - Open Drain | Status Flag (Active Low) | H-Bridge A open drain active LOW Status Flag output (requires an external pull-up resistor to $V_{DD}$. Maximum permissible load current < 0.5 mA. Maximum $V_{\overline{SF}LOW}$< 0.4 V at 0.3 mA. Maximum permissible pull-up voltage < 7.0 V.) |
| TAB | 54<br>27 | AGNDA<br>AGNDB | Analog Ground | Analog Signal Ground | The low-current analog signal ground must be connected to PGND via low-impedance path (<10 mΩ, 0 Hz to 20 kHz). |
| — | 2, 6 - 8, 14, 21, 22, 29, 33 - 35, 41, 48, 49 | NC | None | No Connect | These pins have no electrical connection or function. |
| — | EP | EP | Thermal Pad | Exposed Pad | Exposed TAB is also the main heatsinking path for the device and must be connected to ground. |

# ELECTRICAL CHARACTERISTICS

## MAXIMUM RATINGS

**Table 2. Maximum Ratings**

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device. These parameters are not production tested.

| Ratings | Symbol | Value | Unit |
|---|---|---|---|
| **ELECTRICAL RATINGS** | | | |
| Power Supply Voltage | | | V |
| Normal Operation (Steady-state) | $V_{PWR(SS)}$ | -0.3 to 28 | |
| Transient Over-voltage(1) | $V_{PWR(T)}$ | -0.3 to 40 | |
| Logic Input Voltage(2) | $V_{IN}$ | -0.3 to 7.0 | V |
| $\overline{SFA}$, $\overline{SFB}$ Output(3) | $V_{\overline{SF}}$ | -0.3 to 7.0 | V |
| Continuous Output Current(4) | $I_{OUT(CONT)}$ | 5.0 | A |
| ESD Voltage(5) | | | V |
| Human Body Model | $V_{ESD1}$ | ±2000 | |
| Machine Model | $V_{ESD2}$ | ±200 | |
| Charge Device Model | | | |
| Corner Pins | | ±750 | |
| All Other Pins | | ±500 | |
| **THERMAL RATINGS** | | | |
| Storage Temperature | $T_{STG}$ | -65 to 150 | °C |
| Operating Temperature(6) | | | °C |
| Ambient | $T_A$ | -40 to 125 | |
| Junction | $T_J$ | -40 to 150 | |
| Peak Package Reflow Temperature During Reflow(7), (8) | $T_{PPRT}$ | Note 8 | °C |
| Approximate Junction-to Case Thermal Resistance(9) | $R_{THJC}$ | <1.0 | °C/W |

Notes

1. Device will survive repetitive transient over-voltage conditions for durations not to exceed 500 ms at duty cycle not to exceed 10%. External protection is required to prevent device damage in case of a reverse battery condition.
2. Exceeding the maximum input voltage on IN1, IN2, IN3, IN4, EN/$\overline{D2}$, EN/$\overline{D4}$, D1, or D3 may cause a malfunction or permanent damage to the device.
3. Exceeding the pull-up resistor voltage on the open drain $\overline{SFA}$ or $\overline{SFB}$ pin may cause permanent damage to the device.
4. Continuous output current capability is dependent on sufficient package heatsinking to keep junction temperature ≤150 °C.
5. ESD testing is performed in accordance with the Human Body Model ($C_{ZAP}$ = 100 pF, $R_{ZAP}$ = 1500 Ω), Machine Model ($C_{ZAP}$ = 200 pF, $R_{ZAP}$ = 0 Ω), and the Charge Device Model (CDM), Robotic ($C_{ZAP}$ = 4.0 pF).
6. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking provided. Brief non-repetitive excursions of junction temperature above 150 °C can be tolerated, provided the duration does not exceed 30 seconds maximum. (Non-repetitive events are defined as not occurring more than once in 24 hours.)
7. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
8. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.
9. Exposed heatsink pad plus the power and ground pins comprise the main heat conduction paths. The actual $R_{\theta JB}$ (junction-to-PC board) values will vary depending on solder thickness and composition and copper trace thickness and area. Maximum current at maximum die temperature represents ~16 W of conduction loss heating in the diagonal pair of output MOSFETs. Therefore, the $R_{\theta JA}$ must be <5.0 °C/W for maximum current at 70 °C ambient. Module thermal design must be planned accordingly.

## STATIC ELECTRICAL CHARACTERISTICS

**Table 3. Static Electrical Characteristics**

Characteristics noted under conditions 5.0 V ≤ $V_{PWR}$ ≤ 28 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted. Specifications given for H-Bridge A apply symmetrically to H-Bridge B.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **POWER INPUTS (VPWR)** | | | | | |
| Operating Voltage Range[10] | | | | | V |
| Steady-state | $V_{PWR(SS)}$ | 5.0 | – | 28 | |
| Transient (t < 500 ms)[11] | $V_{PWR(t)}$ | – | – | 40 | |
| Sleep State Supply Current[12] | $I_{PWR(SLEEP)}$ | | | | µA |
| EN/$\overline{D2}$ = Logic [0], IN1, IN2, D1 = Logic [1], and $I_{OUT}$ = 0 A | | – | – | 50 | |
| Standby Supply Current (Part Enabled) | $I_{PWR(STANDBY)}$ | | | | mA |
| $I_{OUT}$ = 0 A, $V_{EN}$ = 5.0 V | | – | – | 20 | |
| Under-voltage Lockout Thresholds | | | | | |
| $V_{PWR(FALLING)}$ | $V_{UVLO(ACTIVE)}$ | 4.15 | – | – | V |
| $V_{PWR(RISING)}$ | $V_{UVLO(INACTIVE)}$ | – | – | 5.0 | V |
| Hysteresis | $V_{UVLO(HYS)}$ | 150 | 200 | 350 | mV |
| **CHARGE PUMP** | | | | | |
| Charge Pump Voltage (CP Capacitor = 33 nF), No PWM | $V_{CP}$ - $V_{PWR}$ | | | | V |
| $V_{PWR}$ = 5.0 V | | 3.5 | – | – | |
| $V_{PWR}$ = 28 V | | – | – | 12 | |
| Charge Pump Voltage (CP Capacitor = 33 nF), PWM = 11 kHz | $V_{CP}$ - $V_{PWR}$ | | | | V |
| $V_{PWR}$ = 5.0 V | | 3.5 | – | – | |
| $V_{PWR}$ = 28 V | | – | – | 12 | |
| **CONTROL INPUTS** | | | | | |
| Operating Input Voltage (IN1, IN2, D1, EN/$\overline{D2}$, IN3, IN4, D3, EN/$\overline{D4}$) | $V_I$ | – | – | 5.5 | V |
| Input Voltage (IN1, IN2, D1, EN/$\overline{D2}$, IN3, IN4, D3, EN/$\overline{D4}$) | | | | | |
| Logic Threshold HIGH | $V_{IH}$ | 2.0 | – | – | V |
| Logic Threshold LOW | $V_{IL}$ | – | – | 1.0 | V |
| Hysteresis | $V_{HYS}$ | 250 | 400 | – | mV |
| Logic Input Currents, VPWR = 8.0 V | $I_{IN}$ | | | | µA |
| Input EN/$\overline{D2}$, EN/$\overline{D4}$ (internal pull-downs), $V_{IH}$ = 5.0 V | | 20 | 80 | 200 | |
| Inputs IN1, IN2, D1, IN3, IN4, D3 (internal pull-ups), VIL = 0 V | | -200 | -80 | -20 | |

Notes

10. Device specifications are characterized over the range of 8.0 V ≤ $V_{PWR}$ ≤ 28 V. Continuous operation above 28 V may degrade device reliability. Device is operational down to 5.0V, but below 8.0 V the output resistance may increase by 50 percent.
11. Device will survive the transient over-voltage indicated for a maximum duration of 500 ms. Transient not to be repeated more than once every 10 seconds.
12. $I_{PWR(SLEEP)}$ is with Sleep Mode activated and EN/ $\overline{D2}$, = logic [0], and IN1, IN2, D1 = logic [1] or with these inputs left floating.

**Table 3. Static Electrical Characteristics (continued)**

Characteristics noted under conditions 5.0 V ≤ $V_{PWR}$ ≤ 28 V, -40 °C ≤ $T_A$ ≤ 125 °C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25 °C under nominal conditions, unless otherwise noted. Specifications given for H-Bridge A apply symmetrically to H-Bridge B.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **POWER OUTPUTS OUT1, OUT2** | | | | | |
| Output-ON Resistance[14], $I_{LOAD}$ = 3.0 A | $R_{DS(ON)}$ | | | | mΩ |
| $V_{PWR}$ = 8.0 V, $T_J$ = 25 °C | | – | 120 | – | |
| $V_{PWR}$ = 8.0 V, $T_J$ = 150 °C | | – | – | 235 | |
| $V_{PWR}$ = 5.0 V, $T_J$ = 150 °C | | – | – | 325 | |
| Output Current Regulation Threshold | $I_{LIM}$ | | | | A |
| $T_J$ < $T_{FB}$ | | 5.2 | 6.5 | 8.0 | |
| $T_J$ ≥ $T_{FB}$ (Fold back Region - see Figure 9 and Figure 11)[13] | | – | 4.2 | – | |
| High Side Short-circuit Detection Threshold (Short-circuit to Ground)[13] | $I_{SCH}$ | 11 | 13 | 16 | A |
| Low Side Short-circuit Detection Threshold (Short-circuit to $V_{PWR}$)[13] | $I_{SCL}$ | 9.0 | 11 | 14 | A |
| Output Leakage Current[15], Outputs off, $V_{PWR}$ = 28 V | $I_{OUTLEAK}$ | | | | μA |
| $V_{OUT}$ = $V_{PWR}$ | | – | – | 100 | |
| $V_{OUT}$ = Ground | | -60 | – | – | |
| Output MOSFET Body Diode Forward Voltage Drop, $I_{OUT}$ = 3.0 A | $V_F$ | – | – | 2.0 | V |
| Over-temperature Shutdown[13] | | | | | °C |
| Thermal Limit at $T_J$ | $T_{LIM}$ | 175 | – | 200 | |
| Hysteresis at $T_J$ | $T_{HYS}$ | – | 12 | – | |
| Current Foldback at $T_J$[13] | $T_{FB}$ | 165 | – | 185 | °C |
| Current Foldback to Thermal Shutdown Separation[13] | $T_{SEP}$ | 10 | – | 15 | °C |
| **HIGH SIDE CURRENT SENSE FEEDBACK** | | | | | |
| Feedback Current (pin FB sourcing current)[16] | $I_{FB}$ | | | | |
| $I_{OUT}$ = 0.0 mA | | 0.0 | – | 50 | μA |
| $I_{OUT}$ = 300 mA | | 0.0 | 270 | 750 | μA |
| $I_{OUT}$ = 500 mA | | 0.35 | 0.775 | 1.56 | mA |
| $I_{OUT}$ = 1.5 A | | 2.86 | 3.57 | 4.28 | mA |
| $I_{OUT}$ = 3.0 A | | 5.71 | 7.14 | 8.57 | mA |
| $I_{OUT}$ = 6.0 A | | 11.43 | 14.29 | 17.15 | mA |
| **STATUS FLAG**[17] | | | | | |
| Status Flag Leakage Current[18] | $I_{\overline{SF}LEAK}$ | | | | μA |
| $V_{\overline{SF}}$ = 5.0 V | | – | – | 5.0 | |
| Status Flag SET Voltage[19] | $V_{\overline{SF}LOW}$ | | | | V |
| $I_{\overline{SF}}$ = 300 μA | | – | – | 0.4 | |

Notes

13. This parameter is Guaranteed By Design.
14. Output-ON resistance as measured from output to VPWR and from output to GND.
15. Outputs switched OFF via D1 or EN/$\overline{D2}$.
16. Accuracy is better than 20% from 0.5 A to 6.0 A. Recommended terminating resistor value: $R_{FB}$ = 270 Ω.
17. Status Flag output is an open drain output requiring a pull-up resistor to logic $V_{DD}$.
18. Status Flag Leakage Current is measured with Status Flag HIGH and *not* SET.
19. Status Flag Set Voltage measured with Status Flag LOW and SET with $I_{\overline{SF}}$ = 300 μA. Maximum allowable sink current from this pin is < 500 μA. Maximum allowable pull-up voltage < 7.0 V.

## DYNAMIC ELECTRICAL CHARACTERISTICS

**Table 4. Dynamic Electrical Characteristics**

Characteristics noted under conditions 5.0 V ≤ $V_{PWR}$ ≤ 28 V, -40°C ≤ $T_A$ ≤ 125°C, GND = 0 V, unless otherwise noted. Typical values noted reflect the approximate parameter means at $T_A$ = 25°C under nominal conditions, unless otherwise noted.

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **TIMING CHARACTERISTICS** | | | | | |
| PWM Frequency[20] | $f_{PWM}$ | – | – | 11 | kHz |
| Maximum Switching Frequency During Current Limit Regulation[21] | $f_{MAX}$ | – | – | 20 | kHz |
| Output ON Delay[22]<br>$V_{PWR}$ = 14 V | $t_{DON}$ | – | – | 18 | µs |
| Output OFF Delay[22]<br>$V_{PWR}$ = 14 V | $t_{DOFF}$ | – | – | 12 | µs |
| $I_{LIM}$ Output Constant-OFF Time[23] [25] | $t_A$ | 15 | 20.5 | 32 | µs |
| $I_{LIM}$ Blanking Time[24] [25] | $t_B$ | 12 | 16.5 | 27 | µs |
| Disable Delay Time[26] | $t_{DDISABLE}$ | – | – | 8.0 | µs |
| Output Rise and Fall Time[27] | $t_F$, $t_R$ | 1.5 | 3.0 | 8.0 | µs |
| Short-circuit/Over-temperature Turn-OFF (Latch-OFF) Time[28], [29] | $t_{FAULT}$ | – | – | 8.0 | µs |
| Power-ON Delay Time[29] | $t_{POD}$ | – | 1.0 | 5.0 | ms |
| Output MOSFET Body Diode Reverse Recovery Time[29] | $t_{RR}$ | 75 | 100 | 150 | ns |
| Charge Pump Operating Frequency[29] | $f_{CP}$ | – | 7.0 | – | MHz |

Notes

20. The maximum PWM frequency should be limited to frequencies < 11 kHz in order to allow the internal high side driver circuitry time to fully enhance the high side MOSFETs.
21. The internal current limit circuitry produces a constant-OFF-time Pulse Width Modulation of the output current. The output load's inductance, capacitance, and resistance characteristics affect the total switching period (OFF-time + ON-time), and thus the PWM frequency during current limit.
22. * Output Delay is the time duration from 1.5 V on the IN1 or IN2 input signal to the 20% or 80% point (dependent on the transition direction) of the OUT1 or OUT2 signal. If the output is transitioning HIGH-to-LOW, the delay is from 1.5 V on the input signal to the 80% point of the output response signal. If the output is transitioning LOW-to-HIGH, the delay is from 1.5 V on the input signal to the 20% point of the output response signal. See Figure 4, page 10.
23. The time during which the internal constant-OFF time PWM current regulation circuit has tri-stated the output bridge.
24. The time during which the current regulation threshold is ignored so that the short-circuit detection threshold comparators may have time to act.
25. Parameter guaranteed by characterization.
26. * Disable Delay Time measurement is defined in Figure 5, page 10.
27. Rise Time is from the 10% to the 90% level and Fall Time is from the 90% to the 10% level of the output signal with $V_{PWR}$ = 14 V, $R_{LOAD}$ = 3.0 ohm. See Figure 6, page 10.
28. Load currents ramping up to the current regulation threshold become limited at the $I_{LIM}$ value (see Figure 7). The short-circuit currents possess a di/dt that ramps up to the $I_{SCH}$ or $I_{SCL}$ threshold during the $I_{LIM}$ blanking time, registering as a short-circuit event detection and causing the shutdown circuitry to force the output into an immediate tri-state latch-OFF (see Figure 8). Operation in Current Limit mode may cause junction temperatures to rise. Junction temperatures above ~160 °C will cause the output current limit threshold to "fold back", or decrease, until ~175 °C is reached, after which the $t_{LIM}$ thermal latch-OFF will occur. Permissible operation within this fold back region is limited to non-repetitive transient events of duration not to exceed 30 seconds (see Figure 9).
29. Parameter is Guaranteed By Design.

## TIMING DIAGRAMS

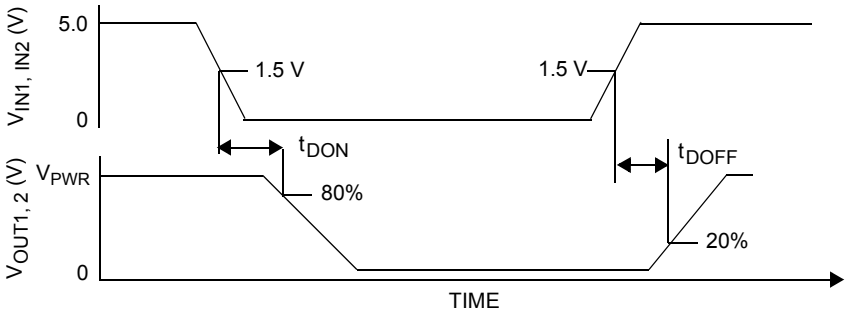



**Figure 4. Output Delay Time**

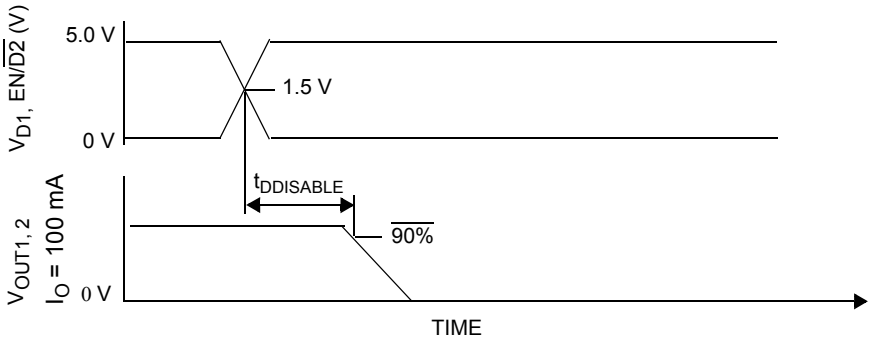



**Figure 5. Disable Delay Time**

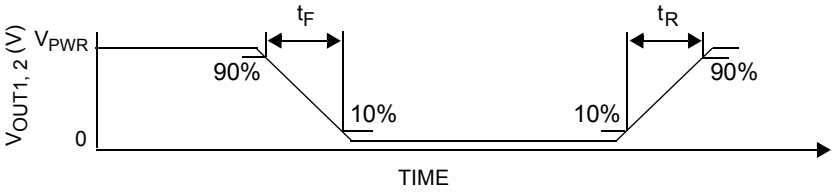



**Figure 6. Output Switching Time**

**Overload Condition**

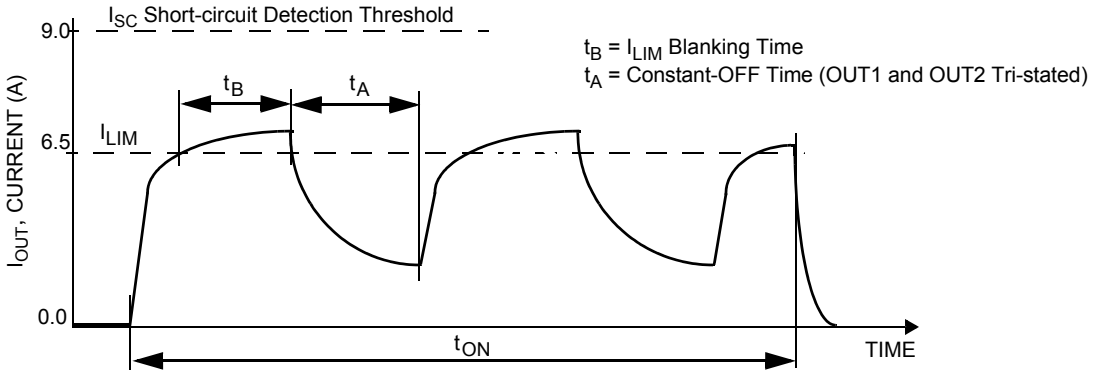



**Figure 7. Current Limit Blanking Time and Constant-OFF Time**

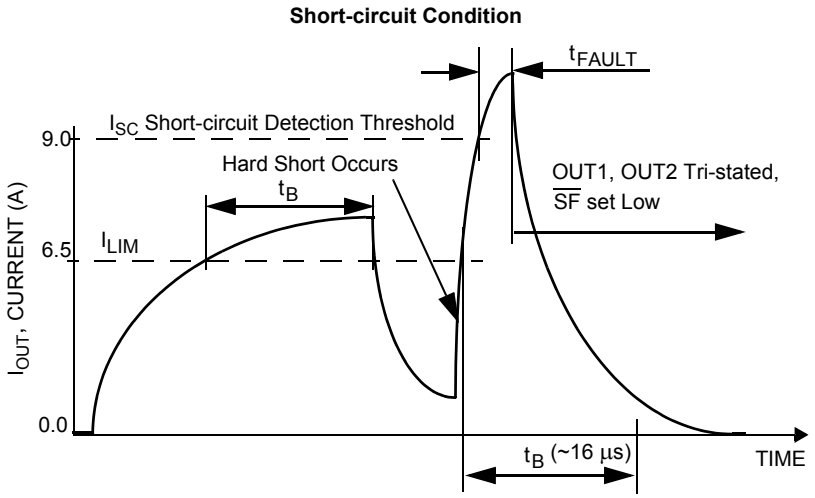



**Figure 8. Short-circuit Detection Turn-OFF Time $t_{FAULT}$**

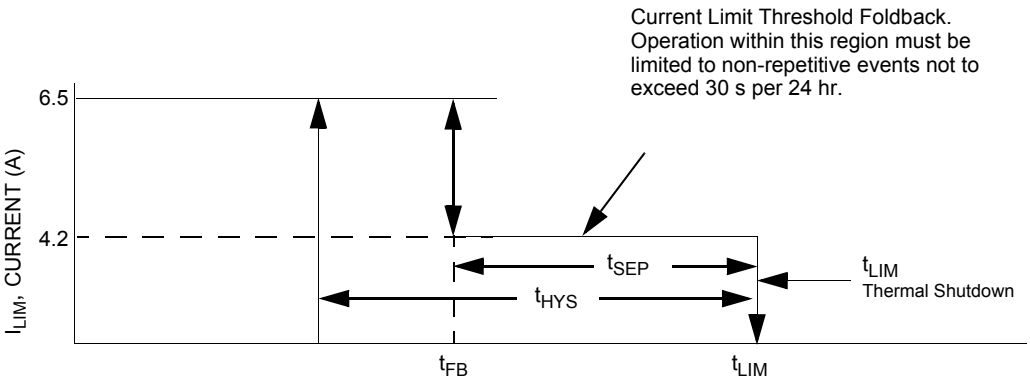



**Figure 9. Output Current Limiting Foldback Region**

# FUNCTIONAL DESCRIPTION

## INTRODUCTION

The 33932 has two identical H-Bridge drivers in the same package. The only connection that is shared internally is the Analog Ground (AGND). This description is given for the H-Bridge A half of the total device. However, the H-Bridge B half will exhibit identical behavior.

Numerous protection and operational features (speed, torque, direction, dynamic breaking, PWM control, and closed-loop control) make the 33932 a very attractive, cost-effective solution for controlling a broad range of small DC motors. The 33932 outputs are capable of supporting peak DC load currents of up to 5.0 A from a 28 V $V_{PWR}$ source. An internal charge pump and gate drive circuitry are provided that can support external PWM frequencies up to 11 kHz.

The 33932 has an analog feedback (current mirror) output pin (the FB pin) that provides a constant-current source ratioed to the active high side MOSFETs' current. This can be used to provide "real time" monitoring of output current to facilitate closed-loop operation for motor speed/torque control, or for the detection of open load conditions.

Two independent inputs, IN1 and IN2, provide control of the two totem-pole half-bridge outputs. Two independent disable inputs, D1 and EN/$\overline{D2}$, provide the means to force the H-bridge outputs to a high-impedance state (all H-bridge switches OFF). The EN/$\overline{D2}$ pin also controls an enable function that allows the IC to be placed in a power-conserving Sleep mode.

The 33932 has output current limiting (via constant OFF-time PWM current regulation), output short-circuit detection with latch-OFF, and over-temperature detection with latch-OFF. Once the device is latched-OFF due to a fault condition, either of the disable inputs (D1 or EN/$\overline{D2}$), or $V_{PWR}$ must be "toggled" to clear the status flag.

Current limiting (Load Current Regulation) is accomplished by a constant-OFF time PWM method using current limit threshold triggering. The current limiting scheme is unique in that it incorporates a junction temperature-dependent current limit threshold. This means that the current limit threshold is "reduced to around 4.2 A" as the junction temperature increases above 160 °C. When the temperature is above 175 °C, over-temperature shutdown (latch-OFF) will occur. This combination of features allows the device to continue operating for short periods of time (<30 seconds) with unexpected loads, while still retaining adequate protection for both the device and the load.

## FUNCTIONAL PIN DESCRIPTION

### POWER GROUND AND ANALOG GROUND (PGND AND AGND)

The power and analog ground pins should be connected together with a very low-impedance connection.

### POSITIVE POWER SUPPLY (VPWR)

VPWR pins are the power supply inputs to the device. All VPWR pins must be connected together on the printed circuit board with as short as possible traces, offering as low an impedance as possible between pins.

### STATUS FLAG ($\overline{SF}$)

This pin is the device fault status output. This output is an active LOW open drain structure requiring a pull-up resistor to $V_{DD}$. The maximum $V_{DD}$ is <7.0 V. Refer to Table 5, Truth Table, for the $\overline{SF}$ Output status definition.

### INPUT 1,2 AND DISABLE INPUT 1 (IN1, IN2, AND D1)

These pins are input control pins used to control the outputs. These pins are 3.0 V/5.0 V CMOS-compatible inputs with hysteresis. IN1 and IN2 independently control OUT1 and OUT2, respectively. D1 input is used to tri-state disable the H-Bridge outputs.

When D1 is SET (D1 = logic HIGH) in the disable state, outputs OUT1 and OUT2 are both tri-state disabled; however, the rest of the device circuitry is fully operational and the supply $I_{PWR(STANDBY)}$ current is reduced to a few mA. Refer to Table 3, Static Electrical Characteristics.

### H-BRIDGE OUTPUT (OUT1, OUT2)

These pins are the outputs of the H-bridge with integrated free-wheeling diodes. The bridge output is controlled using the IN1, IN2, D1, and EN/$\overline{D2}$ inputs. The outputs have PWM current limiting above the $I_{LIM}$ threshold. The outputs also have thermal shutdown (tri-state latch-OFF) with hysteresis as well as short circuit latch-OFF protection.

A disable timer (time $t_B$) is incorporated to distinguish between load currents that are higher than the $I_{LIM}$ threshold and short circuit currents. This timer is activated at each output transition.

### CHARGE PUMP CAPACITOR (CCP)

This pin is the charge pump output pin and connection for the external charge pump reservoir capacitor. The allowable value is from 30 to 100 nF. This capacitor must be connected from the CCP pin to the VPWR pin. The device cannot operate properly without the external reservoir capacitor.

### ENABLE INPUT/DISABLE INPUT 2 (EN/$\overline{D2}$)

The EN/$\overline{D2}$ pin performs the same function as D1 pin, when it goes to a logic LOW the outputs are immediately tri-stated. It is also used to place the device in a Sleep mode so as to consume very low currents. When the EN/$\overline{D2}$ pin voltage is a logic LOW state, the device is in the Sleep mode. The device is enabled and fully operational when the EN pin voltage is logic HIGH. An internal pull-down resistor maintains the device in Sleep mode in the event EN is driven through a high-impedance I/O or an unpowered microcontroller, or the EN/$\overline{D2}$ input becomes disconnected.

### FEEDBACK (FB)

The 33932 has a feedback output (FB) for “real time” monitoring of H-Bridge high side output currents to facilitate closed-loop operation for motor speed and torque control.

The FB pin provides current sensing feedback of the H-Bridge high side drivers. When running in the forward or reverse direction, a ground-referenced 0.24% of load current is output to this pin. Through the use of an external resistor to ground, the proportional feedback current can be converted to a proportional voltage equivalent and the controlling microcontroller can “read” the current proportional voltage with its analog-to-digital converter (ADC). This is intended to provide the user with only first-order motor current feedback for motor torque control. The resistance range for the linear operation of the FB pin is 100 Ω <$R_{FB}$ <300 Ω.

If PWM-ing is implemented using the disable pin input (only D1), a small filter capacitor (~1.0 µF) may be required in parallel with the $R_{FB}$ resistor to ground for spike suppression

## FUNCTIONAL INTERNAL BLOCK DESCRIPTION

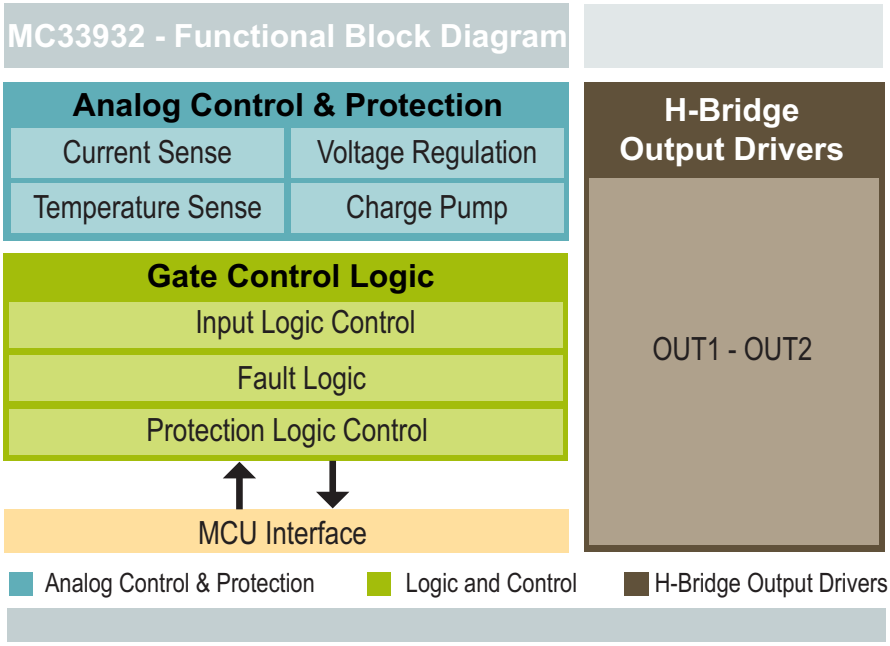



**Figure 10. Functional Internal Block Diagram**

### ANALOG CONTROL AND PROTECTION CIRCUITRY:

An on-chip voltage regulator supplies the internal logic. The charge pump provides gate drive for the H-Bridge MOSFETs. The Current and Temperature sense circuitry provides detection and protection for the output drivers. Output under-voltage protection shuts down the MOSFETS.

### GATE CONTROL LOGIC:

The 33932 is a monolithic H-Bridge Power IC designed primarily for any low-voltage DC servo motor control application within the current and voltage limits stated for the device. Two independent inputs provide polarity control of two half-bridge totem-pole outputs. Two independent disable inputs are provided to force the H-Bridge outputs to tri-state (high-impedance off-state).

### H-BRIDGE OUTPUT DRIVERS: OUT1 AND OUT2

The H-Bridge is the power output stage. The current flow from OUT1 to OUT2 is reversible and under full control of the user by way of the Input Control Logic. The output stage is designed to produce full load control under all system conditions. All protective and control features are integrated into the control and protection blocks. The sensors for current and temperature are integrated directly into the output MOSFET for maximum accuracy and dependability.

# FUNCTIONAL DEVICE OPERATION

## OPERATIONAL MODES

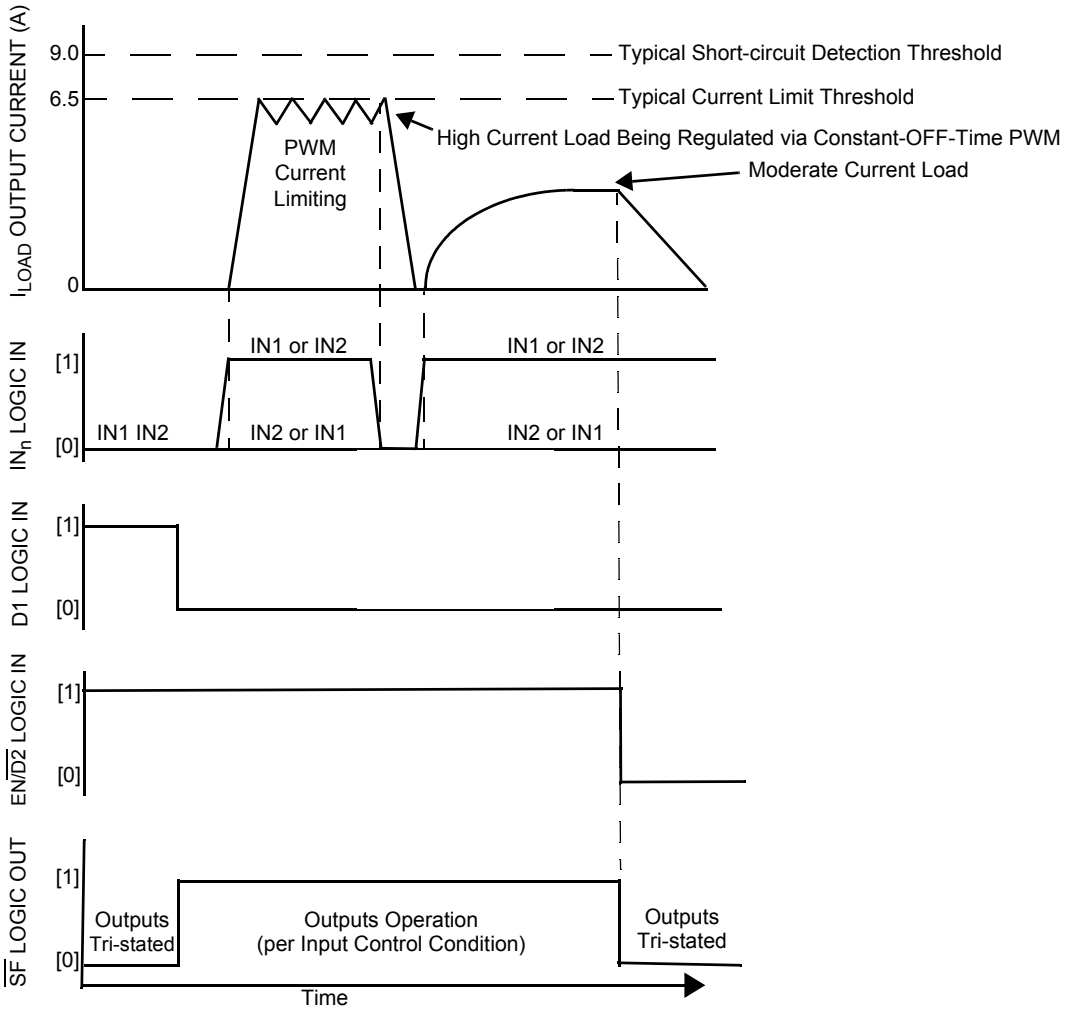



**Figure 11. Operating States**

## LOGIC COMMANDS

**Table 5. Truth Table**

The tri-state conditions and the status flag are reset using D1 or $\overline{D2}$. The truth table uses the following notations: L = LOW, H = HIGH, X = HIGH or LOW, and Z = High-impedance. All output power transistors are switched off.

| Device State | Input Conditions | | | | Status | Outputs | |
|---|---|---|---|---|---|---|---|
| | EN/$\overline{D2}$ | D1 | IN1 | IN2 | $\overline{SF}$ | OUT1 | OUT2 |
| Forward | H | L | H | L | H | H | L |
| Reverse | H | L | L | H | H | L | H |
| Freewheeling Low | H | L | L | L | H | L | L |
| Freewheeling High | H | L | H | H | H | H | H |
| Disable 1 (D1) | H | H | X | X | L | Z | Z |
| IN1 Disconnected | H | L | Z | X | H | H | X |
| IN2 Disconnected | H | L | X | Z | H | X | H |
| D1 Disconnected | H | Z | X | X | L | Z | Z |
| Under-voltage Lockout(30) | H | X | X | X | L | Z | Z |
| Over-temperature(31) | H | X | X | X | L | Z | Z |
| Short-circuit(31) | H | X | X | X | L | Z | Z |
| Sleep mode EN/$\overline{D2}$ | L | X | X | X | H | Z | Z |
| EN/$\overline{D2}$ disconnected | Z | X | X | X | H | Z | Z |

Notes

30. In the event of an under-voltage condition, the outputs tri-state and status flag is SET logic LOW. Upon under-voltage recovery, status flag is reset automatically or automatically cleared and the outputs are restored to their original operating condition.
31. When a short-circuit or over-temperature condition is detected, the power outputs are tri-state latched-OFF independent of the input signals and the status flag is latched to logic LOW. To reset from this condition requires the toggling of either D1, EN/$\overline{D2}$, or $V_{PWR}$.

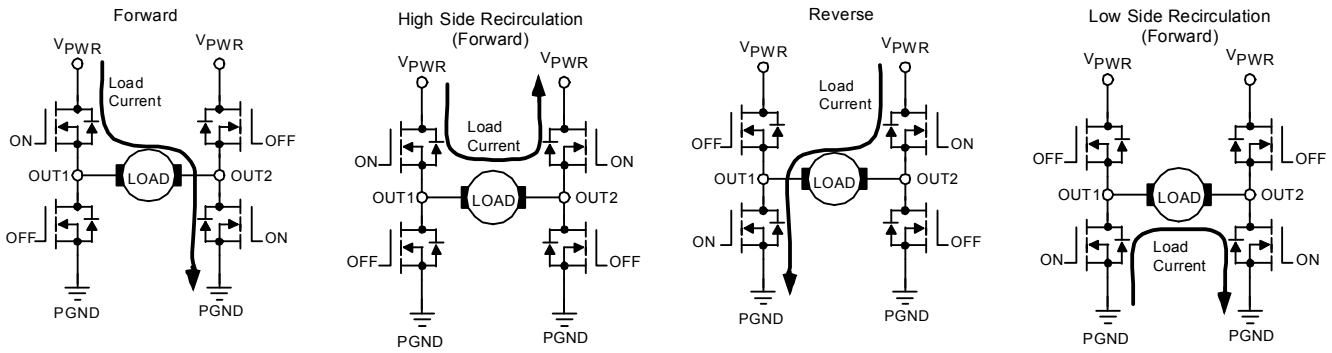



**Figure 12. 33932 Power Stage Operation**

# PROTECTION AND DIAGNOSTIC FEATURES

## SHORT-CIRCUIT PROTECTION

If an output short-circuit condition is detected, the power outputs tri-state (latch-OFF) independent of the input (IN1 and IN2) states, and the fault status output flag ($\overline{SF}$) is SET to logic LOW. If the $\overline{D1}$ input changes from logic HIGH to logic LOW, or if the EN/$\overline{D2}$ input changes from logic LOW to logic HIGH, the output bridge will become operational again and the fault status flag will be reset (cleared) to a logic HIGH state.

The output stage will always switch into the mode defined by the input pins (IN1, IN2, D1, and EN/$\overline{D2}$), provided the device junction temperature is within the specified operating temperature range.

## INTERNAL PWM CURRENT LIMITING

The maximum current flow under normal operating conditions should be less than 5.0 A. The instantaneous load currents will be limited to $I_{LIM}$ via the internal PWM current limiting circuitry. When the $I_{LIM}$ threshold current value is reached, the output stages are tri-stated for a fixed time ($T_A$) of 20 µs typical. Depending on the time constant associated with the load characteristics, the output current decreases during the tri-state duration until the next output ON cycle occurs.

The PWM current limit threshold value is dependent on the device junction temperature. When -40 °C < $T_J$ < 160 °C, $I_{LIM}$ is between the specified minimum/maximum values. When $T_J$ exceeds 160 °C, the $I_{LIM}$ threshold decreases to 4.2 A. Shortly above 175 °C the device over-temperature circuit will detect $t_{LIM}$ and an over-temperature shutdown will occur. This feature implements a graceful degradation of operation before thermal shutdown occurs, thus allowing for intermittent unexpected mechanical loads on the motor's gear-reduction train to be handled.

**Important** Die temperature excursions above 150 °C are permitted only for non-repetitive durations < 30 seconds. Provision must be made at the system level to prevent prolonged operation in the current-foldback region.

## OVER-TEMPERATURE SHUTDOWN AND HYSTERESIS

If an over-temperature condition occurs, the power outputs are tri-stated (latched-OFF) and the fault status flag ($\overline{SF}$) is SET to logic LOW.

To reset from this condition, D1 must change from logic HIGH to logic LOW, or EN/$\overline{D2}$ must change from logic LOW to logic HIGH. When reset, the output stage switches ON again, provided that the junction temperature is now below the over-temperature threshold limit minus the hysteresis.

**Important** Resetting from the fault condition will clear the fault status flag. Powering down and powering up the device will also reset the 33932 from the fault condition.

## OUTPUT AVALANCHE PROTECTION

If VPWR were to become an open circuit, the outputs would likely tri-state simultaneously due to the disable logic. This could result in an unclamped inductive discharge. The VPWR input to the 33932 should not exceed 40 V during this transient condition, to prevent electrical overstress of the output drivers.This can be accomplished with a zener clamp or MOV, and/or an appropriately valued input capacitor with sufficiently low ESR (see Figure 13).

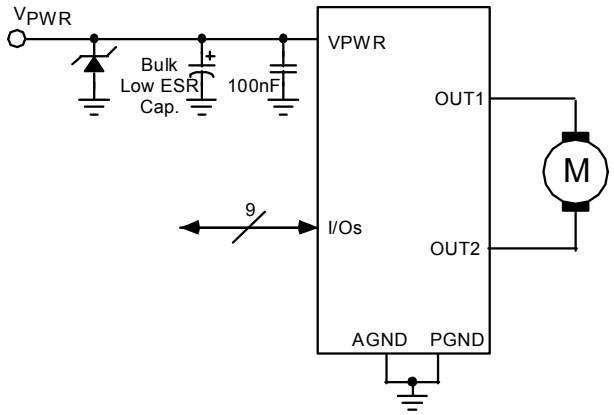



**Figure 13. Avalanche Protection**

# TYPICAL APPLICATIONS

## *INTRODUCTION*

A typical application schematic is shown in Figure 14. For precision high-current applications in harsh, noisy environments, the $V_{PWR}$ by-pass capacitor may need to be substantially larger.

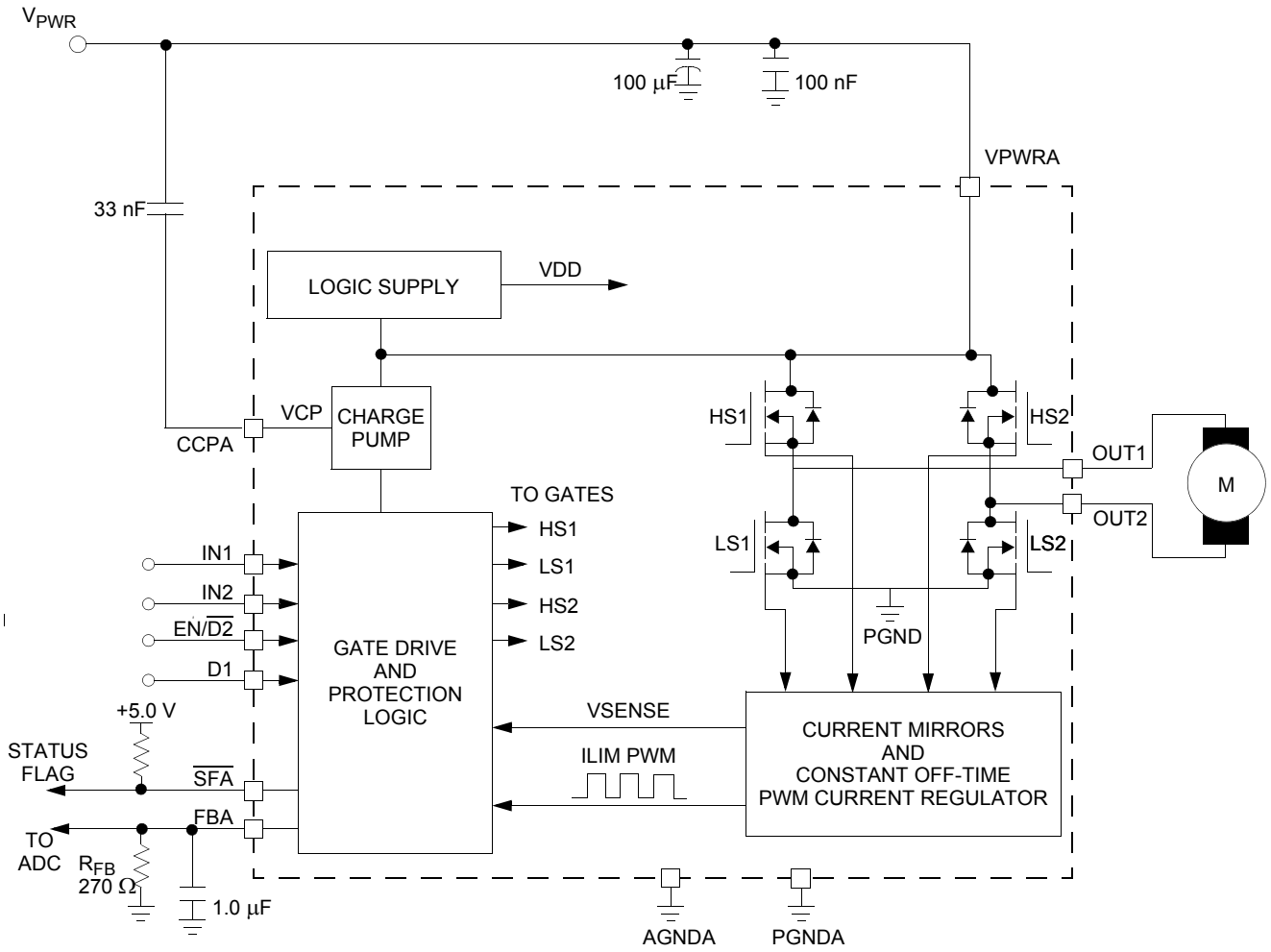
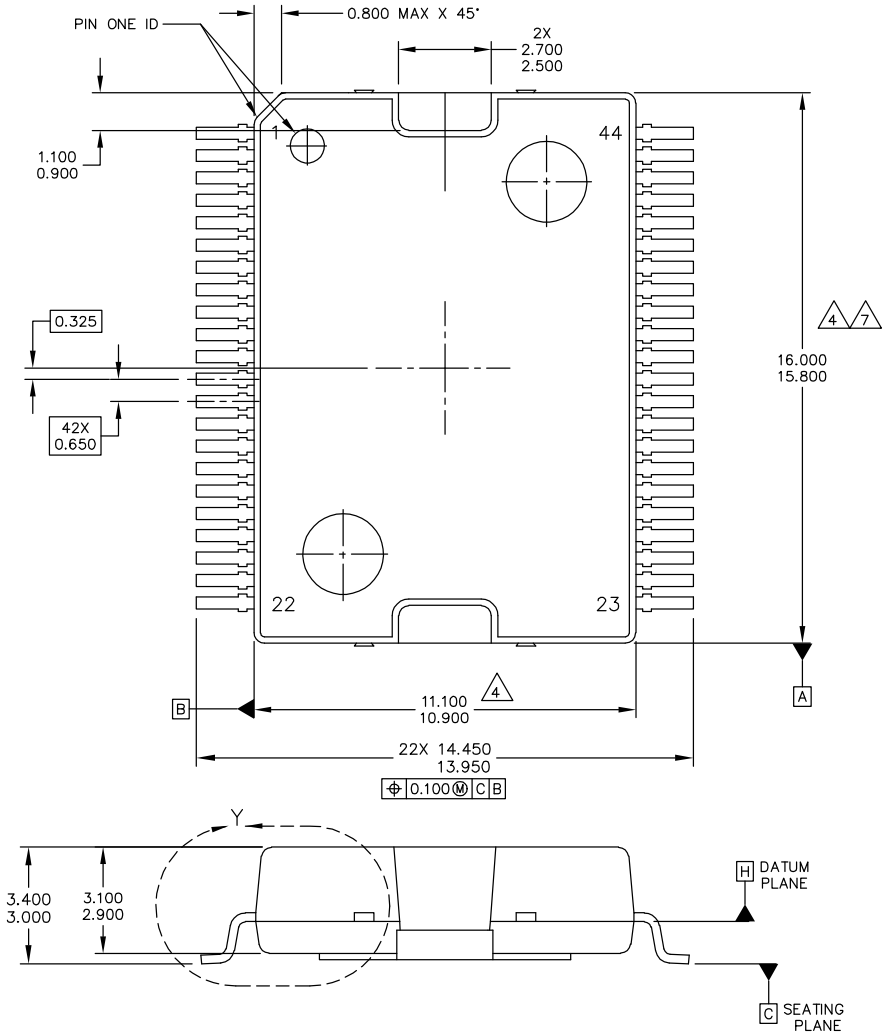



**Figure 14. 33932 Typical Application Schematic 1/2 Device**

# PACKAGING

## PACKAGE DIMENSIONS

For the most current package revision, visit **www.freescale.com** and perform a keyword search using the 98Axxxxxxxxx listed below. Dimensions shown are provided for reference ONLY.

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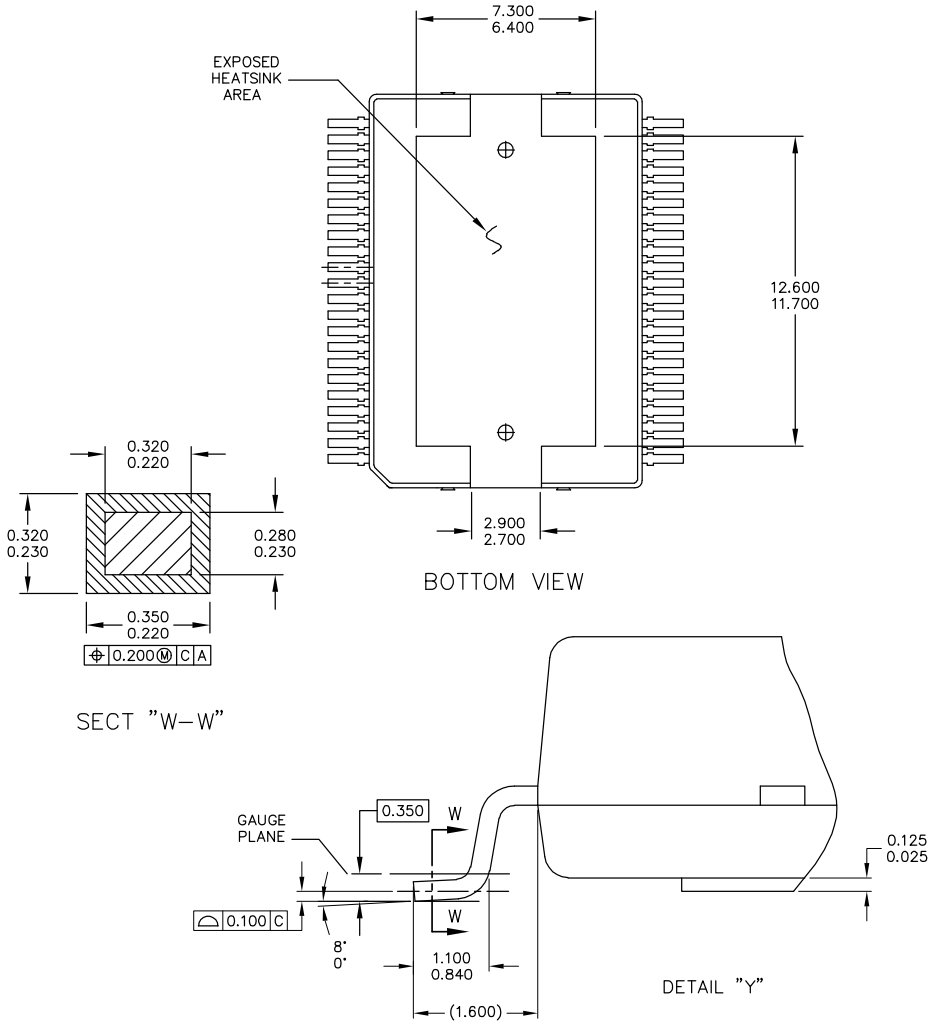
|---|---|---|
| TITLE: 44 LEAD HSOP W/PROTRUDING HEATSINK | DOCUMENT NO: 98ARH98330A | REV: B |
| | CASE NUMBER: 1291–02 | 16 MAR 2005 |
| | STANDARD: NON–JEDEC | |

**VW SUFFIX**
44-PIN
98ARH98330A
REVISION B

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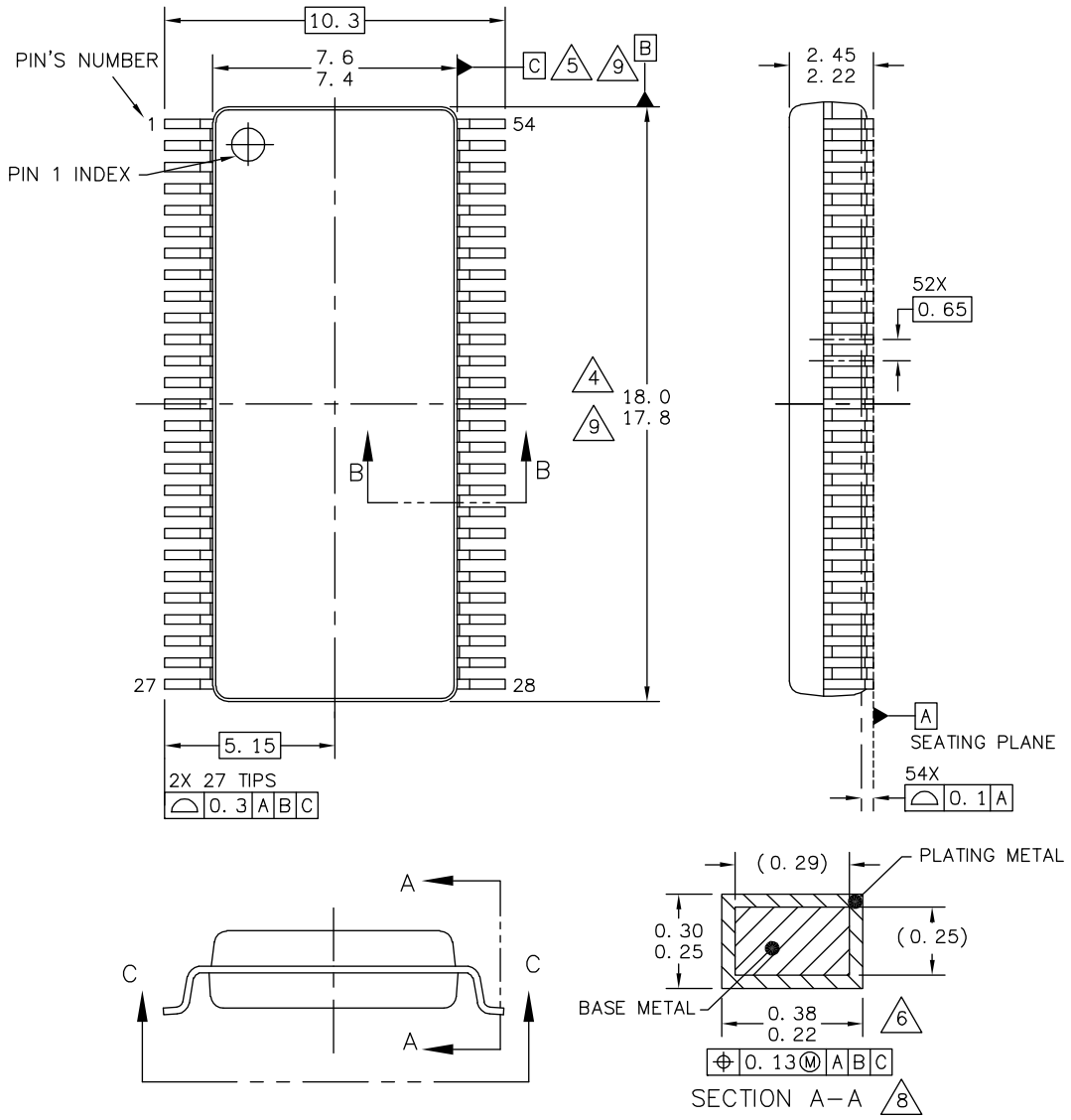
|---|---|---|
| TITLE: 44 LEAD HSOP W/PROTRUDING HEATSINK | DOCUMENT NO: 98ARH98330A | REV: B |
| | CASE NUMBER: 1291–02 | 16 MAR 2005 |
| | STANDARD: NON–JEDEC | |

**VW SUFFIX**
44-PIN
98ARH98330A
REVISION B

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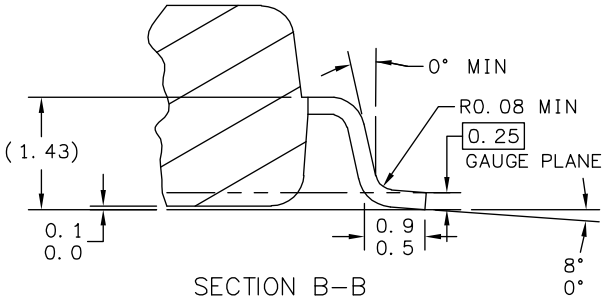
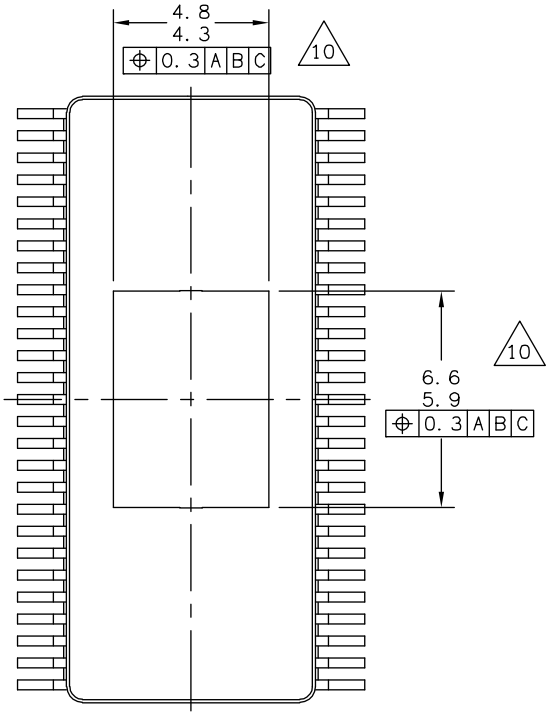
|---|---|---|
| TITLE: 54LD SOIC W/B, 0.65 PITCH 4.6 X 6.3 EXPOSED PAD, CASE–OUTLINE | DOCUMENT NO: 98ASA99334D | REV: C |
| | CASE NUMBER: 1377–02 | 11 MAR 2005 |
| | STANDARD: NON–JEDEC | |

**EK SUFFIX**
54-PIN
98ASA99334D
REVISION C




SECTION B–B




VIEW C–C

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|---|---|---|
| TITLE: 54LD SOIC W/B, 0. 65 PITCH 4. 6 X 6. 3 EXPOSED PAD, CASE–OUTLINE | DOCUMENT NO: 98ASA99334D | REV: C |
| | CASE NUMBER: 1377–02 | 11 MAR 2005 |
| | STANDARD: NON–JEDEC | |

**EK SUFFIX**
54-PIN
98ASA99334D
REVISION C

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSIONS DEFINE THE PRIMARY SOLDERABLE SURFACE AREA.

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|---|---|---|
| TITLE: 54LD SOIC W/B, 0.65 PITCH 4.6 X 6.3 EXPOSED PAD, CASE–OUTLINE | DOCUMENT NO: 98ASA99334D | REV: C |
| | CASE NUMBER: 1377–02 | 11 MAR 2005 |
| | STANDARD: NON–JEDEC | |

**EK SUFFIX**
54-PIN
98ASA99334D
REVISION C

# ADDITIONAL DOCUMENTATION

## *THERMAL ADDENDUM*

### Introduction

This thermal addendum is provided as a supplement to the MC33932 technical datasheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application, and packaging information is provided in the datasheet.

### Package and Thermal Considerations

The MC33932 is offered in a 54-pin SOICW-EP and a 44-pin HSOP single die package. There is a single heat source (P), a single junction temperature ($T_J$), and thermal resistance ($R_{\theta JA}$). This thermal addendum is specific to the 54-pin SOICW-EP package.

$$\{ T_J \} = [ R_{\theta JA} ] \cdot \{ P \}$$

The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to, and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

**Table 6. Table of Thermal Resistance Data**

| Rating | | | Value | Unit | Notes |
|---|---|---|---|---|---|
| Junction to Ambient<br>Natural Convection | Single Layer board (1s) | $R_{\theta JA}$ | 58.8 | °C/W | (32),(33) |
| Junction to Ambient<br>Natural Convection | Four layer board (2s2p) | $R_{\theta JA}$ | 24.4 | °C/W | (32),(34) |
| Junction to Board | | $R_{\theta JB}$ | 7.0 | °C/W | (35) |
| Junction to Case (bottom / flag) | | $R_{\theta JC}$ (bottom) | 0.36 | °C/W | (38) |
| Junction to Case (top) | | $R_{\theta JC}$ (top) | 18 | °C/W | (36) |
| Junction to Package Top | Natural Convection | $\Psi_{JT}$ | 2.0 | °C/W | (37) |

Notes

32. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
33. Per JEDEC JESD51-2 with the single layer board (JESD51-3) horizontal.
34. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
35. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
36. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
37. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
38. Thermal resistance between the die and the case bottom / flag surface (simulated) (flag bottom side fixed to ambient temperature).

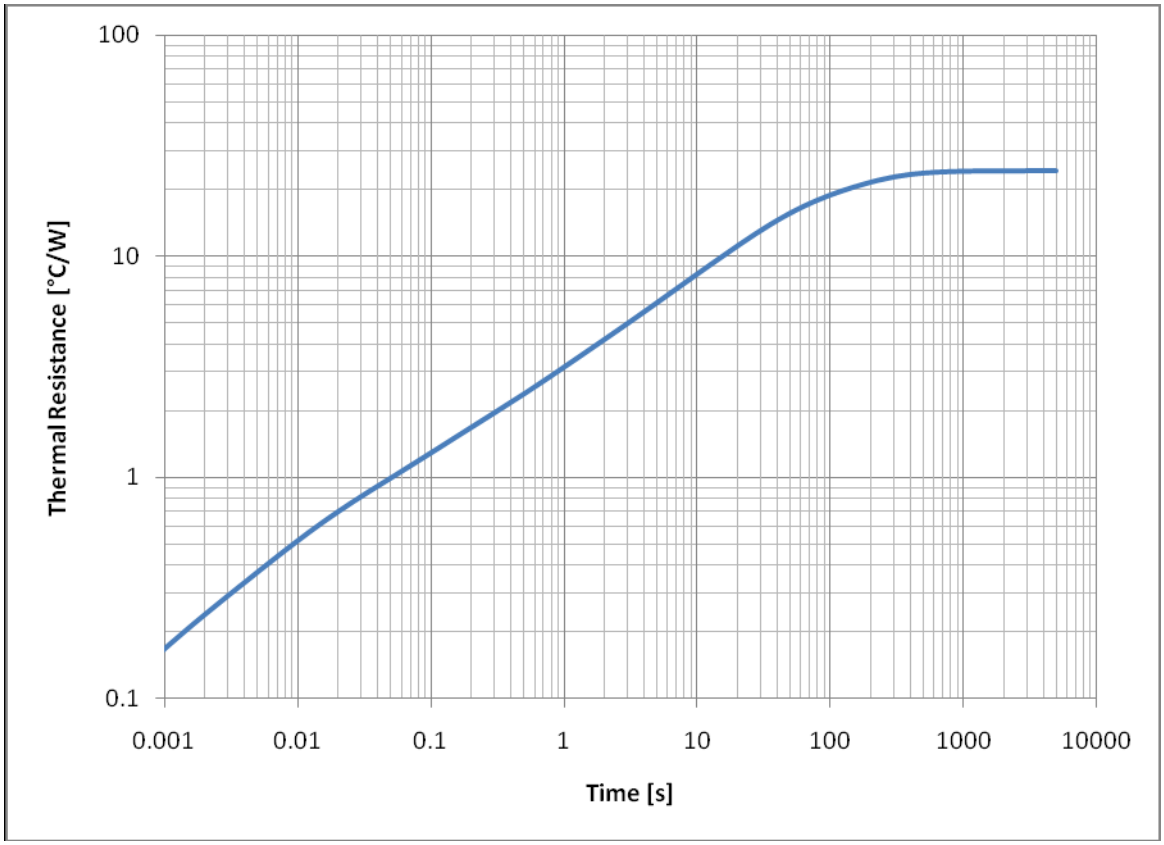


**Figure 15. Transient Thermal Resistance $R_{\theta JA}$ MC33932EK on 2s2p Test Board**

# REFERENCE SECTION

**Table 7. Thermal Analysis Reference Documents**

| Reference | Description |
|---|---|
| AN4146 | Thermal Modeling and Simulation of 12V Gen3 eXtreme Switch Devices with SPICE |
| BASICTHERMALWP | Basic Principles of Thermal Analysis for Semiconductor Systems |

# REVISION HISTORY

| REVISION | DATE | DESCRIPTION |
|---|---|---|
| 1.0 | 8/2007 | • Initial Release |
| 2.0 | 8/2008 | • Added parameters (TBD) for Change Pump Voltages in Table 3 |
| 3.0 | 11/2008 | • Changed maximum $R_{DS(ON)}$ from 225 to 235 mΩ.<br>• Changed Peak Package Reflow Temperature During Reflow(7), (8)<br>• Changed Approximate Junction-to Case Thermal Resistance(9) |
| 4.0 | 6/2012 | • Added PC33932EK to the Ordering Information Table<br>• Added EK ordering information<br>• Form and style corrections<br>• Added note 25<br>• Added Thermal Addendum and Reference Document sections<br>• Added 98ASA99334D package drawing<br>• Minor corrections throughout the spec |
| 5.0 | 10/2012 | • PC33932EK changed to MC33932EK and released to production<br>• Document level changed from Advance Information to Technical Data<br>• Changed SOIC to SOICW-EP |

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Rev. 5.0
10/2012