1 Orderable parts

Table 1. Orderable part variations

Part number [1]	Temperature (T_A)	Package	Parameter	Symbol	Condition	33660	33660B [2]
MC33660EF	-40 °C to 125 °C	8-SOICN	VBB Load Dump Peak Voltage (in accordance with ISO 7637-2 & ISO 7637-3)	$V_{BB(5a)}$	**Pulse 5a** 470 ohm series resistor and 100 nF capacitor to GND on VBB	–	82 V
				$V_{BB(5b)}$	**Pulse 5b** 470 ohm series resistor and 100 nF capacitor to GND on VBB	45 V	45 V
MC33660BEF			Module Level ESD (Air Discharge, Powered)	V_{ESD4}	33 V zener diode and 470 pF capacitor to GND on ISO	–	±25000 V

Notes
1. To order parts in tape & reel, add the R2 suffix to the part number.
2. Recommended for all new designs

2 Internal block diagram

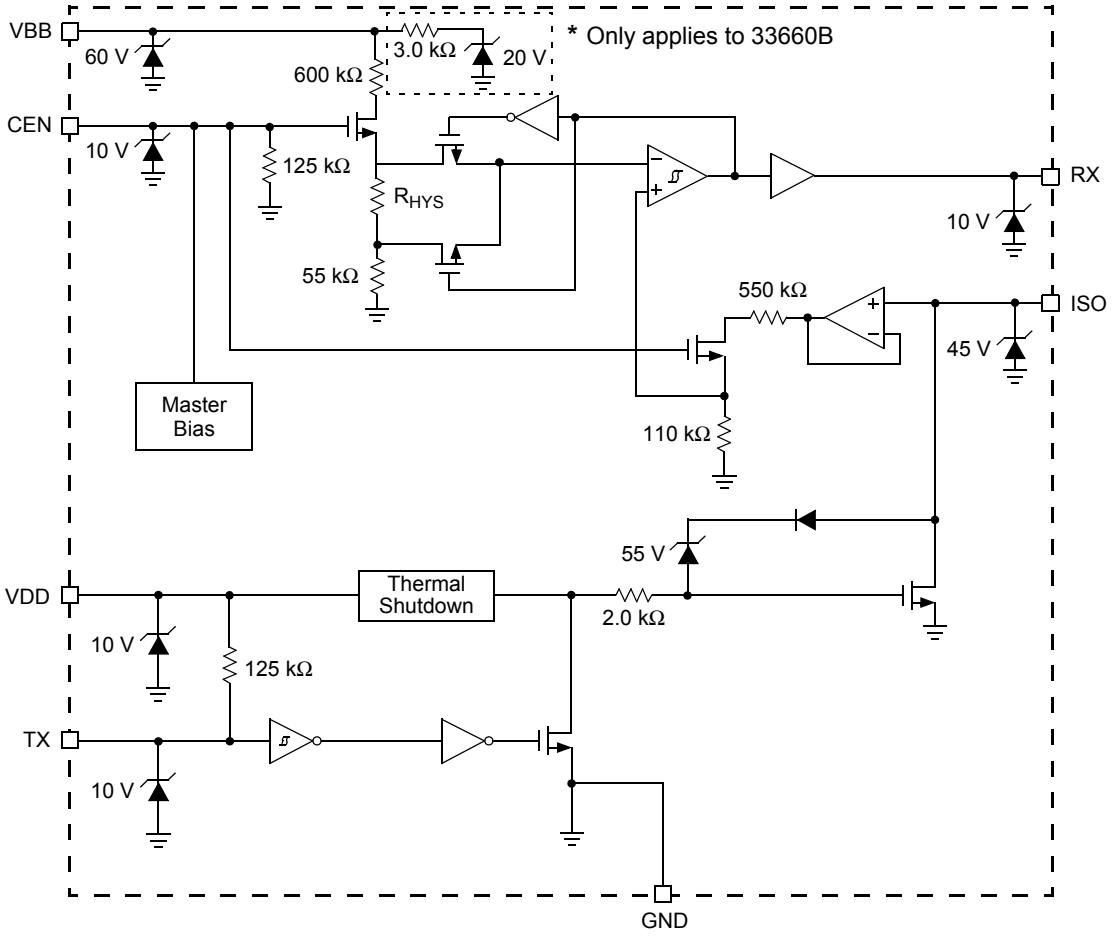


Figure 2. 33660 simplified internal block diagram

3 Pin connections

3.1 Pinout diagram

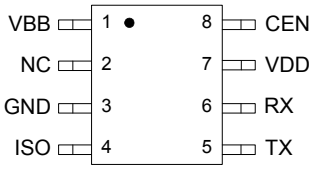


Figure 3. 33660 pin connections

3.2 Pin definitions

Table 2. 33660 pin definitions

Pin Number	Pin Name	Definition
1	VBB	Battery power through external resistor and diode.
2	NC	Not to be connected. (3)
3	GND	Common signal and power return.
4	ISO	Bus connection.
5	TX	Logic level input for data to be transmitted on the bus.
6	RX	Logic output of data received on the bus.
7	VDD	Logic power source input.
8	CEN	Chip enable. Logic “1” for active state. Logic “0” for sleep state.

Notes

3. NC pins should not have any connections made to them. NC pins are not guaranteed to be open circuits.

4 Electrical characteristics

4.1 Maximum ratings

Table 3. Maximum ratings

All voltages are with respect to ground unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Rating	Value	Unit	Notes
V_{DD}	VDD DC Supply Voltage	-0.3 to 7.0	V	
$V_{BB(5a)}$ $V_{BB(5b)}$	VBB Load Dump Peak Voltage (in accordance with ISO 7637-2 & ISO 7637-3) • Pulse 5a - 33660B only • Pulse 5b	 82 45	V	
V_{ISO}	ISO Pin Load Dump Peak Voltage	40	V	(4)
V_{ESD1} V_{ESD2}	ESD Voltage • Human Body Model • Machine Model 33660 33660B	 ±2000 ±150 ±200	V	(5) (6) (6)
V_{ESD3-1} V_{ESD3-2}	• Charge Device Model Corner Pins All other Pins	 ±750 ±500	V	(6)
V_{ESD4}	• Module Level ESD (Air Discharge, Powered) 33660B only ISO pin with 33 V zener diode and 470 pF capacitor to GND -	 ±25000		(7)
E_{CLAMP}	ISO Clamp Energy	10	mJ	(8)
T_{STG}	Storage Temperature	-55 to +150	°C	
T_C	Operating Case Temperature	-40 to +125	°C	
T_J	Operating Junction Temperature	-40 to +150	°C	
P_D	Power Dissipation T_A = 25 °C	100	mW	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	Note 10.	°C	(9), (10)
$R_{\theta JA}$	Thermal Resistance: Junction-to-Ambient	150	°C/W	

Notes

4. Device will survive double battery jump start conditions in typical applications for 10 minutes duration, but is not guaranteed to remain within specified parametric limits during this duration.
5. ESD data available upon request.
6. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), ESD3 testing is performed in accordance with the Charge Device Model (C_{ZAP} = 4.0 pF).
7. ESD4 testing is performed in accordance with ISO 10605 ESD model (C = 330 pF, R = 2.0 kΩ). ESD discharges start at ±5.0 kV and go up to ±25 kV in increments of 5.0 kV. There are two positions for discharges: 8.0 cm cable from ISO connector, 85 cm cable from ISO connector. There are 10 ESD discharges per voltage at each cable position at a minimum of 1.0 s intervals. Remaining charge is not bled off after every discharge.
8. Nonrepetitive clamping capability at 25 °C.
9. Pin soldering temperature limit is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.
10. Freescale's Package Reflow capability meets Pb-free requirements for JEDEC standard J-STD-020C. For Peak Package Reflow Temperature and Moisture Sensitivity Levels (MSL), Go to www.freescale.com, search by part number [e.g. remove prefixes/suffixes and enter the core ID to view all orderable parts. (i.e. MC33xxxD enter 33xxx), and review parametrics.

4.2 Static electrical characteristics

Table 4. Static electrical characteristics

Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB} ≤ 18 V, -40 °C ≤ T_C ≤ 125 °C, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
Power and control						
$I_{DD(SS)}$	V_{DD} Sleep State Current • T_x = 0.8 V_{DD}, CEN = 0.3 V_{DD}	–	–	0.1	mA	
$I_{DD(Q)}$	V_{DD} Quiescent Operating Current • T_x = 0.2 V_{DD}, CEN = 0.7 V_{DD}	–	–	1.0	mA	
$I_{BB(SS)}$	V_{BB} Sleep State Current • V_{BB} = 16 V, T_x = 0.8 V_{DD}, CEN = 0.3 V_{DD}	–	–	50	µA	
$I_{BB(Q)}$	V_{BB} Quiescent Operating Current • T_X = 0.2 V_{DD}, CEN = 0.7 V_{DD}	–	–	1.0	mA	
$V_{IH(CEN)}$ $V_{IL(CEN)}$	Chip Enable • Input High Voltage Threshold • Input Low Voltage Threshold	0.7 V_{DD} –	– –	– 0.3 V_{DD}	V	(11) (12)
$I_{PD(CEN)}$	Chip Enable Pull-down Current	2.0	–	40	µA	(13)
$V_{IL(TX)}$	T_X Input Low Voltage Threshold • R_{ISO} = 510 Ω	–	–	0.3 x V_{DD}	V	(14)
$V_{IH(TX)}$	T_X Input High Voltage Threshold • R_{ISO} = 510 Ω	0.7 x V_{DD}	–	–	V	(15)
$I_{PU(TX)}$	T_X Pull-up Current	-40	–	-2.0	µA	(16)
$V_{OL(RX)}$	R_X Output Low Voltage Threshold • R_{ISO} = 510 Ω, T_X = 0.2 V_{DD}, R_x Sinking 1.0 mA	–	–	0.2 V_{DD}	V	
$V_{OH(RX)}$	R_X Output High Voltage Threshold • R_{ISO} = 510 Ω, T_X = 0.8 V_{DD}, R_X Sourcing 250 µA	0.8 V_{DD}	–	–	V	
T_{LIM}	Thermal Shutdown	150	170	–	°C	(17)
ISO I/O						
$V_{IL(ISO)}$	Input Low Voltage Threshold • R_{ISO} = 510 Ω, T_X = 0.8 V_{DD}	–	–	0.4 x V_{BB}	V	
$V_{IH(ISO)}$	Input High Voltage Threshold • R_{ISO} = 510 Ω, T_X = 0.8 V_{DD}	0.7 x V_{BB}	–	–	V	
$V_{HYS(ISO)}$	Input Voltage Hysteresis	0.05 x V_{BB}	–	0.1 x V_{BB}	V	
$I_{PU(ISO)}$	Internal Pull-up Current • R_{ISO} = ∞ Ω, T_X = 0.8 V_{DD}, V_{ISO} = 9.0 V, V_{BB} = 18 V	-5.0	–	-140	µA	
$I_{SC(ISO)}$	Short-circuit Current Limit • R_{ISO} = 0 Ω, T_X = 0.4 V_{DD}, V_{ISO} = V_{BB}	50	–	200	mA	

Notes

11. When I_{BB} transitions to >100 µA.
12. When I_{BB} transitions to <100 µA.
13. Enable pin has an internal current pull-down. Pull-down current is measured with CEN pin at 0.3 V_{DD}.
14. Measured by ramping T_X down from 0.8 V_{DD} and noting T_X value at which ISO falls below 0.2 V_{BB}.
15. Measured by ramping T_X up from 0.2 V_{DD} and noting the value at which ISO rises above 0.9 V_{BB}.
16. T_x pin has internal current pull-up. Pull-up current is measured with T_X pin at 0.7 V_{DD}.
17. Thermal Shutdown performance (T_{LIM}) is guaranteed by design, but not production tested.

Table 4. Static electrical characteristics (continued)

Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB} ≤ 18 V, -40 °C ≤ T_C ≤ 125 °C, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
ISO I/O (Continued)						
$V_{OL(ISO)}$	Output Low Voltage • R_{ISO} = 510 Ω, T_X = 0.2 V_{DD}	–	–	0.1 x V_{BB}	V	
$V_{OH(ISO)}$	Output High Voltage • R_{ISO} = ∞ Ω, T_X = 0.8 V_{DD}	0.95 x V_{BB}	–	–	V	

4.3 Dynamic electrical characteristics

Table 5. Dynamic electrical characteristics

Characteristics noted under conditions of 4.75 V ≤ V_{DD} ≤ 5.25 V, 8.0 V ≤ V_{BB} ≤ 18 V, -40 °C ≤ T_C ≤ 125 °C, unless otherwise noted.

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Notes
$t_{FALL(ISO)}$	Fall Time • R_{ISO} = 510 Ω to V_{BB}, C_{ISO} = 10 nF to Ground	–	–	2.0	µs	(18)
$t_{PD(ISO)}$	ISO Propagation Delay • High to Low: R_{ISO} = 510 Ω, C_{ISO} = 500 pF • Low to High: R_{ISO} = 510 Ω, C_{ISO} = 500 pF	 – –	 – –	 2.0 2.0	µs	(19) (20) (21)

Notes

18. Time required ISO voltage to transition from 0.8 V_{BB} to 0.2 V_{BB}.
19. Changes in the value of C_{ISO} affect the rise and fall time but have minimal effect on Propagation Delay.
20. Step T_X voltage from 0.8 V_{DD} to 0.2 V_{DD}. Time measured from $V_{IH(Tx)}$ until V_{ISO} reaches 0.3 V_{BB}.
21. Step T_X voltage from 0.2 V_{DD} to 0.8 V_{DD}. Time measured from $V_{IL(Tx)}$ until V_{ISO} reaches 0.7 V_{BB}.

4.4 Electrical performance curves

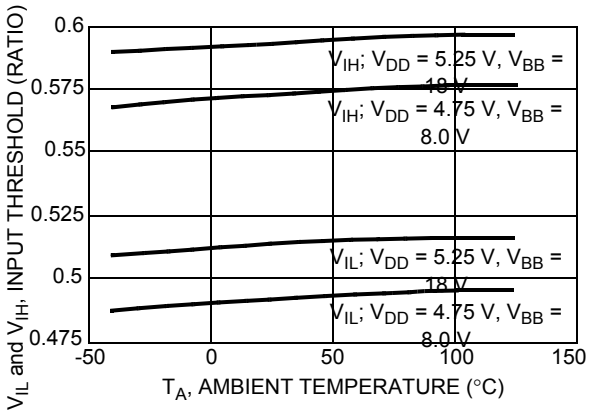


Figure 4. ISO input threshold/V_{BB} vs. temperature

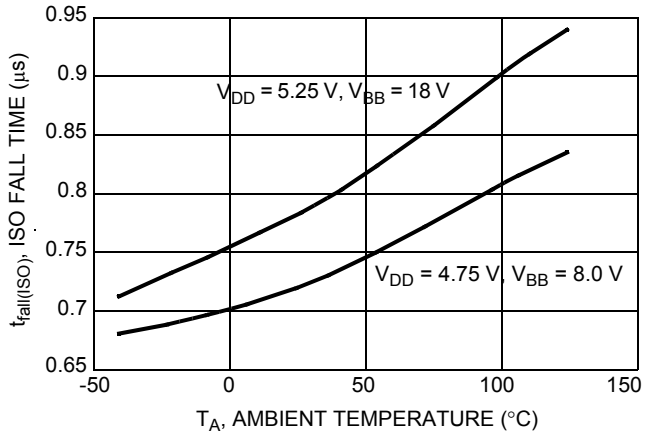


Figure 5. ISO output/V_{BB} vs. temperature

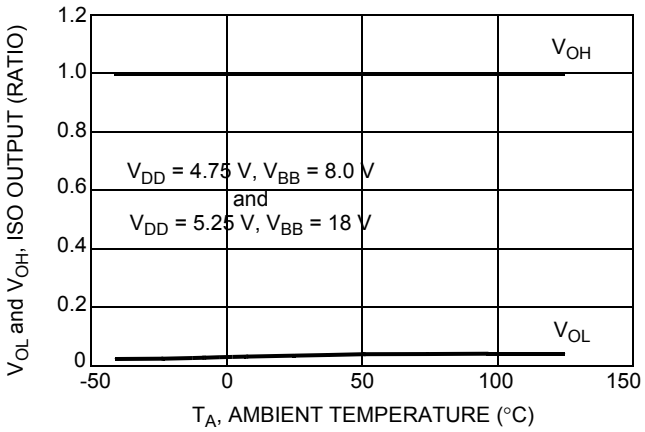


Figure 6. ISO fall time vs. temperature

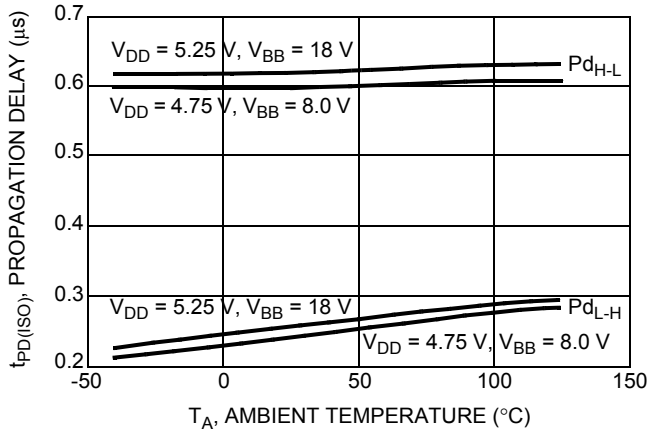


Figure 7. ISO propagation delay vs. temperature

5 Typical applications

5.1 Introduction

The 33660 is a serial link bus interface device conforming to the ISO 9141 physical bus specification. The device is designed for automotive environment usage, compliant with On-board Diagnostics (OBD) requirements set forth by the California Air Resources Board (CARB) using the ISO K line. The device does not incorporate an ISO L line. It provides bi-directional half-duplex communications interfacing from a microcontroller to the communication bus. The 33660 incorporates circuitry to interface the digital translations from 5.0 V microcontroller logic levels to battery level logic, and from battery level logic to 5.0 V logic levels. The 33660 is built using Freescale Semiconductor's SMARTMOS process and is packaged in an 8-pin plastic SOIC.

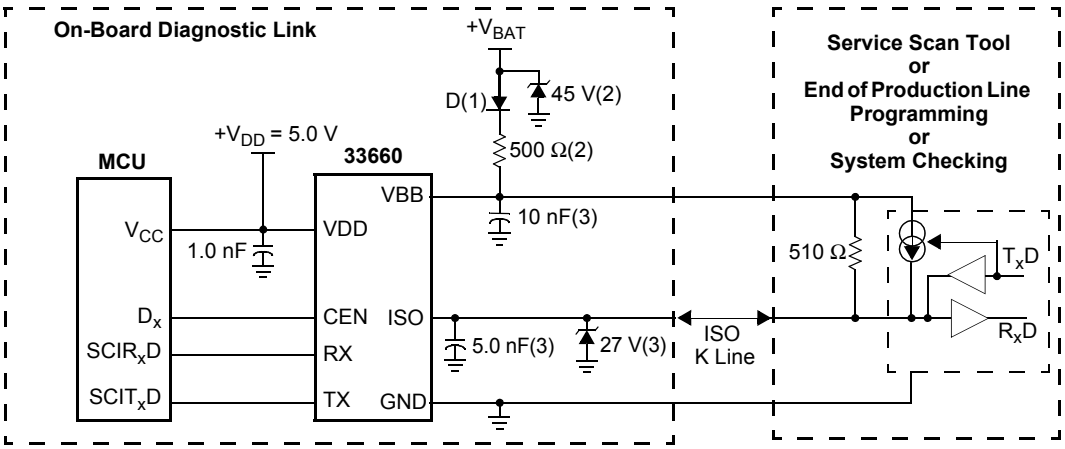
5.2 Functional description

The 33660 transforms 5.0 V microcontroller logic signals to battery level logic signals and vice versa. The maximum data rate is set by the rise and fall time. The fall time is set by the output driver. The rise time is set by the bus capacitance and the pull-up resistors on the bus. The fall time of the 33660 allows data rates up to 150 kbps using a 30 percent maximum bit time transition value. The serial link interface remains fully functional over a battery voltage range of 6.0 V to 18 V. The device is parametrically specified over a dynamic V_{BB} voltage range of 8.0 V to 18 V.

Required input levels from the microcontroller are ratio-metric with the V_{DD} voltage normally used to power the microcontroller. This enhances the 33660's ability to remain in harmony with the R_X and T_X control input signals of the microcontroller. The R_X and T_X control inputs are compatible with standard 5.0 V CMOS circuitry. For fault tolerant purposes the T_X input from the microcontroller has an internal passive pull-up to V_{DD}, while the CEN input has an internal passive pull-down to ground.

A pull-up to battery is internally provided as well as an active data pull-down. The internal active pull-down is current-limit protected against shorts to battery, and further protected by thermal shutdown. Typical applications have reverse battery protection by the incorporation of an external 510 Ω pull-up resistor and a diode to battery.

Reverse battery protection of the device is provided by the use of a reverse battery blocking diode (See "D" in the Typical application diagram on page 9). Battery line transient protection of the device is provided for by using a 45 V zener and a 500 Ω resistor connected to the V_{BB} source, as shown in the same diagram. Device ESD protection from the communication lines exiting the module is through the use of the capacitor connected to the V_{BB} device pin, and the capacitor used in conjunction with the 27 V zener connected to the ISO pin.



Components necessary for Reverse Battery (1), Overvoltage Transient (2), and 8.0 kV ESD Protection (3) in a metal module case.

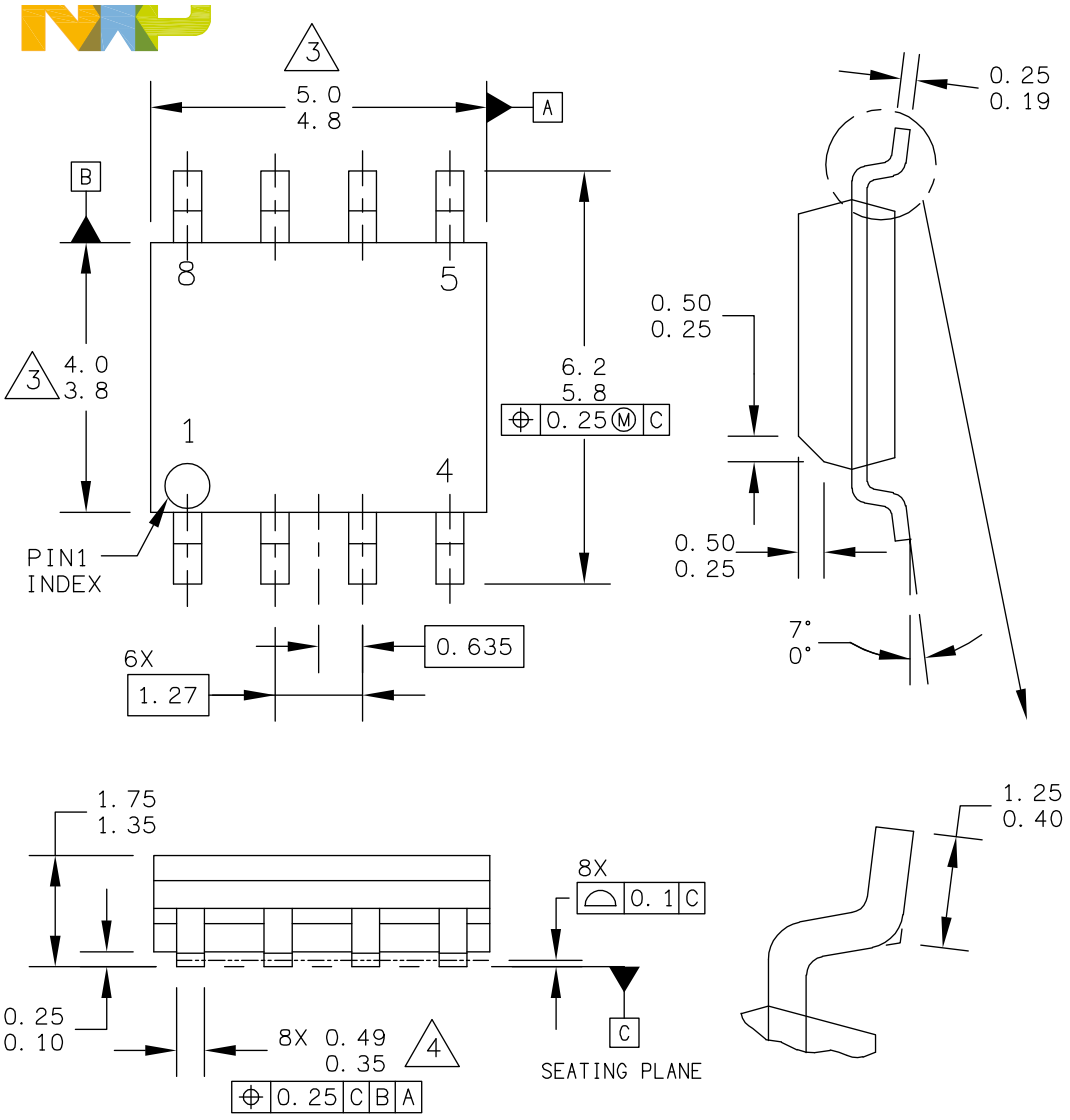
Figure 8. Typical application diagram

6 Packaging

6.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.NXP.com and perform a keyword search for the drawing's document number.

Package	Suffix	Package outline drawing number
8-Pin SOICN	EF	98ASB42564B



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	SOT96-4	11 APR 2016

33660

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.

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	STANDARD: JEDEC MS-012AA
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7 Revision history

Revision	Date	Description of changes
1.0	1/2011	• Initial release
2.0	9/2011	• Adjusted format to meet current compliance standards. No data was altered.
3.0	10/2011	• Updated the PC part number to MC.
4.0	2/2013	• Added PC33660BEF to the ordering information • Redefined VBB Load Dump Peak Voltage (in accordance with ISO 7637-2 & ISO 7637-3) for the 33660B • Added Module Level ESD (Air Discharge, Powered) for the 33660B • Added note (7) • Increased ESD structure voltage for 33660B, and added bleed-off circuit on VBB pin in Figure 2
5.0	10/2013	• Clarified machine model limits for MC33660 and MC33660B, page 5
6.0	1/2016	• Changed document classification to Technical Data • Updated format and style
	7/2016	• Updated to NXP document form and style

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