MBR16..PbF Series

Vishay High Power Products Schottky Rectifier, 16 A



ELECTRICAL SPECIFICATIONS						
PARAMETER	SYMBOL	TEST CO	VALUES	UNITS		
Maximum forward voltage drop	V _{FM} ⁽¹⁾	16 A	T _J = 25 °C	0.63	V	
Maximum forward voltage drop			T _J = 125 °C	0.57]	
Maximum instantaneous reverse current	I _{RM} ⁽¹⁾	T _J = 25 °C	Rated DC voltage	0.2	mA	
Maximum instantaneous reverse current		T _J = 125 °C	hated DC voltage	40		
Maximum junction capacitance	C _T	$V_R = 5 V_{DC}$ (test signal range 100 kHz to 1 MHz) 25 °C		1400	pF	
Typical series inductance	L _S	Measured from top of terminal to mounting plane		8.0	nΗ	
Maximum voltage rate of change	dV/dt	Rated V _R		10 000	V/µs	

Note

 $^{^{(1)}\,}$ Pulse width < 300 µs, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS						
PARAMETER		SYMBOL	TEST CONDITIONS	VALUES	UNITS	
Maximum junction temperature range		TJ		- 65 to 150	°C	
Maximum storage temperature range		T _{Stg}	- 68		C	
Maximum thermal resistance, junction to case		R _{thJC}	DC operation	1.50		
Typical thermal resistance, case to heatsink		R _{thCS}	Mounting surface, smooth and greased	0.50	°C/W	
Approximate weight				2	g	
				0.07	OZ.	
Mounting torque	minimum			6 (5)	kgf · cm	
	maximum			12 (10)	(lbf \cdot in)	
Marking device			Coop at the TO 200AC (IEDEC)	MBR	MBR1635	
			Case style TO-220AC (JEDEC)	MBR	MBR1645	

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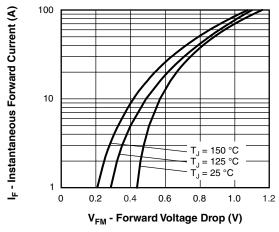


Fig. 1 - Maximum Forward Voltage Drop Characteristics

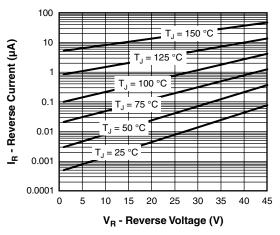


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

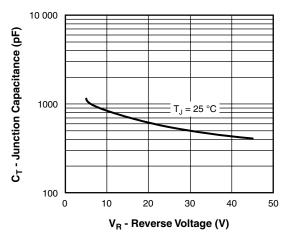


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

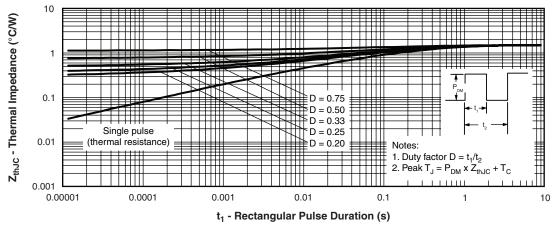


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics

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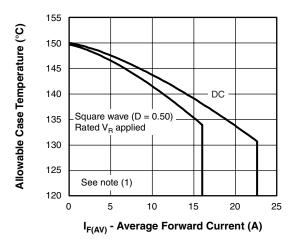


Fig. 5 - Maximum Allowable Case Temperature vs.
Average Forward Current

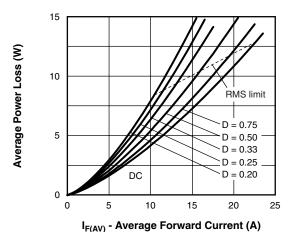


Fig. 6 - Forward Power Loss Characteristics

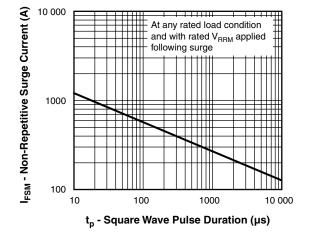


Fig. 7 - Maximum Non-Repetitive Surge Current (Per Leg)

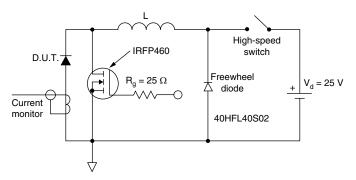


Fig. 8 - Unclamped Inductive Test Circuit

Note

 $^{(1)}$ Formula used: T_C = T_J - (Pd + Pd_{REV}) x R_{th,JC}; Pd = Forward power loss = I_{F(AV)} x V_{FM} at (I_{F(AV)}/D) (see fig. 6); Pd_{REV} = Inverse power loss = V_{R1} x I_R (1 - D); I_R at V_{R1} = Rated V_R applied

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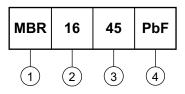


Schottky Rectifier, 16 A

Vishay High Power Products

ORDERING INFORMATION TABLE

Device code



1 - Schottky MBR series

Current rating (16 = 16 A)

35 = 35 V 45 = 45 V None = Standard production

• PbF = Lead (Pb)-free

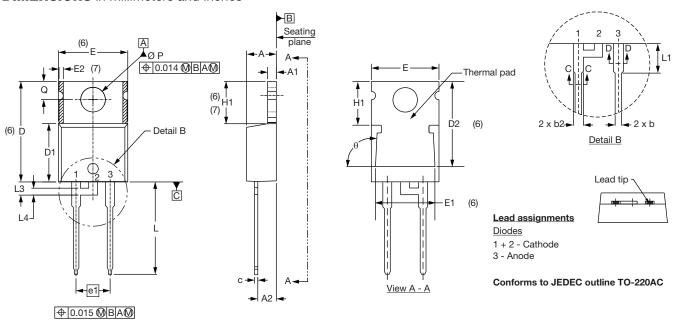
LINKS TO RELATED DOCUMENTS					
Dimensions	http://www.vishay.com/doc?95221				
Part marking information	http://www.vishay.com/doc?95224				

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Vishay Semiconductors

TO-220AC

DIMENSIONS in millimeters and inches



SYMBOL	MILLIM	IETERS	INC	NOTES	
STWIBOL	MIN.	MAX.	MIN.	MAX.	NOTES
Α	4.25	4.65	0.167	0.183	
A1	1.14	1.40	0.045	0.055	
A2	2.56	2.92	0.101	0.115	
b	0.69	1.01	0.027	0.040	
b1	0.38	0.97	0.015	0.038	4
b2	1.20	1.73	0.047	0.068	
b3	1.14	1.73	0.045	0.068	4
С	0.36	0.61	0.014	0.024	
c1	0.36	0.56	0.014	0.022	4
D	14.85	15.25	0.585	0.600	3
D1	8.38	9.02	0.330	0.355	
D2	11.68	12.88	0.460	0.507	6
Е	10.11	10.51	0.398	0.414	3, 6

SYMBOL	MILLIMETERS		INCHES		NOTES
STIVIBUL	MIN.	MAX.	MIN.	MAX.	NOTES
E1	6.86	8.89	0.270	0.350	6
E2	-	0.76	-	0.030	7
е	2.41	2.67	0.095	0.105	
e1	4.88	5.28	0.192	0.208	
H1	6.09	6.48	0.240	0.255	6, 7
L	13.52	14.02	0.532	0.552	
L1	3.32	3.82	0.131	0.150	2
L3	1.78	2.13	0.070	0.084	
L4	0.76	1.27	0.030	0.050	2
ØΡ	3.54	3.73	0.139	0.147	
Q	2.60	3.00	0.102	0.118	
θ	90° to 93°		90° to 93°		

Notes

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- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension and finish uncontrolled in L1
- (3) Dimension D, D1 and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (4) Dimension b1, b3 and c1 apply to base metal only
- (5) Controlling dimension: inches
- (6) Thermal pad contour optional within dimensions E, H1, D2 and E1
- (7) Dimension E2 x H1 define a zone where stamping and singulation irregularities are allowed
- (8) Outline conforms to JEDEC TO-220, D2 (minimum) where dimensions are derived from the actual package outline

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