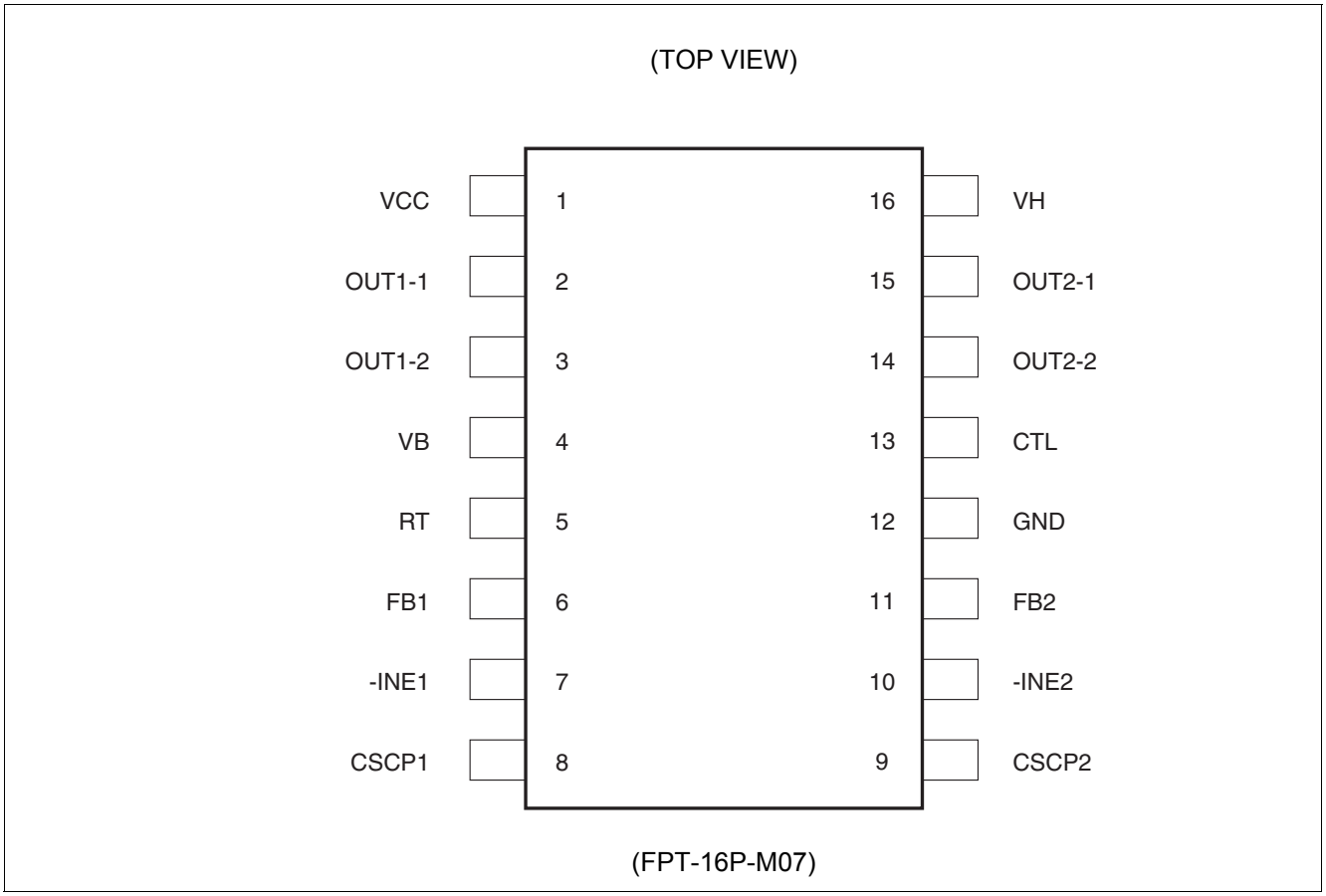
Contents

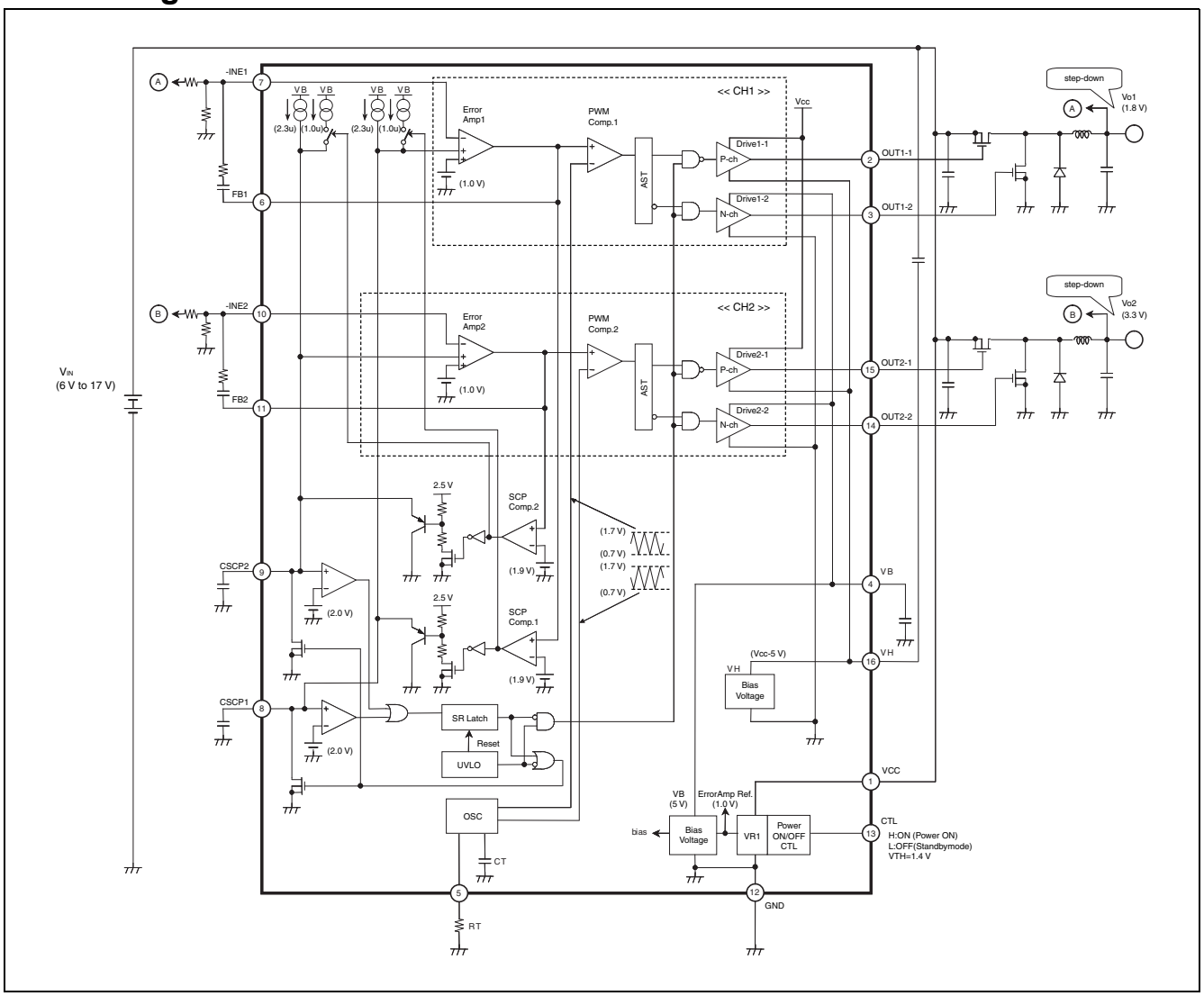
1. Pin Assignment



2. Pin Description

Pin No.	Pin Name	I/O	Description
1	VCC	-	Power supply pin for the reference voltage circuit and control circuit.
2	OUT1-1	O	Output pin for P-ch drive (drives the gate of the external High side FET).
3	OUT1-2	O	Output pin for N-ch drive (drives the gate of the external Low side FET).
4	VB	I/O	Power supply pin for the N-ch FET drive circuit (VB = 5 V).
5	RT	-	Triangular-wave oscillation frequency setting resistor connection pin.
6	FB1	O	Error amplifier (Error Amp1) output pin.
7	-INE1	I	Error amplifier (Error Amp1) inverted input pin.
8	CSCP1	-	Timer-latch short-circuit protection circuit 1 capacitor connection pin.
9	CSCP2	-	Timer-latch short-circuit protection circuit 2 capacitor connection pin.
10	-INE2	I	Error amplifier (Error Amp2) inverted input pin.
11	FB2	O	Error amplifier (Error Amp2) output pin.
12	GND	-	Ground pin for the reference voltage circuit, control circuit, and output circuit.
13	CTL	I	Power supply control pin. IC becomes a stand-by mode by setting CTL pin “L” level.
14	OUT2-2	O	Output pin for N-ch drive (drives the gate of the external Low side FET).
15	OUT2-1	O	Output pin for P-ch drive (drives the gate of the external High side FET).
16	VH	O	Power supply pin for the N-ch FET drive circuit (VH = VCC – 5 V).

3. Block Diagram



4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{CC}	VCC pin	-	18	V
Input voltage	V_B	VB pin (When VCC pin connected to VB pin)	-	7	V
	V_{INE}	-INE1, -INE2 pins	− 0.3	V_B	V
	V_{CTL}	CTL pin	-	18	V
Output current	I_O	OUT1-1, OUT1-2, OUT2-1, OUT2-2 pins	-	60	mA
Peak output current	I_{OP}	Duty ≤ 5% (t = 1/fosc × Duty)	-	700	mA
Power dissipation	P_D	Ta ≤ + 25°C	-	1060[1]	mW
Storage temperature	T_{STG}	-	− 55	+ 125	°C

[1] : When mounted on a 10 cm square double-sided epoxy circuit board.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

5. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{CC}	VCC pin	4.5	12	17	V
VH pin output current	I_{VH}	VH pin	0	-	40	mA
VB pin output current	I_{VB}	VB pin	− 40	-	0	mA
VB pin input voltage	V_B	VB pin(When VCC pin connected to VB pin)	4.5	5	6	V
Input voltage	V_{INE}	-INE1, -INE2 pins	0	-	V_B − 0.9	V
CTL pin input voltage	V_{CTL}	CTL pin	0	-	17	V
Output current	I_{OUT}	OUT1-1, OUT1-2, OUT2-1, OUT2-2 pins	− 45	-	+ 45	mA
Oscillation frequency	f_{OSC}	Tj ≤ + 85°C	100	500	2000	kHz
Timing resistor	R_T	RT pin	3.6	16	100	kΩ
VH pin capacitor	C_{VH}	VH pin	-	1.0	4.7	µF
VB pin capacitor	C_{VB}	VB pin	-	1.0	4.7	µF
CSCP1, CSCP2 pin capacitor	CSCP1, CSCP2	CSCP1, CSCP2 pins	-	0.047	1.0	µF
Operating ambient temperature	Ta	-	− 30	+ 25	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

6. Electrical Characteristics

(Ta = +25°C, V_{CC} = 12 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Under Voltage Lockout Protection Circuit Block [UVLO]	Threshold voltage	V_{TLH}	4	VB ↑	3.8	4.0	4.2	V
		V_{THL}	4	VB ↓	3.6	3.8	4.0	V
	Hysteresis width	V_H	4	-	-	0.2[1]	-	V
Short-circuit protection circuit Block [SCP]	Threshold voltage	V_{TH}	8, 9	-	1.9	2.0	2.1	V
	Input source current	I_{CSCP}	8, 9	RT = 16 kΩ	− 3.2	− 2.3	− 1.4	µA
	Reset voltage	V_{RST}	4	VB = ↓	3.6	3.8	4.0	V
Triangular Wave Oscillator Block [OSC]	Oscillation frequency	fosc	2, 15	RT = 16 kΩ	450	500	550	kHz
Soft-Start Block [CS]	Charge current	I_{CS}	8, 9	CSCP1, 2 = 0 V, RT = 16 kΩ	− 4.6	− 3.3	− 2.0	µA
Error Amp Block [Error Amp1, Error Amp2]	Threshold voltage	V_{TH}	6, 11	FB1 = 1 V, FB2 = 1 V	0.99	1.00	1.01	V
	Input bias current	I_B	7, 10	-INE1 = 0 V, -INE2 = 0 V	− 100	0	+ 100	nA
	Voltage gain	A_V	6, 11	DC	-	80[1]	-	dB
	Frequency bandwidth	BW	6, 11	A_V = 0 dB	-	5.0[1]	-	MHz
	Output voltage	V_{OH}	6, 11	-	V_B − 0.3	V_B − 0.1	-	V
		V_{OL}	6, 11	-	-	40	200	mV
	Output source current	I_{SOURCE}	6, 11	FB1 = 1 V, FB2 = 1 V	-	-400	− 300	µA
	Output sink current	I_{SINK}	6, 11	FB1 = 1 V, FB2 = 1 V	4.0	8.0	-	mA
PWM Comparator Block [PWM Comp.1, PWM Comp.2]	Threshold voltage	V_{T0}	6, 11	Duty cycle = 0 %	0.6	0.7	-	V
		V_{T100}	6, 11	Duty cycle = 100 %	-	1.7	1.8	V
VH Bias Voltage Block [VH]	Output voltage	V_H	16	VCC = 6 V to 17 V VH = 0 to 40 mA	V_{CC} − 5.5	V_{CC} − 5.0	V_{CC} − 4.5	V
VB Bias Voltage Block [VB]	Output voltage	V_B	4	VCC = 6 V to 17 V VB = 0 to − 40 mA	4.5	5.0	5.5	V

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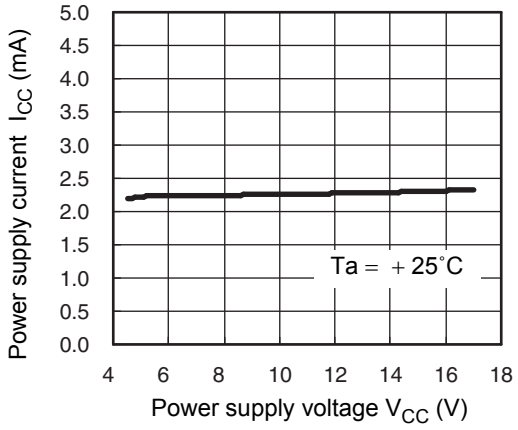
(Ta = +25°C, V_{CC} = 12 V)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Output Block[Drive1 to 2]	Output source current	I_{SOURCE}	2, 15	OUT1-1 = 7 V OUT2-1 = 7 V Duty ≤ 5%	-	– 500[1]	-	mA
			3, 14	VB = VCC = 5 V OUT1-2 = 0 V OUT2-2 = 0 V Duty ≤ 5%				
	Output sink current	I_{SINK}	2, 15	VCC = 5 V, At connect VH-GND OUT1-1 = 5 V OUT2-1 = 5 V Duty ≤ 5%	-	500[1]	-	mA
			3, 14	OUT1-2 = 5 V OUT2-2 = 5 V Duty ≤ 5%				
	Output on resistor	R_{OH}	2, 3, 14, 15	OUT1-1, OUT1-2, OUT2-1, OUT2-2 = – 45 mA	-	4.0	6.0	Ω
		R_{OL}	2, 15	OUT1-1, OUT2-1 = 45 mA	-	4.0	6.0	Ω
			3, 14	OUT1-2, OUT2-2 = 45 mA	-	2.6	3.9	Ω
	Dead time	td	2, 3, 14, 15	OUT1-1, OUT2-1 : H→L OUT1-2, OUT2-2 : H→L	20	40	80	ns
				OUT1-1, OUT2-1 : L →H OUT1-2, OUT2-2: L →H				
Control Block	CTL input voltage	V_{IH}	13	IC active mode	2	-	17	V
		V_{IL}	13	IC standby mode	0	-	0.8	V
	Input current	I_{CTLH}	13	CTL = 5 V	-	50	100	µA
		I_{CTLL}	13	CTL = 0 V	-	-	1	µA
General	Standby current	I_{CCS}	1	CTL = 0 V	-	0	10	µA
	Power supply current	I_{CC}	1	CTL = 5 V	-	2.2	3.3	mA

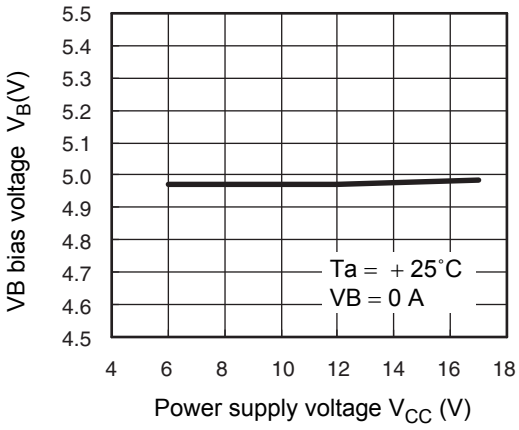
[1] : Standard design value

7. Typical Characteristics

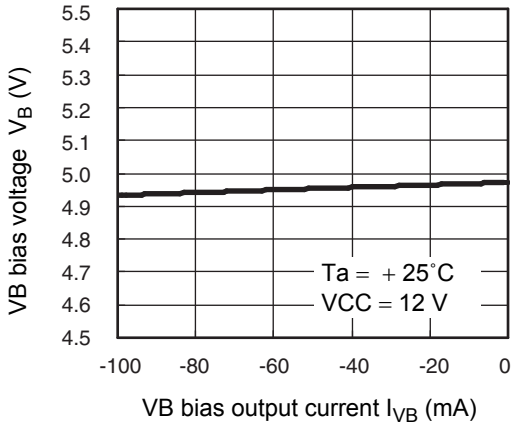
Power supply current vs.Power supply voltage



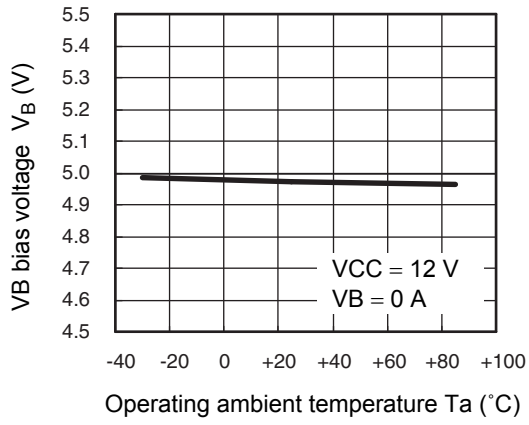
VB bias voltage vs.Power supply voltage



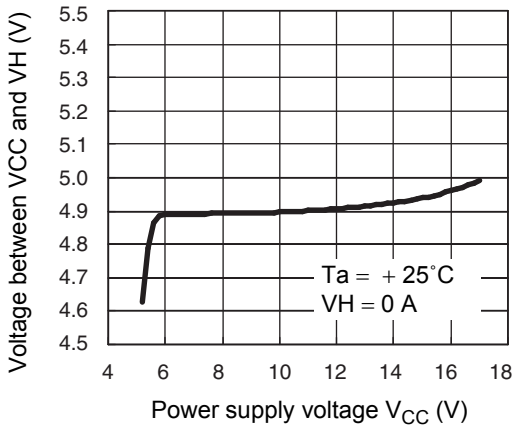
VB bias voltage vs.VB bias output current



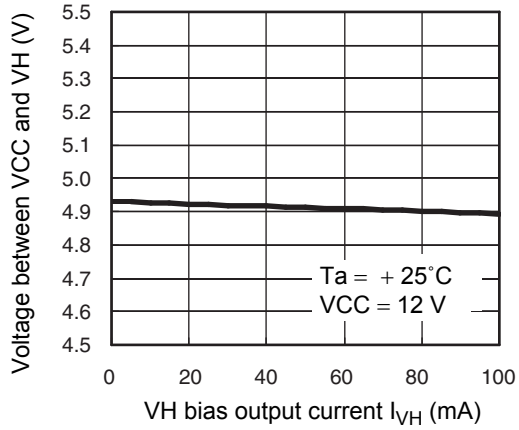
VB bias voltage vs.Operating ambient temperature



Voltage between VCC and VH vs.Power supply voltage



Voltage between VCC and VH vs.VH bias output current



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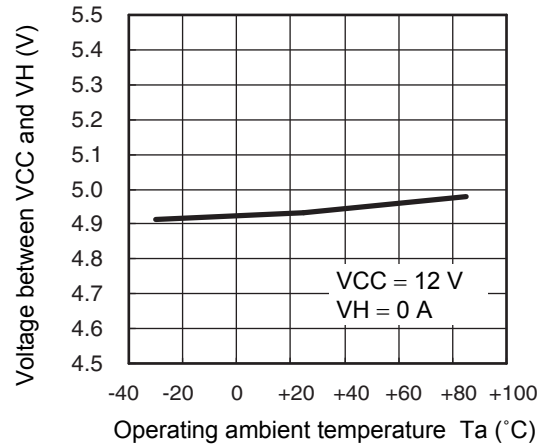
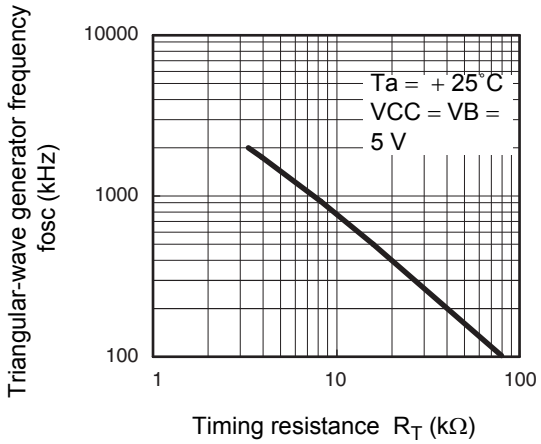
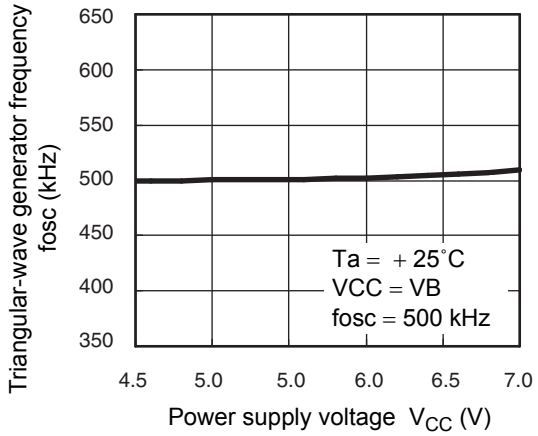
Voltage between VCC and VH vs. Operating ambient temperature



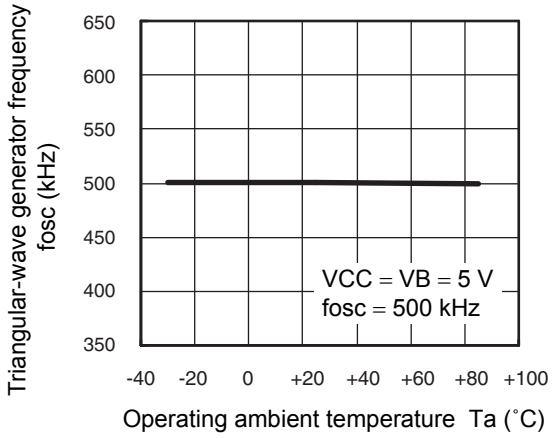
Triangular-wave generator frequency vs. Timing resistance



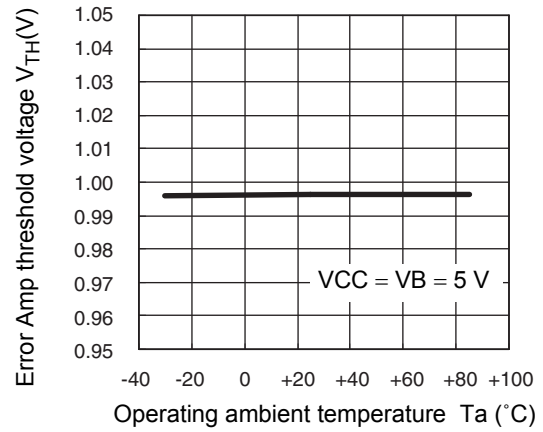
Triangular-wave generator frequency vs. Power supply voltage



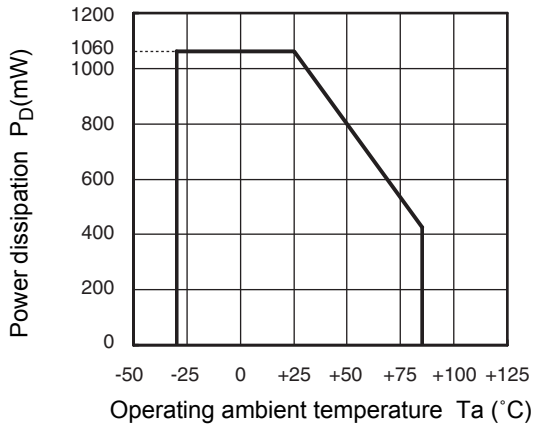
Triangular-wave generator frequency vs. Operating ambient temperature



Error Amp threshold voltage vs. Operating ambient temperature



Power dissipation vs. Operating ambient temperature



8. Functional Description

8.1 DC/DC Converter Block

8.1.1 Triangular Wave Oscillator Block (OSC)

The triangular wave oscillator block has a built-in capacitor for setting the oscillator frequency. The triangular wave is generated by connecting a resistor for selecting the frequency of the triangular wave to the RT pin (pin 5).The triangular wave is input internally to the PWM comparator in the IC.

8.1.2 Error Amplifier Block (Error Amp1, Error Amp2)

The error amplifiers (Error Amp1, Error Amp2) detect the DC/DC converter output voltages and output the PWM control signals. The output voltages can be set to an arbitrary level by externally connecting output voltage setting resistors to the error amplifier inverted input pins.
In addition, an arbitrary loop gain can be set by connecting a feedback resistor and capacitor from the error amplifier output (FB1 pin (pin 6), FB2 pin (pin 11)) to inverted input terminal (-INE1 pin (pin 7), -INE2 pin (pin 10)), enabling stable phase compensation of the system.Connecting a soft-start capacitor to the CSCP1 and CSCP2 pins (pins 8 and 9) prevents rush currents when the IC is turned on. Using an error amplifier for soft-start detection makes the soft-start time constant, independent of the output load of DC/DC converter.

8.1.3 PWM Comparator Block (PWM Comp.)

The PWM comparator circuit is a voltage-pulse width converter for controlling the output duty of the error amplifiers (Error Amp1, Error Amp2) depending on their output voltage.
The PWM comparator circuit compares the triangular wave generated by the triangular wave oscillator to the error amplifier output voltage and turns on the external output transistor during the interval in which the triangular wave voltage is lower than the error amplifier output voltage.

8.1.4 Output Block (Drive1-1, 1-2, Drive 2-1, 2-2)

The output circuit consists of CMOS drivers on both the high side and the low side, and is capable of driving an external P-ch MOS FET on the high side and an external N-ch MOS FET on the low side.

8.1.5 Power Supply Control Block (CTL)

The DC/DC converter can be put into standby mode by setting the CTL pin (pin 13) to the “L” level (the maximum power supply current in standby mode is 10 μA), and put into operating mode by setting the CTL pin (pin 13) to the “H” level.

Control Function Table

CTL	IC
L	OFF (Standby)
H	ON (Operating)

8.2 Protection Function

8.2.1 Soft-start Circuit

To prevent rush currents when the IC is turned on, soft-start can be performed by connecting soft-start capacitors (CSCP1 and CSCP2) to the CSCP1 and CSCP2 pins (pins 8 and 9). When CTL pin (pin 13) is driven to the “H” level and the IC begins operation (VCC ≥ UVLO threshold voltage), the external soft-start capacitors (CSCP1 and CSCP2) connected to the CSCP1 and CSCP2 pins (pins 8 and 9) are charged by the charging current obtained from the following formula.

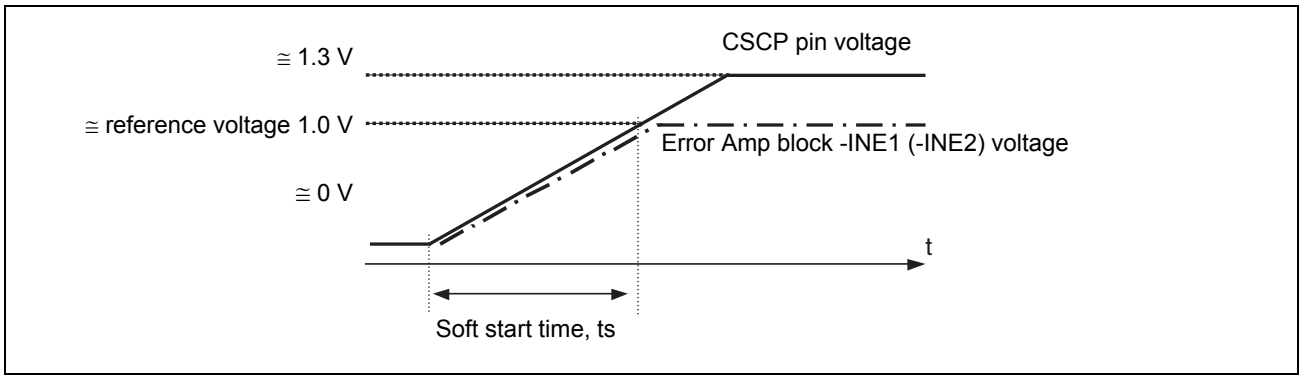
$I_{CS} \cong 5.4 \times 10^{-5} / R_T$

I_{CS} :Charge current [A]
R_T :Timing resistance [kΩ]

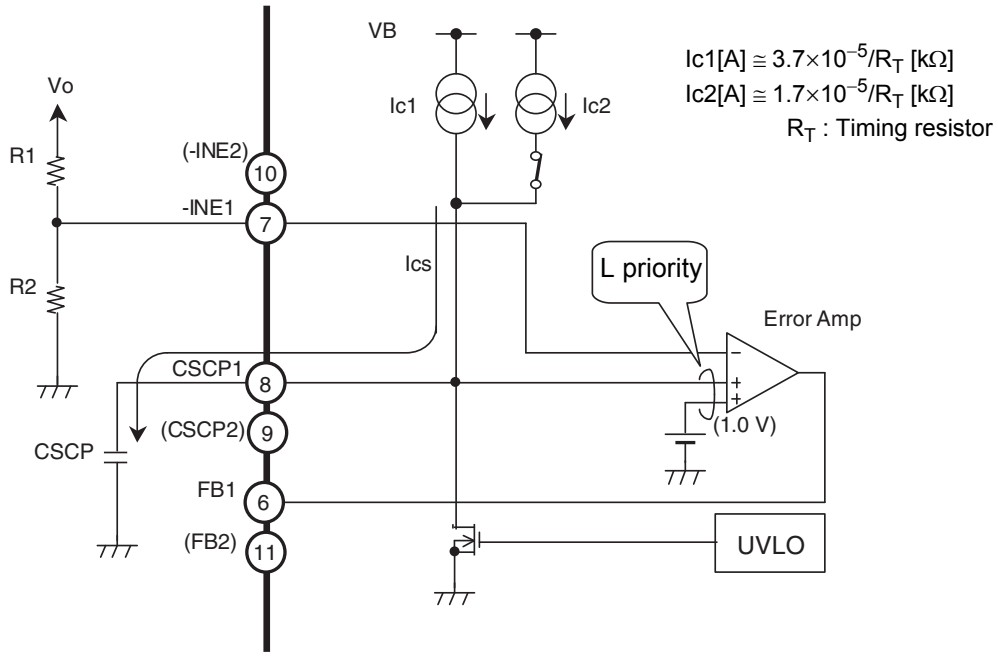
The error amplifier output (FB1 pin (pin 6), FB2 pin (pin 11)) is determined by comparing the voltages of the two non-inverted input pins (whichever of the internal 1.0 V reference voltage and the CSCP1 and CSCP2 pins (pin 8 and pin 9) has the lowest voltage) against the inverted input pin voltages (-INE1 pin (pin 7) voltage, -INE2 pin (pin 10) voltage). During the soft-start period, FB1 and FB2 are determined by comparing the internal 1.0 V reference voltage against the voltages of the CSCP1 and CSCP2 pins (pins 8 and 9), and the DC/DC converter output voltages rise in proportion to voltages of the CSCP1 and CSCP2 pins (pins 8 and 9) as the soft-start capacitors (CSCP1 and CSCP2) connected to the CSCP1 and CSCP2 pins (pins 8 and 9) are charged.
The soft-start time can be found from the following formula.

$ts \cong 0.019 \times CSCP \times R_T$

ts :Soft-start time (time to output voltage 100%) [s]
CSCP :Capacitance of CSCP pin [μF]
R_T :Timing resistance [kΩ]



Soft-start circuit



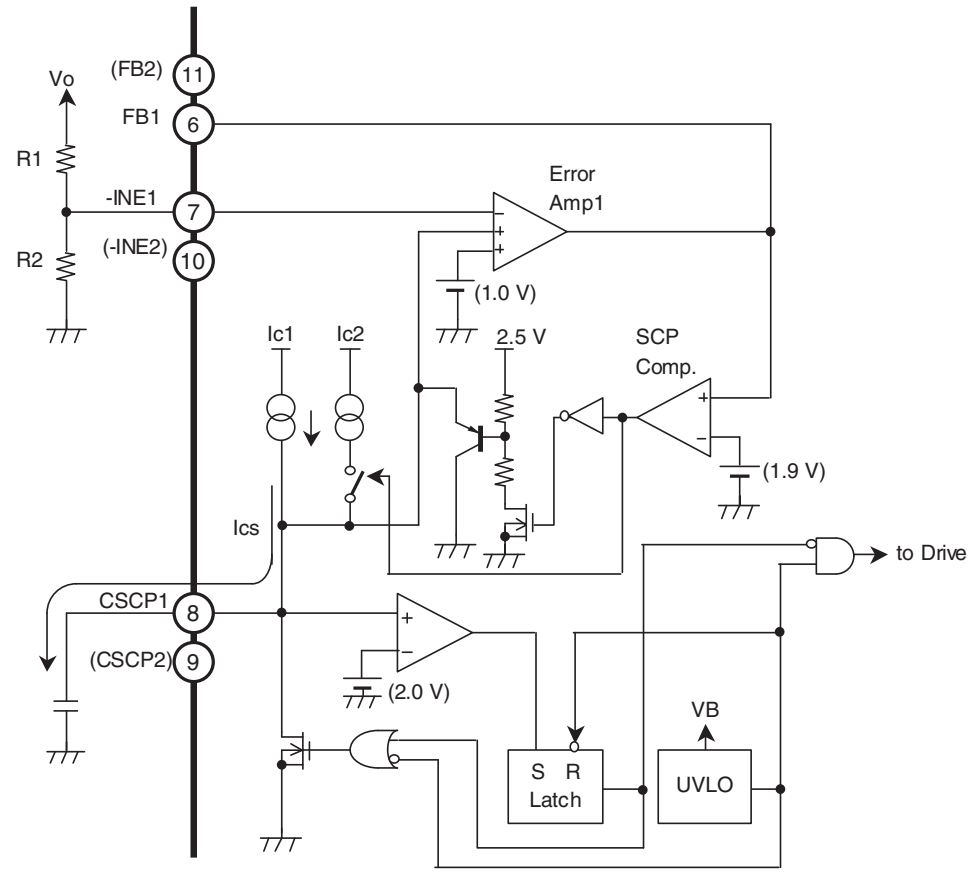
8.2.2 Timer-Latch Short-Circuit Protection Circuit

Each channel has a short-circuit detection comparator (SCP Comp1 and Comp2) that constantly compares the output level of the error amplifier against the reference voltage. While the DC/DC converter load conditions remain stable, the error amplifier output does not change and the short-circuit protection comparator remains in an equilibrium state. At this time, the CSCP1 and CSCP2 pins (pins 8 and 9) maintain the voltage from when the soft-start finished (about 1.3 V). If the output voltage of the DC/DC converter falls drastically due to a short-circuit or other load conditions, the output voltage of the error amplifier rises 1.9 V or more, and the external CSCP1 and CSCP2 capacitors are further charged. When the CSCP1 or CSCP2 capacitors are charged to about 2.0 V, a latch is set that turns off the external P-ch/N-ch MOSFETs (dead time is set to 100%). At this time, the latch input is closed and the CSCP1 and CSCP2 pins (pins 8 and 9) are held at the “L” level. Once the protection circuit has been activated, it can be reset by allowing the VB pin (pin 4) voltage to 3.8 V (minimum) or loss by turning the power off and on again.

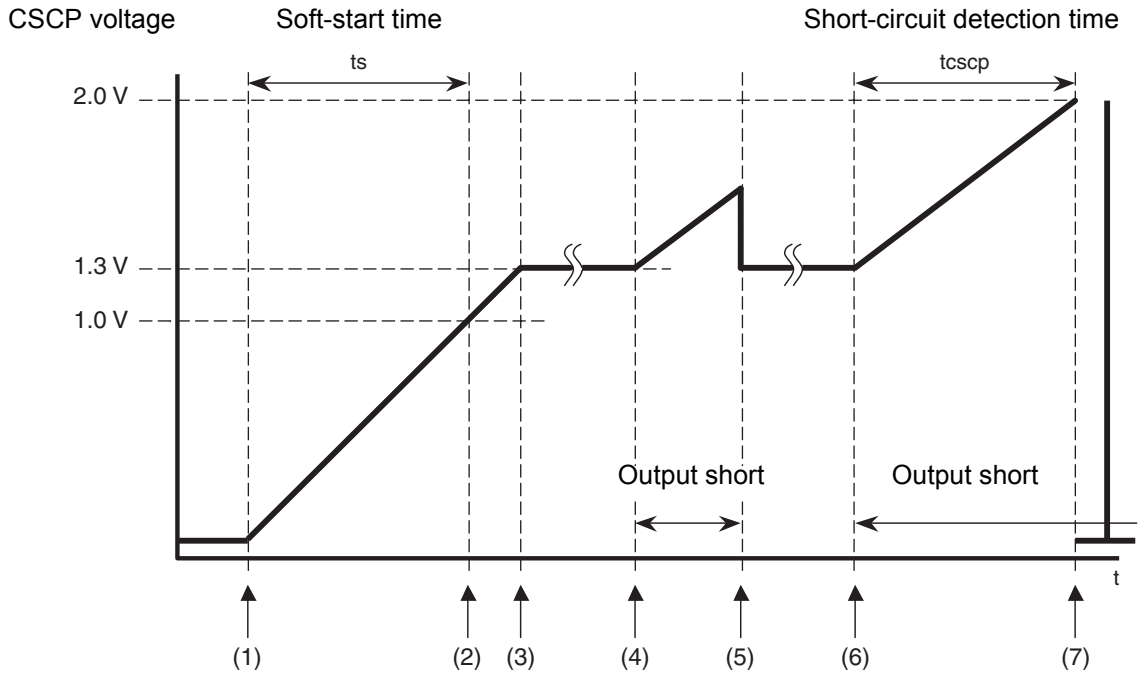
$t_{CSCP} \cong 0.019 \times CSCP \times R_T$

t_{CSCP} :Short-circuit detection time [s]
CSCP :Capacitance of CSCP pin [μF]
R_T :Timing resistance [kΩ]

Timer-latch short-circuit protection circuit



Soft-start and short-circuit protection timing chart



1. When the CTL pin (pin 13) is set to the “H” level and the IC becomes active, the voltages of the CSCP1 and CSCP2 pins (pins 8 and 9) rise due to the capacitors attached externally to the CSCP1 and CSCP2 pins (pins 8 and 9) being charged. During this time, Error Amp1 and Error Amp2 are controlled by the CSCP1 and CSCP2 pins (pins 8 and 9) and the -INE1 and -INE2 pins (pins 7 and 10) inputs, thus performing a soft-start.
2. When the CSCP1 and CSCP2 pins (pins 8 and 9) reach 1 V or more, Error Amp1 and Error Amp2 become controlled by the internal reference voltage (1 V) and the -INE1 and -INE2 pin (pins 7 and 10) inputs, and the output voltage is held at a constant level.
3. The CSCP1 and CSCP2 pins (pins 8 and 9) are clamped to about 1.3 V.
4. When there is a short circuit in the load and the error amplifier output becomes 1.9 V or more, the short-circuit protection comparator (SCP Comp.) is activated and the CSCP1 and CSCP2 capacitors are charged further.
5. If the short-circuit in the load is cleared within the short-circuit detection time t_{CSCP}, the CSCP1 and CSCP2 pins (pins 8 and 9) return to the clamping voltage of about 1.3 V.
6. When there is a short-circuit in the load and the error amplifier output becomes 1.9 V or more, the short-circuit protection comparator (SCP Comp.) is activated and the CSCP1 and CSCP2 capacitors are charged further.
7. The latch is set when the load short-circuit is not released even if short-circuit detection time t_{CSCP} passes, external MOS FET P-ch/N-ch are turned off, and the CSCP1,CSCP2 pins (pins 8 and 9) are hold at “L” level.

Notes :

- The output is stopped by the short-circuit protection (SCP) function when the DC/DC output is short-circuited to GND etc. However, care needs to be taken because the short-circuit protection (SCP) function will not stop the output when a half short-circuit occurs. Measures such as placing a fuse in the input can be used for this situation. [Half short-circuit refers to a short-circuit condition where an overcurrent flows, but it is not sufficient to reduce the output voltage.]
- In the event that an output short current flows that exceeds the capacity of the input power supply, the power supply voltage may drop. If the power supply voltage at this time drops below 3.8 V, the output is stopped by the under voltage lockout protection circuit (UVLO). However, once the input power supply voltage recovers after the output has been stopped, the output will begin again. Care needs to be taken because this situation may result in a repeating cycle of “short-circuit → power-supply voltage drop → output stop → power-supply voltage recovery → output start → short-circuit”. There are putting a fuse in the input etc. as measures.
- Notes the short-circuit protection (SCP) function when the DC/DC converter is started/stopped. The output may also be stopped by the short-circuit protection (SCP) function under the following conditions.
  - Operations that act on the input power supply and the CTL pin (for example, shorting the input power supply to the CTL pin).
  - During the transition period when the input power supply voltage (V_{IN}) is changing (such as when the input power supply is turned on or turned off), the condition is met that input power supply voltage (V_{IN}) < output setting voltage (V_O).

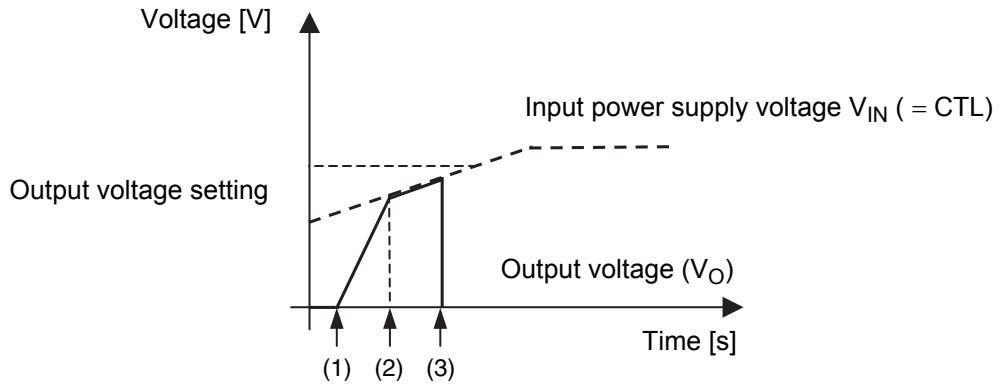
Although this is normal IC operation, as an example of startup of the IC, the output may be stopped due to the following process.

(1) DC/DC converter output begins when V_{IN} (= VB) > UVLO threshold voltage.

(2) A period of time occurs where the input power supply voltage (V_{IN}) < the output voltage setting (V_O), and the duty cycle becomes 100% on. The error amplifier output rises above 1.9 V due to the feedback control.

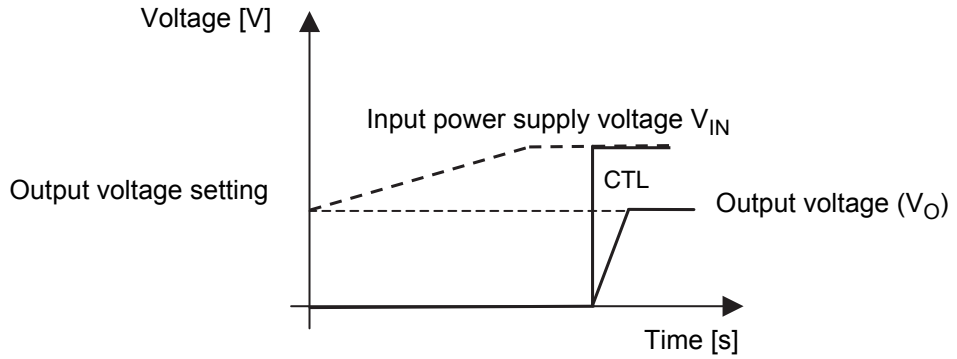
(3) The output is stopped after the short-circuit detection time has elapsed.

Example where the output stops when the DC/DC converter is activated by the input power supply (example of output stopped by SCP during startup)



In this case, the output can be prevented from being stopped by the SCP function during startup by controlling the CTL pin independently.

Example of the DC/DC converter being started by the CTL pin



Furthermore, when turning off the input power supply, set the CTL pin to “L” before turning off the input power supply.

8.2.3 Under Voltage Lockout Protection Circuit (UVLO)

A drop in the power supply voltage may cause the IC to malfunction, resulting in breakdown or degradation of the system. To prevent such malfunctions, the under voltage lockout protection circuit detects decreases in VB voltage due to the power supply voltage, and locks, the OUT1-1 pin (pin 2) and OUT2-1 pin (pin 15) at the “H” level and the OUT1-2 pin (pin 3) and OUT2-2 pin (pin 14) at the “L” level. The system is restored if the VB voltage rises above the threshold voltage of the under voltage lockout protection circuit.

Function Table When the Protection Circuit (UVLO) is Operating

When the UVLO circuit is operating (the VB voltage is below the UVLO threshold voltage), the following pins are fixed at the following logic levels.

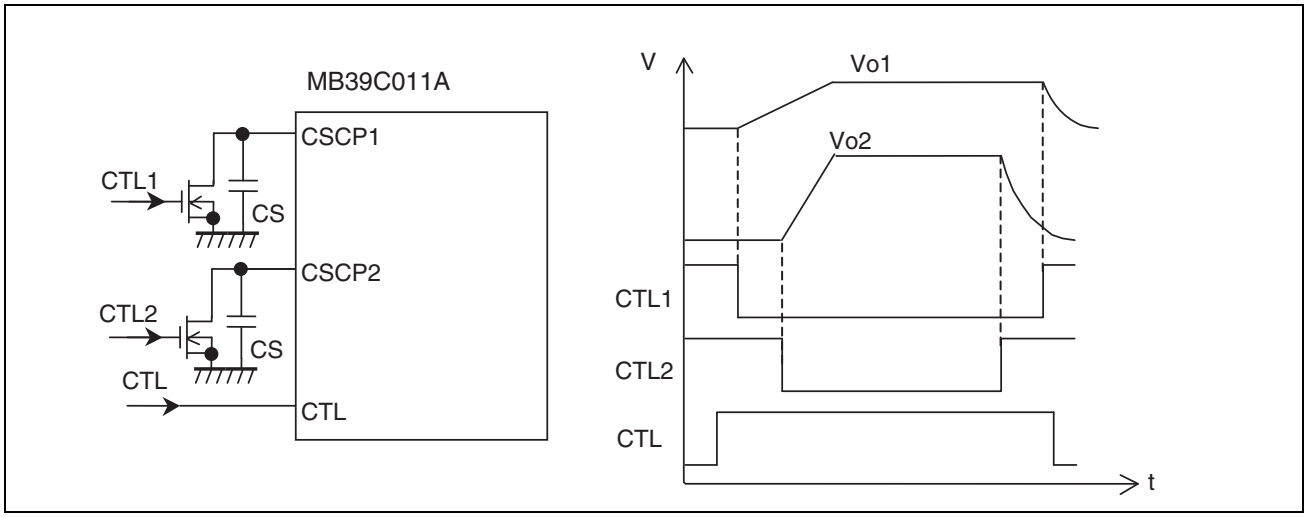
OUT1-1	OUT1-2	OUT2-1	OUT2-2	CSCP1	CSCP2
H	L	H	L	L	L

8.2.4 Operation When CTL is Turned On and Off

When CTL is turned on, the internal reference voltages VR1 and VB begin to rise. When VB exceeds the threshold voltage (VTH) of UVLO (under voltage lockout protection circuit), UVLO is released, and the output drive circuits of each channel are allowed to operate.When CTL is off, the output drive circuit of each channel is locked in the full off state and the CSCP1 and CSCP2 pins (pins 8 and 9) are fixed at the “L” level, even if the UVLO circuit is in the clear state. When the internal reference voltages VR1 and VB begin to fall and when VB falls below the threshold voltage of the UVLO (under voltage lockout protection circuit), the UVLO circuit is activated.

8.2.5 Independent Control Of Each Channel

The on/off state of each output voltage can be controlled independently by externally connecting the CSCP1 and CSCP2 pins (pins 8 and 9) to the drain pin of an NMOS transistor or to an NMOS open drain pin of a microcontroller, etc. When the CSCP1 or CSCP2 pins (pins 8 and 9) is set to the “L” level by turning on the external NMOS transistor, the output voltage turns off. Furthermore, when the external NMOS transistor is turned off, the soft-start function begins and the output voltage turns on. Note that the internal operation of the IC continues when the output voltages are turned off using the CSCP1 and CSCP2 pins (pins 8 and 9). Set the CTL pin (pin 13) to the “L” level to enter standby mode (the maximum power supply current in standby mode is 10 μA).



9. Switching Scheme Selection

This device can operate even by a synchronous rectification and an asynchronous rectification. There is superiority or inferiority respectively. Select the switching type considering the features as a guide.

Switching type	Parts	Feature
Asynchronous rectification	P-ch FET + Fly-back diode	■ Superior cost advantages ■ Under large load currents and low output voltages, it is inefficient because generation of heat of the Fly-back diode (SBD) is large.
Synchronous rectification	P-ch FET + N-ch FET	■ Offers a balance between cost and efficiency. ■ Supports large load currents and low output voltages
	P-ch FET + N-ch FET + Fly-back diode	■ Emphasis on efficiency (particularly effective at high oscillator frequencies) ■ Supports large load currents and low output voltages ■ Because of the increased number of parts, the cost is a disadvantage.

10. Setting The Output Voltage

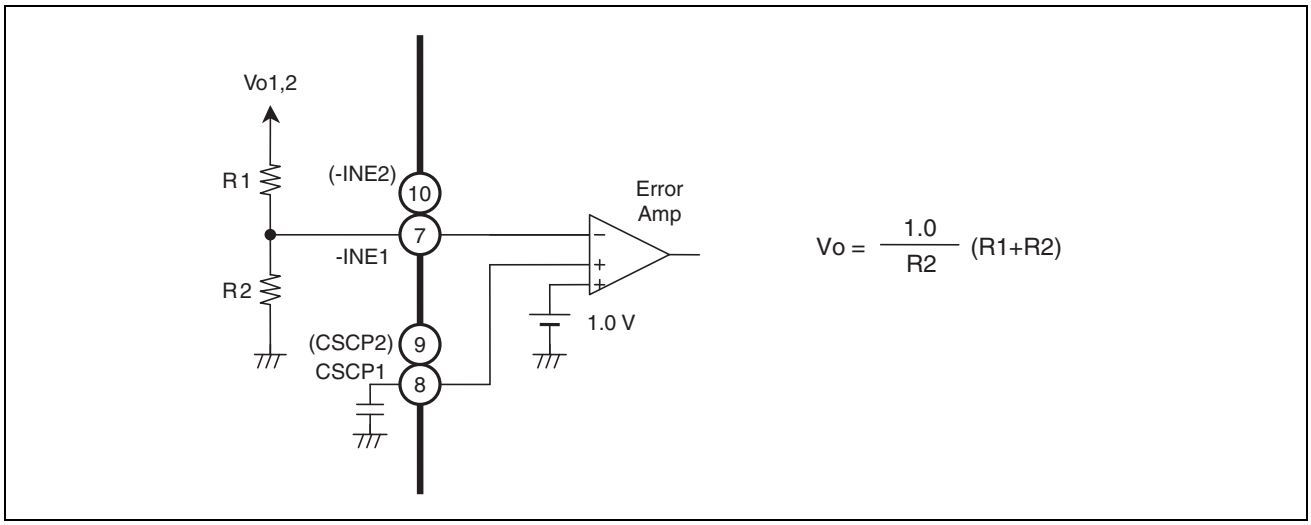
The output voltage can be set to an arbitrary value by the ratio of the feedback resistance to -INE1 (-INE2).

■Set the output voltage to a value higher than the reference voltage (1 V) of the Error Amp.

■Under usage conditions where the duty cycle is 30% or less, set $V_O1 < V_O2$ as much as possible.

$$D = \frac{V_O}{V_{IN}} \times 100$$

D :Duty cycle [%]
V_{IN} :Power supply voltage of switching system [V]
V_O :Output setting voltage [V]
R1, R2 :Output voltage setting resistors [Ω]



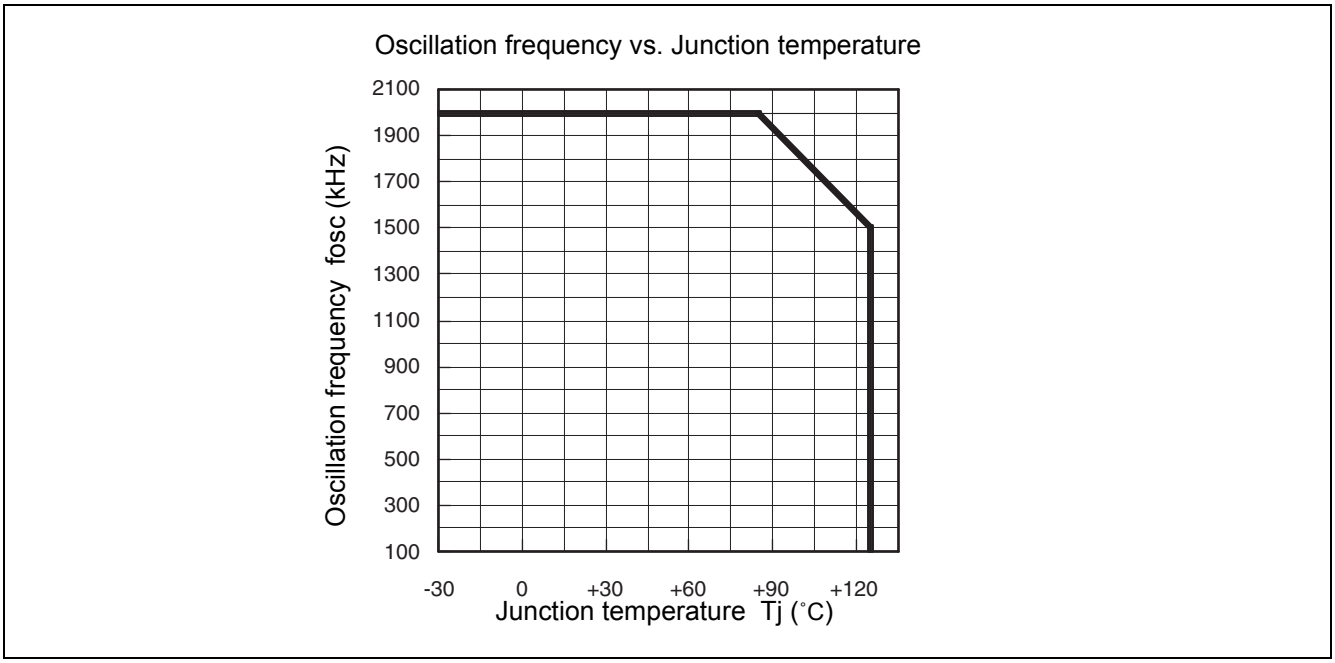
11. Setting The Triangular Oscillation Frequency

The triangular oscillation frequency is determined by the timing resistor (R_T) connected to the RT pin (pin 5).

$$fosc \cong \frac{0.001}{122.4 \times 10^{-12} \times R_T \times 10^3 + 96 \times 10^{-9}}$$

fosc : Triangular oscillation frequency [kHz]
R_T : Timing resistance [kΩ]

The upper limit on the oscillation frequency that can be set depends on the junction temperature and duty cycle. It is recommended that the device is used within the range shown in the following graph.



Note : Refer to " Power Dissipation and Thermal Design" for details on calculating the junction temperature.

11.1 Power Dissipation and Thermal Design

It is necessary to examine it for the use at a high power-supply voltage, a high oscillation frequency, and the high temperature. Also use within the range of "Oscillation frequency vs. Junction temperature".

The junction temperature can be investigated from the internal power dissipation of the IC.

The internal power dissipation of the IC (P_{IC}) is given by the following formula.

$P_{IC} = V_{CC} \times (I_{CC} + Qg \times fosc)$

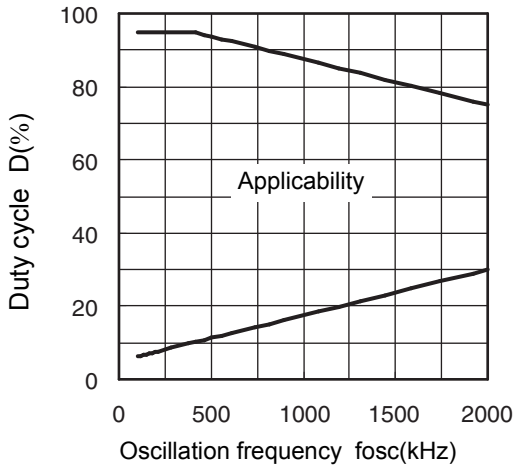
P_{IC} : Internal IC power dissipation [W]
V_{CC} : Power supply voltage (VIN : [V])
I_{CC} : Power supply current (3.3 mA Max)
Qg : Total electric charge (Vgs = 5 V) of all SW FET for 2ch [C]
fosc : Oscillation frequency [Hz]

The junction temperature is given by the following formula.

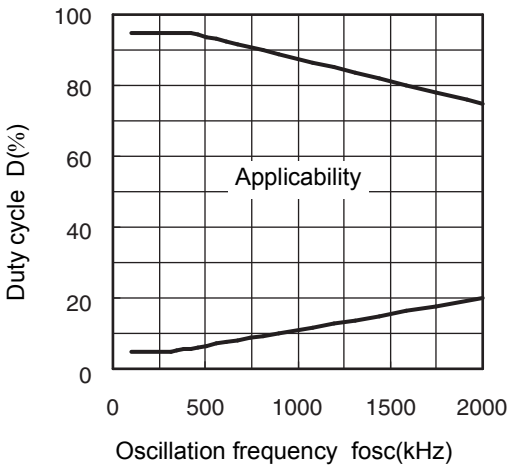
$Tj = Ta + \theta ja \times P_{IC}$

Tj :Junction temperature (+ 125˚C Max)
Ta :Ambient temperature [˚C]
θja :TSSOP-16 package thermal resistance (94˚C/W)
P_{IC} :Internal IC power dissipation [W]

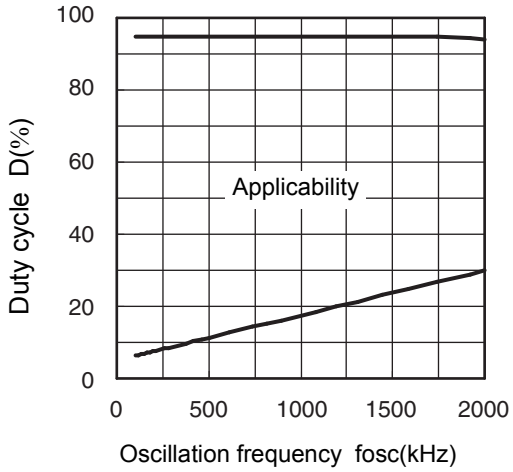
Synchronous rectification,
at 4.5 V ≤ V_{IN} ≤ 6 V (VCC = VB)
Duty cycle vs. Oscillation frequency



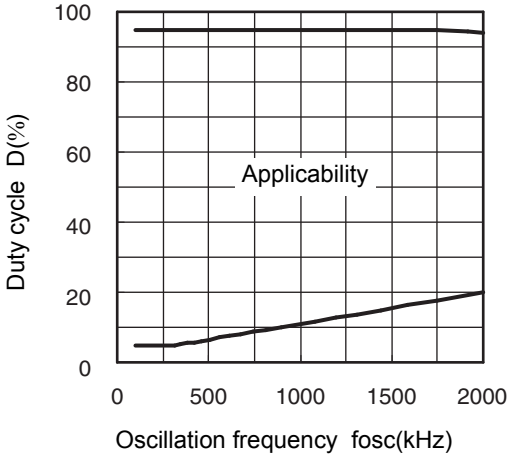
Synchronous rectification,
at V_{IN} > 6 V(VB = 5 V)
Duty cycle vs. Oscillation frequency



Asynchronous rectification,
at 4.5 V ≤ V_{IN} ≤ 6 V(VCC = VB)
Duty cycle vs. Oscillation frequency



Asynchronous rectification,
at V_{IN} > 6 V(VB = 5 V)
Duty cycle vs. Oscillation frequency



Notes :

■Refer to “Setting The Output Voltage” for details on calculating the duty cycle.

■When using the IC outside of the ranges shown in the above graphs, check for jitter and other adverse effects on the output voltage before use.

12. Setting The Soft-start And Short-circuit Detection Times

Set the soft-start time and the short-circuit detection time using the CSCP pins. Both become the same time.

$ts = t_{CSCP} \cong 0.019 \times CSCP \times R_T$

ts :Soft-start time (time to output voltage 100%) [s]
t_{CSCP} :Short-circuit detection time [s]
CSCP :CSCP pin capacitor [μF]
R_T :Timing resistance [kΩ]

13. VB Pin And VH Pin Connections In Condition Of Vcc Voltage

In the range of 4.5 V ≤ VCC ≤ 6.0 V, there is a chance that the VB voltage[1] and VH voltage[2] may drop due to the internal IC regulator saturating. As a result, there are drive voltage shortage and a bird clapper of SW FET. It is therefore recommended that the VB pin (pin 4) and VH pin (pin 16) are connected as shown in the “VB pin and VH pin connection table”.

[1]: Voltage between VB pin (pin 4) and GND pin (pin 12) : 5 V

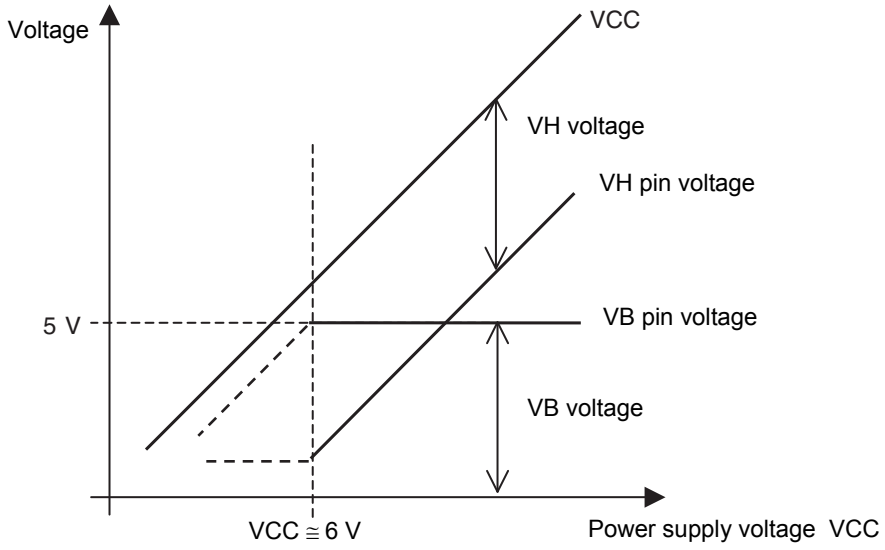
[2] : Voltage between VCC pin (pin 1) and VH pin (pin 16) : 5 V

VB pin and VH pin connection table

VCC condition	VB pin	VH pin
4.5 ≤ VCC ≤ 6 V	Connected to VCC	Connected to GND
6 V ≤ VCC ≤ 17 V	VB capacitor connection[4]	VH capacitor connection[4]
Used with VCC crossing 6 V[3](ex. 5 V ≤ VCC ≤ 7 V)	VB capacitor connection[4]	VH capacitor connection[4]

[3]: Check that the switching operation is functioning normally.
[4]: Refer to the connection of the VB pin (pin 4) and the VH pin (pin 16) in the “Block Diagram”.

Transition diagram of the VB voltage and VH voltage (VB pin: VB capacitor connection, VH pin: VH capacitor connection)

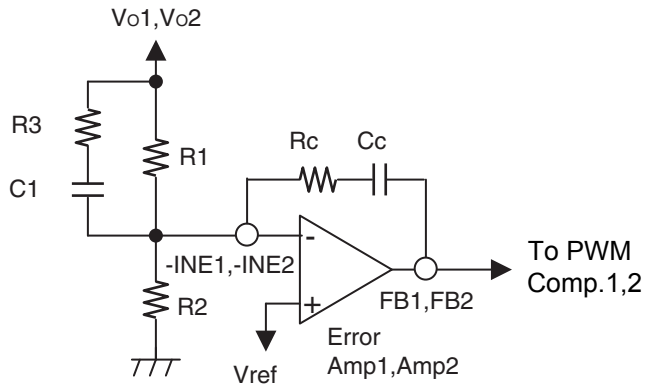


14. Design Of Phase Compensation Circuit

14.1 Phase compensation circuit when low ESR capacitor is used as output capacitor

When a low-ESR capacitor such as a ceramic capacitor is used as the output capacitor, it becomes easy to vibrate for a phase delay of the 180° to be generated due to the resonant frequency of the LC. In this case, it is common to use a phase compensation circuit that can advance the phase, such as a 2-pole/2-zero circuit.

2-pole/2-zero phase compensation circuit



Set the R3, Rc, C1, and Cc constants in the phase compensation circuit by using the following formula as a guide. As for frequency (f_{CO}) of crossover, in which the band width of the control loop of DC/DC is shown, height is excellent in the rapid response. However, vibration may be generated due to an insufficient phase margin. Although the

crossover frequency (f_{CO}) can be set to any value, the maximum value must be 1/2 of the oscillation frequency (f_{OSC}), or 1/5 of the oscillation frequency (f_{OSC}) as preferable. Furthermore, the crossover frequency (f_{CO}) should be set such that the phase margin is a minimum of 30°, or more than 45° as preferable.

$$R3 \cong \frac{f_{LC} \times R1}{2 \times f_{ESR} - f_{LC}}$$

R3, Rc : [Ω]
C1, Cc : [F]
f_{LC} : Resonant frequency [Hz] of the coil L [H] and output capacitor C [F]

$$f_{LC} = \frac{1}{2 \times \pi \sqrt{L \times C}}$$

$$C1 \cong \frac{1}{\pi \times f_{LC} (R1 + R3)}$$

f_{ESR} : Resonant frequency [Hz] of the output capacitor C [F] and ESR [Ω]

$$f_{ESR} = \frac{1}{2 \times \pi \times ESR \times C}$$

$$Rc \cong \frac{(R1//R3) \times f_{ESR} \times f_{CO}}{V_{IN} \times f_{LC}^2}$$

$$Cc \cong \frac{1}{2 \times \pi \times R_C \times f_{LC}}$$

f_{CO} : Crossover frequency (arbitrary setting) [Hz]
R1//R3 : Resistance of R1 and R3 connected in parallel [Ω]
V_{IN} : Switching system power supply voltage [V]

14.2 Notes on Phase Compensation Circuit Constants

Select the constants of the following three points and select the constant for the design of the phase compensation circuit when the large load sudden change, or the capacitor is connected to DC/DC converter operating.
In particular, if a capacitance much larger than the output capacitance of the DC/DC converter is connected by hard-switching while the DC/DC converter is operating, the output voltage may begin vibrating or the protection function may be activated, due to the sudden response. Note the following points.

14.2.1 Error Amp output (FB1 and FB2 pins) current capacity

The resistance constants of the phase compensation circuit need to be designed by considering the current capacities of the Error Amp outputs (FB1 and FB2 pins (pins 6 and 11)). Take the output source current (− 300 μA Max) of the Error Amp and the threshold voltage V_{T100} (1.7 V Typ) of the PWM Comp into consideration, select the resistance values such that the following formula is satisfied.

$$300\ [\mu A] > \frac{1.7\ [V]}{R1//R2//R3 + R_C}$$

R1//R2//R3 = Resistance of R1, R2 and R3 connected in parallel [Ω]
R_C : [Ω]

Although low resistance values may be desired to improve the noise immunity, the above formula may not be satisfied as a result. While it is ideal for each of the resistance values to satisfy the above formula, in this situation the values may be used after confirming that there are no problems when used under the rapidly varying load conditions.

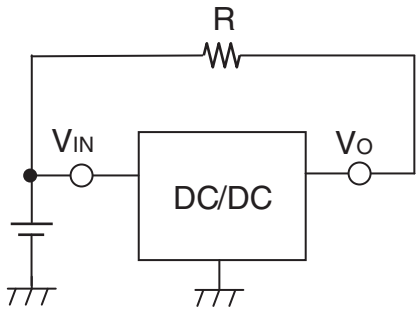
14.2.2 Phase Margin at the Output Load changes

Select phase compensation constants that ensure the phase margin when the output load (resistive load, capacitative load, inductive load) is connected.

14.2.3 Phase Margin at the rEverse Current Flow from the Output Pin

Under usage conditions where current from the DC/DC converter output (VO) pin flows by the load sudden change, select phase compensation constants that ensure the phase margin even when reverse current flow occurs.

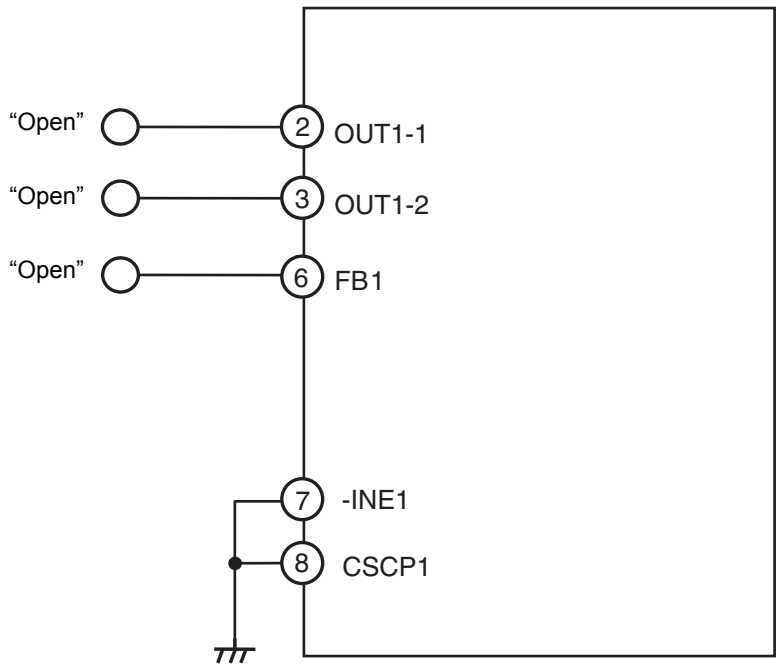
Example of measuring the phase margin during reverse current flow



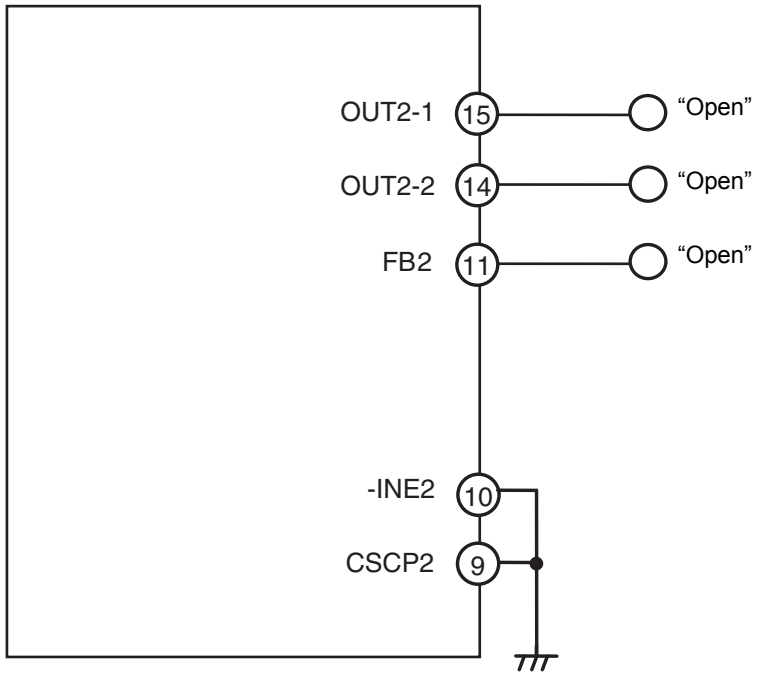
15. Handling the Unused Channel Pins when using a Single Channel

Although this device is a 2-channel DC/DC converter control IC, it is also able to be used as a 1-channel DC/DC converter by handling the pins of the unused channel as shown in the following diagram.

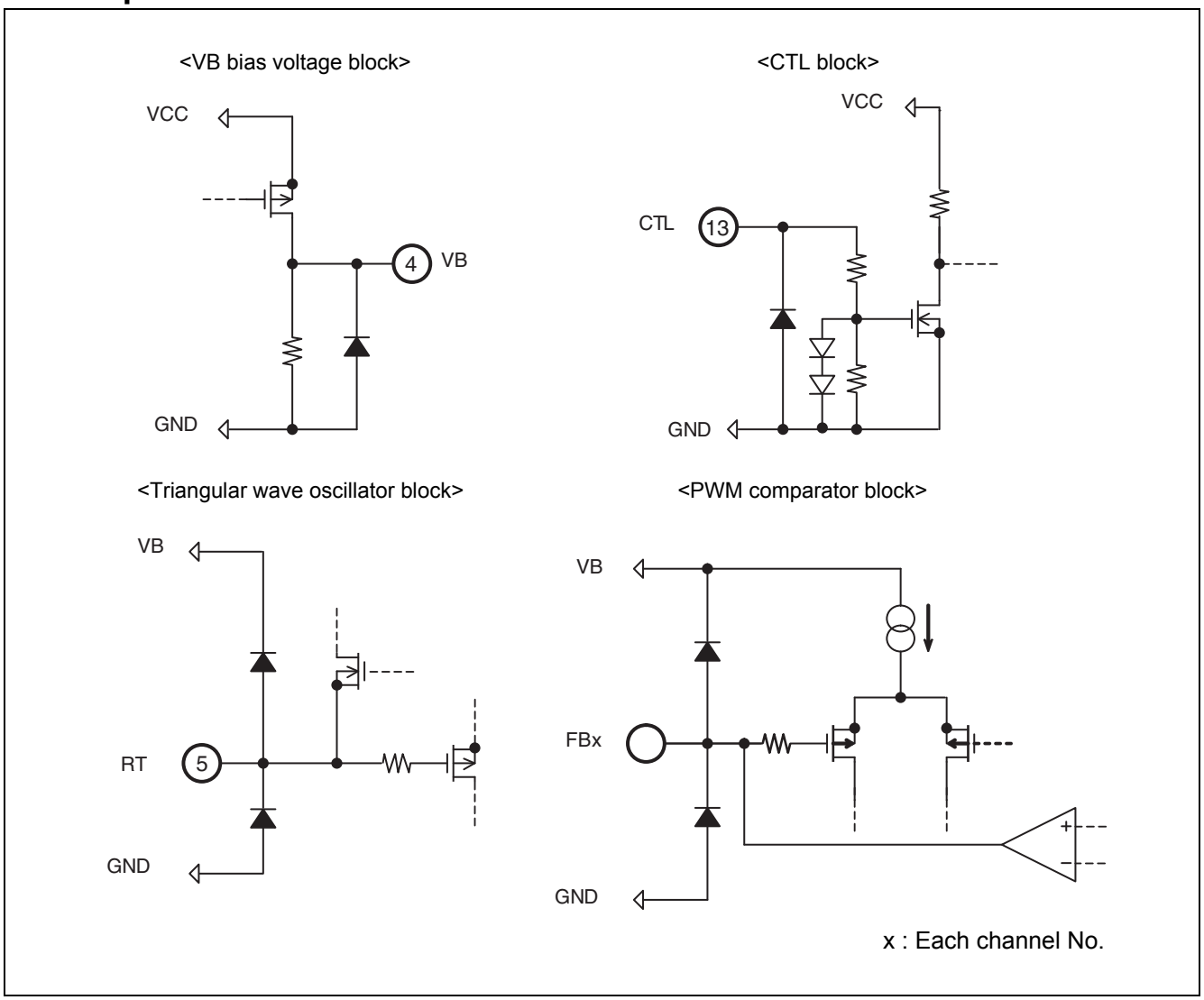
1. Connection when CH 1 is not used



2. Connection when CH 2 is not used



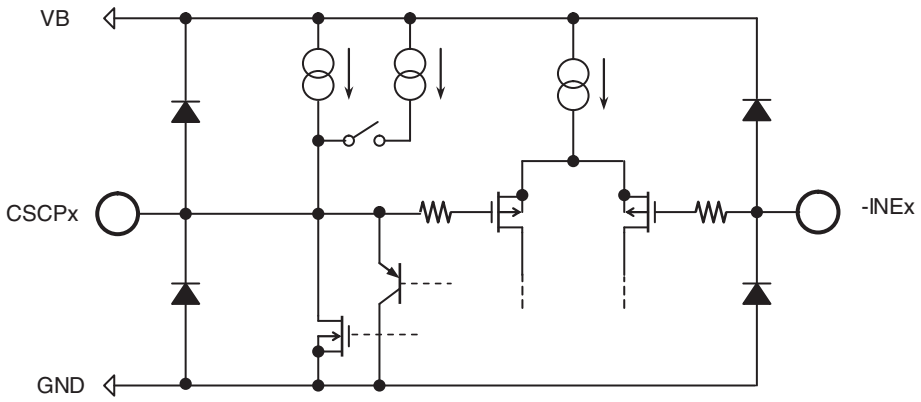
16. I/O Equivalent Circuit



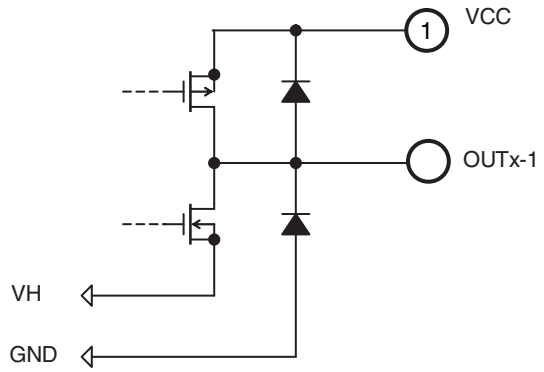
(Continued)

(Continued)

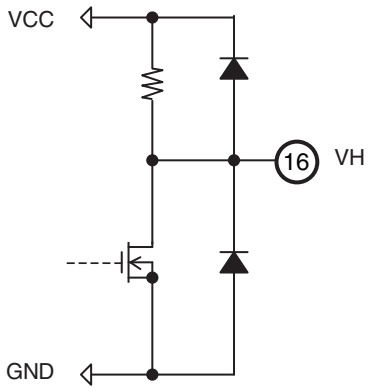
<Soft-start block, Error Amp block>



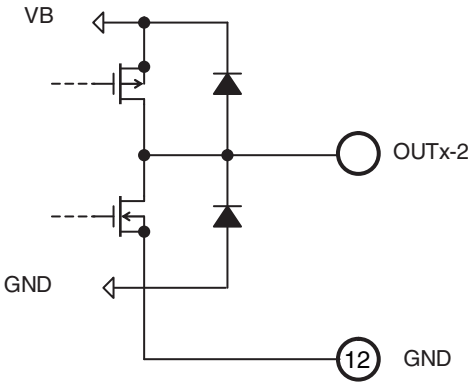
<Output block(OUTx-1)>



<VH bias voltage block>

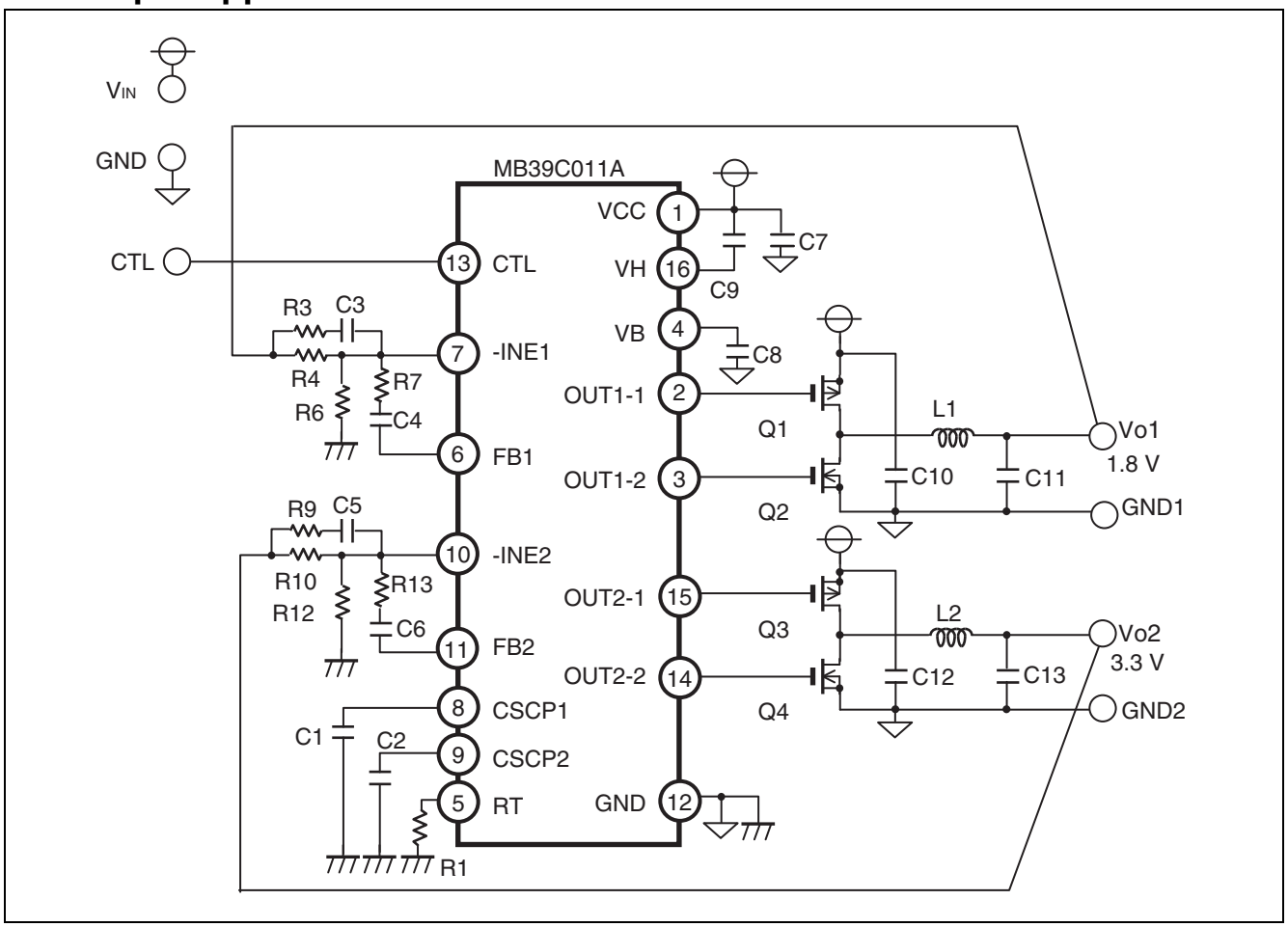


<Output block (OUTx-2)>



x : Each channel No.

17. Example Application Circuit



18. Parts List

Component	Item	Specification	Component	Item	Specification
Q1	P-ch FET	VDS = − 30 V, ID = − 4 A (Max)	C1	Ceramic condenser	0.015 μF (50 V)
Q2	N-ch FET	VDS = 30 V, ID = 5 A (Max)	C2	Ceramic condenser	0.015 μF (50 V)
Q3	P-ch FET	VDS = − 30 V, ID = − 4 A (Max)	C3	Ceramic condenser	100 pF (50 V)
Q4	N-ch FET	VDS = 30 V, ID = 5 A (Max)	C4	Ceramic condenser	470 pF (50 V)
R1	Resistor	16 kΩ	C5	Ceramic condenser	220 pF (50 V)
R3	Resistor	2 kΩ	C6	Ceramic condenser	2200 pF (50 V)
R4	Resistor	5.1 kΩ + 75 kΩ	C7	Ceramic condenser	0.1 μF (50 V)
R6	Resistor	100 kΩ	C8	Ceramic condenser	1 μF (16 V)
R7	Resistor	10 kΩ	C9	Ceramic condenser	1 μF (16 V)
R9	Resistor	1 kΩ	C10	Ceramic condenser	22 μF (25 V)
R10	Resistor	1.5 kΩ + 33 kΩ	C11	Ceramic condenser	33 μF (6.3 V)
R12	Resistor	15 kΩ	C12	Ceramic condenser	22 μF (25 V)
R13	Resistor	5.6 kΩ	C13	Ceramic condenser	33 μF (6.3 V)
L1	Inductor	3.3 μH (IDC = 6.7 A)	-	-	-
L2	Inductor	4.7 μH (IDC = 6 A)	-	-	-

19. Part Selection

19.1 Coil selection

As a rough guide, choose the inductance of the coil such that the peak-to-peak ripple current of the coil is less than 50% of the maximum load current. The inductance in this case is given by the following formula.

$$L \geq \frac{V_{IN} - V_O}{LOR \times I_{OMAX}} \times \frac{V_O}{V_{IN} \times fosc}$$

L : Coil inductance [H]
I_{OMAX} : Maximum load current [A]
LOR : 0.5
V_{IN} : Switching system power-supply voltage [V]
V_O : Output voltage setting [V]
fosc : Oscillation frequency [Hz]

When the IC is used with asynchronous rectification, it is recommended that the IC be used in the load current range where the coil current is continuous in order to ensure responsiveness to the load. For asynchronous rectification it is therefore recommended that the minimum value of the load current is used as the basis for setting the inductance value.

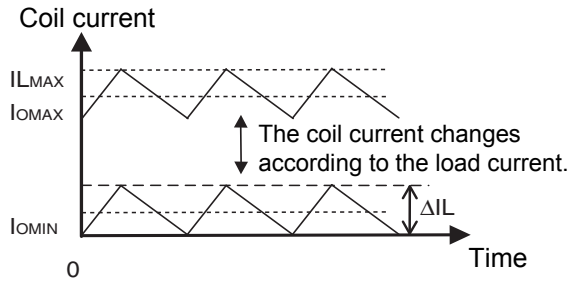
$$L \geq \frac{V_{IN} - V_O}{2 \times I_{OMIN}} \times \frac{V_O}{V_{IN} \times fosc}$$

L : Coil inductance [H]
I_{OMIN} : Minimum load current [A]
V_{IN} : Switching system power-supply voltage [V]
V_O : Output voltage setting [V]
fosc : Oscillation frequency [Hz]

The maximum value of the current flowing through the coil needs to be found in order to determine whether the current flowing through the coil is within the rated value. The maximum current flowing through the coil is given by the following formula.

$$I_{LMAX} = I_{OMAX} + \frac{\Delta IL}{2}$$

$$\Delta IL \geq \frac{V_{IN} - V_O}{L} \times \frac{V_O}{V_{IN} \times fosc}$$



IL_{MAX} : Maximum coil current [A]
I_{OMAX} : Maximum load current [A]
ΔIL : Coil ripple current peak to peak value [A]
L : Coil inductance [H]
V_{IN} : Switching system power-supply voltage [V]
V_O : Output setting voltage [V]
fosc : Oscillation frequency [Hz]

19.2 SW FET selection

The maximum value of the current flowing through the SW FET needs to be found in order to determine whether the current flowing through the SW FET is within the rated value. The maximum current flowing through the SW FET is given by the following formula.

$$I_{DMAX} \geq I_{OMAX} + \frac{\Delta IL}{2}$$

I_{DMAX} : Maximum SW FET drain current [A]
I_{OMAX} : Maximum load current [A]
ΔIL : Coil ripple current peak to peak value [A]

Furthermore, the power dissipation of the SW FET needs to be found in order to determine whether the power dissipation of the SW FET is within the rated value. The power dissipation of the SW FET is given by the following formula.

High side FET (P-ch MOS FET) power dissipation $P_{HiSideFET} = P_{Ron} + P_{SW}$

P_{R}on : High side FET (P-ch MOS FET) conduction loss $P_{Ron} = I_{OMAX}^2 \times \frac{V_O}{V_{IN}} \times Ron$

I_{OMAX} : Maximum load current [A]
V_{IN} : Switching system power supply voltage [V]
V_O : Output voltage [V]
Ron : High side FET ON resistance [Ω]

P_{SW} : High side FET (P-ch MOS FET) switching loss $P_{SW} = \frac{V_{IN} \times f_{OSC} (Ibtm \times tr \times Itop \times tf)}{2}$

V_{IN} : Switching system power supply voltage [V]
fosc : Oscillation frequency [Hz]
Ibtm : Bottom value of ripple current of coil [A]

$$Ibtm = I_{OMAX} - \frac{\Delta IL}{2}$$

Itop :Top value of ripple current of coil [A]

$$Itop = I_{OMAX} + \frac{\Delta IL}{2}$$

ΔIL : Coil ripple current peak to peak value [A]
tr : Turn-on time of High side FET [s]
tf : Turn-off time of High side FET [s]

tr and tf are simply obtained by the following formula.

$$tr = \frac{Qgd \times 4}{5 - Vgs\ (on)} \qquad tf = \frac{Qgd \times 4}{Vgs\ (on)}$$

Qgd : Quantity of charge between the gate and drain of High side FET [C]
Vgs(on) : Absolute value of voltage difference between the gate and source of the High side FET at Qgd [V]

Low side FET(N-ch MOS FET) conduction loss

$$P_{LoSideFET} = P_{Ron} = I_{OMAX}{}^2 \times \left(1 - \frac{V_O}{V_{IN}}\right) \times Ron$$

P_{Ron} : Low side FET conduction loss [W]
I_{OMAX} : Maximum load current [A]
V_{IN} : Switching system power supply voltage [V]
V_O : Output voltage [V]
Ron : Low side FET ON resistance [Ω]

To select SW FETs that offer good conversion efficiency, the High side FET in particular should select such that the switching loss is small (the power dissipated when the SW FET changes between ON and OFF). However, because there is generally a trade-off between switching loss and conduction loss, this balance needs to be considered when making the selection.
As a guide, select FETs such that the total Qg of the SW FETs is as follows.

$$QgHiSideFET < \frac{0.04}{fosc} \qquad QgLoSideFET < \frac{0.04}{fosc}$$

QgHiSideFET : Sum total electric charge of the CH1 and CH2 High side FETs [C]
QgLoSideFET : Sum total electric charge of the CH1 and CH2 Low side FETs [C]
fosc : Oscillation frequency [Hz]

The SW FETs used with this device typically have a drive voltage of 4 V. Although there are FETs that support a drive voltage of less than 4 V, low drive voltage FETs generally have a larger Qg even at equal value of Ron, the efficiency lowers. If a FET with a low drive voltage is used, check that the low side FET does not self turn-on and that the dead-time is secured under the usage conditions.

19.3 Fly-back Diode Selection

Select a Schottky barrier diode (SBD) that has a small forward voltage drop.

The peak current flowing through the Fly-back diode needs to be found in order to determine whether the current flowing through the Fly-back diode is within the rated value. When the DC/DC converter IC is used with asynchronous rectification, the maximum current through the Fly-back diode is given by the following formula.

$$I_f \geq I_{OMAX} \frac{\Delta IL}{2}$$

I_f : Forward current [A]
I_{OMAX} : Maximum load current [A]
ΔIL : Coil ripple current peak to peak value [A]

Furthermore, the power dissipation of the Fly-back diode needs to be found in order to determine whether the power dissipation of the Fly-back diode is within the rated value. The power dissipation of the Fly-back diode is given by the following formula.

$$P_{SBD} = I_{OMAX} \times (1 - \frac{V_O}{V_{IN}}) \times Vf$$

P_{SBD} : Fly-back diode power dissipation [W]
I_{OMAX} : Maximum load current [A]
V_{IN} : Switching system power supply voltage [V]
V_O : Output voltage [V]
Vf :Forward voltage [V]

When the DC/DC converter is used with synchronous rectification, the length of time that the current flows through the Fly-back diode is limited to the synchronous rectification period (dead time). For example, at an oscillating frequency of 500 kHz, the proportion of time that current flows is less than 5%. Therefore, select that Fly-back diode current does not exceed the peak forward surge current (IFSM) rated value. The peak forward surge current value of the SBD is given by the following formula.

$$I_{FSM} \geq I_{OMAX} + \frac{\Delta IL}{2}$$

I_{FSM} : Peak forward surge current value of Fly-back diode [A]
I_{OMAX} : Maximum load current [A]
ΔIL : Coil ripple current peak to peak value [A]

19.4 Output capacitor selection

Because the ripple voltage increases if the ESR is large, a low ESR capacitor needs to be used in order to reduce the ripple voltage. However, using a capacitor with a low ESR has a large effect on the phase characteristics of the loop, and care needs to be taken to prevent the system from losing stability. Furthermore, the capacitor that is used should have sufficient tolerance for the ripple current.

If taking into account the switching ripple voltage, the minimum necessary capacitance is given by the following formula.

$$C_O \geq \frac{1}{2\pi \times fosc \times (\Delta V_O / \Delta IL - ESR)}$$

ESR : Series resistance element of output capacitance [Ω]
ΔV_O : Switching ripple voltage [V]
ΔIL : Coil ripple current peak to peak value [A]
C_O : Output capacitance [F]
fosc : Oscillation frequency [Hz]

When a capacitive load is connected, it is recommended that the DC/DC converter output capacitor have the same capacitance as the load capacitance.

The allowable ripple current of the output capacitor is given by the following formula.

$$Irms \geq \frac{\Delta IL}{2\sqrt{3}}$$

Irms : Allowable ripple current (Root-mean-square value) [A]
ΔIL : Coil ripple current peak to peak value [A]

19.5 Input capacitor selection

Select an input capacitor that has as small an ESR as possible. Ceramic capacitors are ideal. If a large capacitance is required that cannot be provided by a ceramic capacitor, use a polymer capacitor or a tantalum capacitor with a low ESR. Furthermore, the capacitor that is used should have sufficient tolerance for the ripple current.

The allowable ripple current is given by the following formula.

$$Irms \geq I_{OMAX} \frac{\sqrt{V_O (V_{IN} - V_O)}}{V_{IN}}$$

Irms : Allowable ripple current (Root-mean-square value) [A]
I_{OMAX} : Maximum load current [A]
V_{IN} : Switching system power supply voltage [V]
V_O : Output voltage [V]

19.6 VB pin capacitor

Although the VB pin capacitor typically has a capacitance of 1 μF, this needs to be adjusted if the SW FET being used has a large Qg.

The following formula provides a guide to the lower limit of the VB pin capacitor. If this lower limit exceeds 1 μF, use the formula as a guide to set the capacitance.

$$CVBmin \geq 0.1 \times QgLoSideFET$$

CVBmin	: Lower limit of VB pin capacitor [μF]
QgLoSideFET	: Sum total electric charge of CH1 and CH2 Low side FETs [nC]

19.7 VH pin capacitor

The VH pin capacitor typically has a capacitance of 1 μF (when the VB pin capacitor ≤ 1 μF). However, this needs to be adjusted, if the VB pin capacitor exceeds 1 μF or if the SW FET being used has a large Qg.

The following formula provides a guide to the lower limit of the VH pin capacitor. If this lower limit exceeds 1 μF, use the formula as a guide to set the capacitance.

Large one either of

$$CVHmin \geq 0.01 \times QgHiSideFET \text{ or } CVHmin \geq CVB$$

CVHmin	: Lower limit of VH pin capacitor [μF]
QgHiSideFET	: Sum total electric charge of CH1 and CH2 high side FETs [nC]
CVB	: Capacitance of VB pin capacitor [μF]

20. PCB Layout

Consider the following points when designing the PCB layout :

■Make the input capacitor (Cin), SW FET, Fly-back diode (SBD), coil (L), and output capacitor (Cout) connections on the surface as much as possible, and avoid making the connections with the through-holes.

■Take the most care with the loop consisting of the input capacitor (Cin), SW FET, and Fly-back diode (SBD), and make the current loop as small as possible.

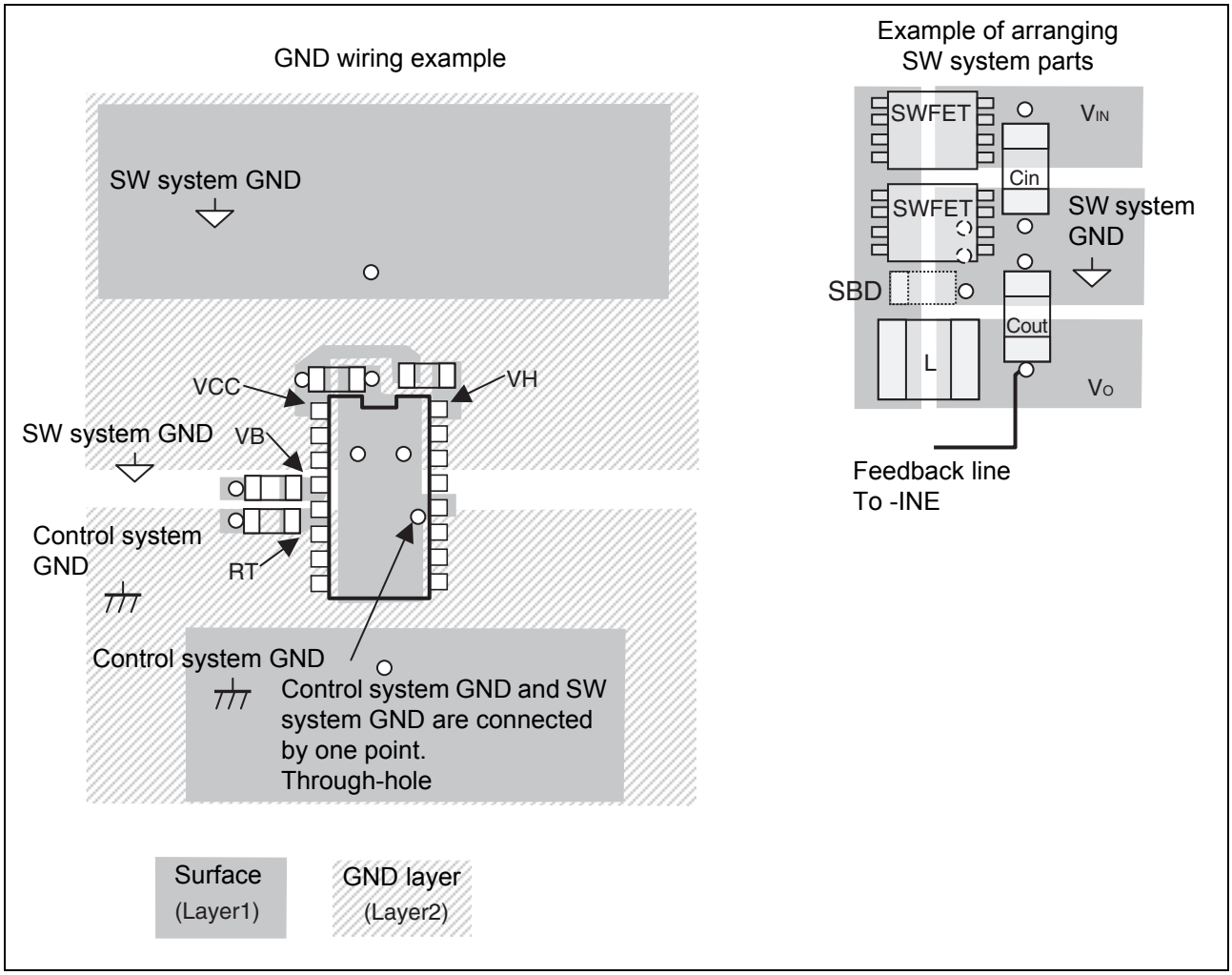
■Create through-hole directly next to the GND pins of the input capacitor (Cin), SW FET, Fly-back diode (SBD), and output capacitor (Cout), and connect these to the SW system GND inner layer.

■Large currents flow momentarily through the wiring of the OUTx-x pins that are connected to the SW FET gates. Use a wiring width of about 0.8 mm as a guide, and make the wiring as short as possible.

■Arrange the bypass capacitors that are connected to the VCC, VB, and VH pins (pins 1, 4, and 16) near the pins as possible. Furthermore, connect the GND pin of the VCC and VB by-pass capacitor with a nearest GND pin of the IC. (Create a through-hole directly next to the GND pin of the IC (pin 12) and the GND pins of the bypass capacitors to reinforce the connection to the inner ground layer).

■The wiring for the -INE1, -INE2, FB1, FB2, and RT pins (pins 7, 10, 6, 11, and 5) is sensitive to noise and should be made as short as possible. Furthermore, the feedback line from the output (V_O) should be kept as far away from SW system components as possible.

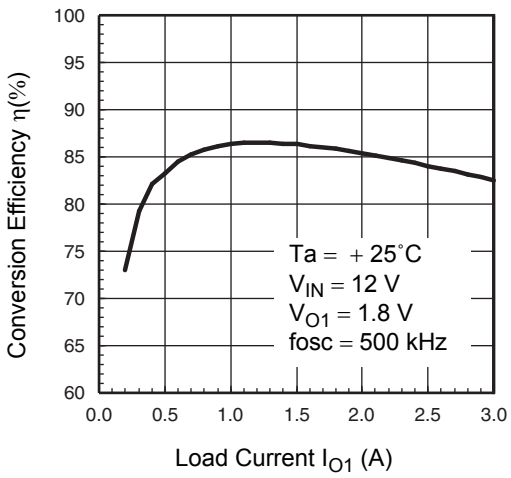
■Create as much ground plane on the side where the IC is mounted as possible. To prevent creating a large current path to the control system GND, connect this to the PGND (SW system GND) at a single point.



21. Reference Data

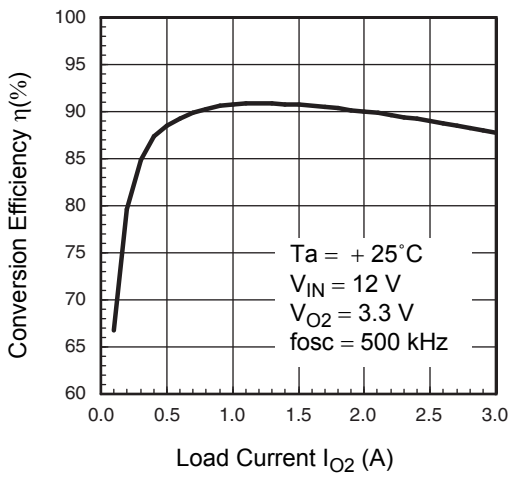
CH1

Conversion Efficiency vs. Load Current

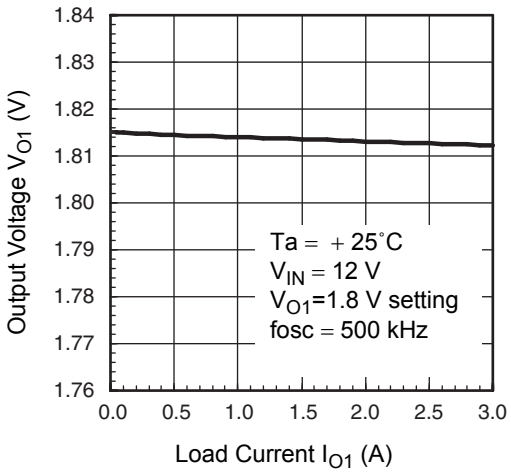


CH2

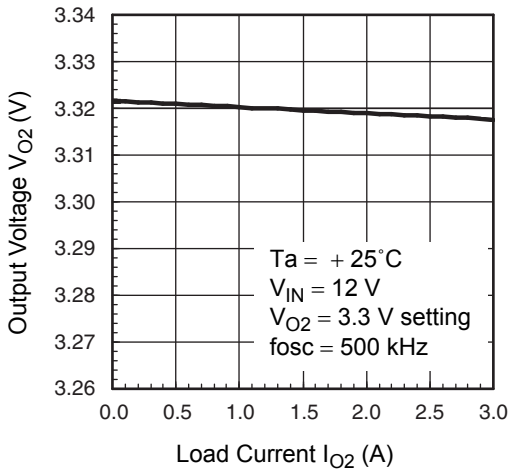
Conversion Efficiency vs. Load Current



Output Voltage vs. Load Current



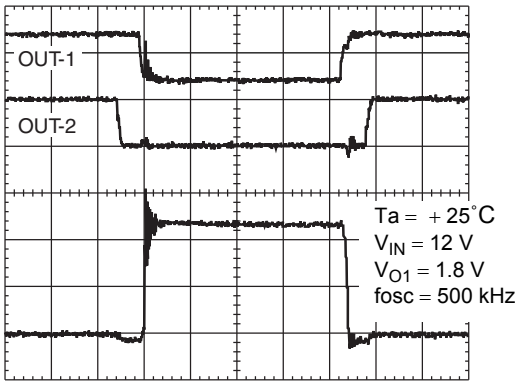
Output Voltage vs. Load Current



(Continued)

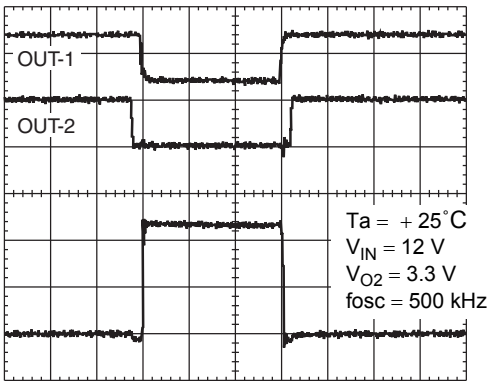
(Continued)

CH1 Switching Wave Form



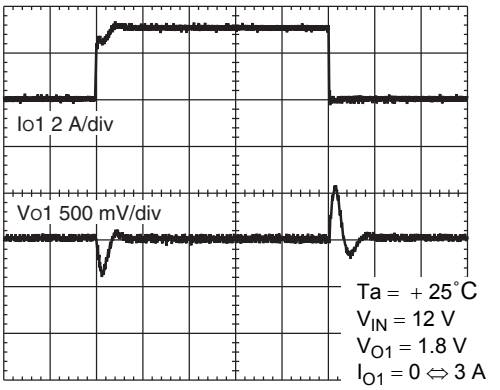
5 V/div, 80 ns/div

CH2 Switching Wave Form



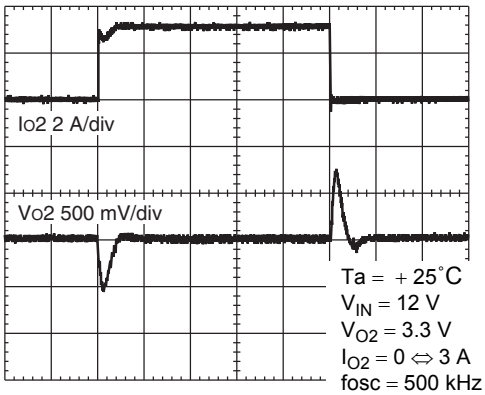
5 V/div, 200 ns/div

CH1 Sudden Load Variation Waveform



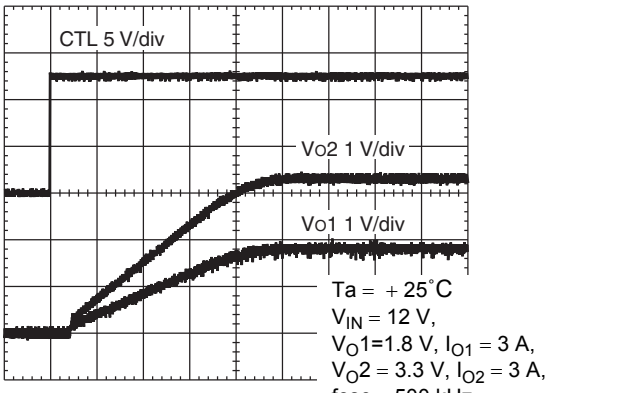
40 µs/div

CH2 Sudden Load Variation Waveform



40 µs/div

CTL Startup Waveform



1 ms/div

22. Usage Precaution

22.1 Do not configure the IC over the maximum ratings

If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions can have a bad effect on the reliability of the LSI.

22.2 Use the device within the recommended operating conditions

The recommended operating conditions are under which the LSI is guaranteed to operate. The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

22.3 Printed circuit board ground lines should be set up with consideration for common Impedance

22.4 Take appropriate measures against static electricity

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ between body and ground.

22.5 Do not apply negative voltages

The use of negative voltages below − 0.3 V may create parasitic transistors on LSI lines, which can cause malfunctions.

23. Ordering Information

Part number	Package	Remarks
MB39C011APFT-❑❑❑E1	16-pin plastic TSSOP (FPT-16P-M07)	Lead-free version

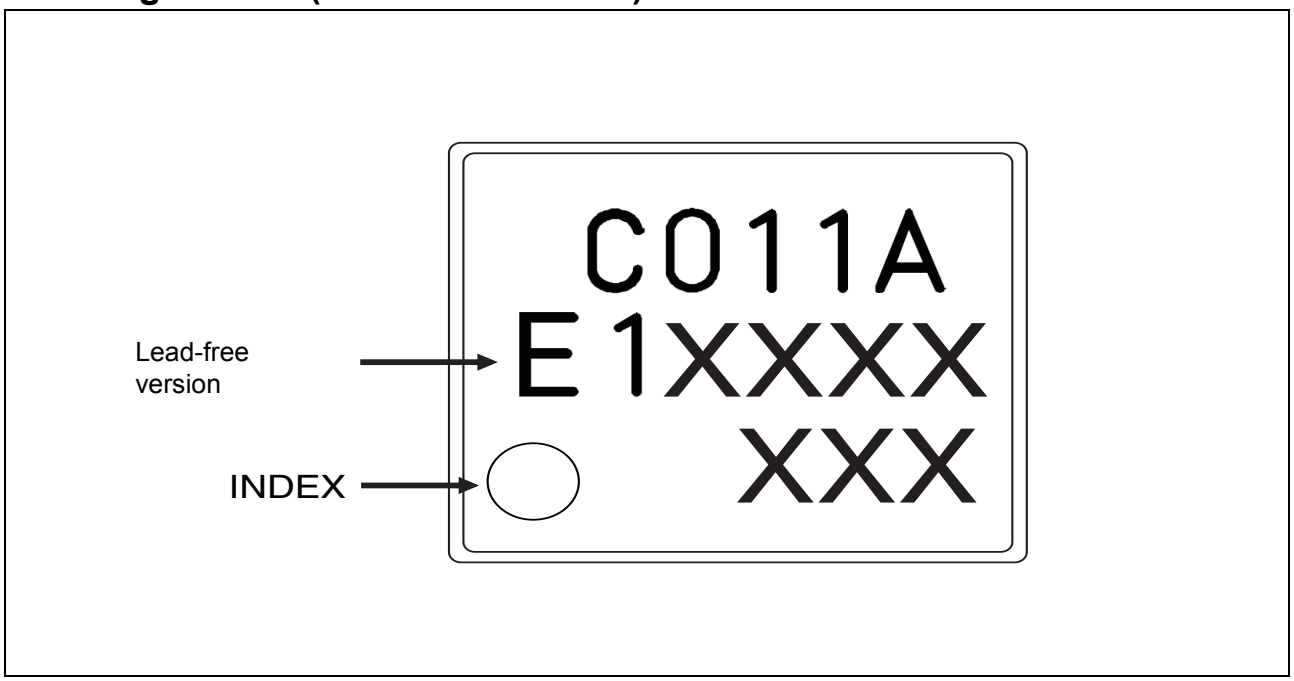
24. EV Board Ordering Information

Part number	EV board version No.	Remarks
MB39C011AEVB-01	Board rev.1.0	TSSOP-16-pin

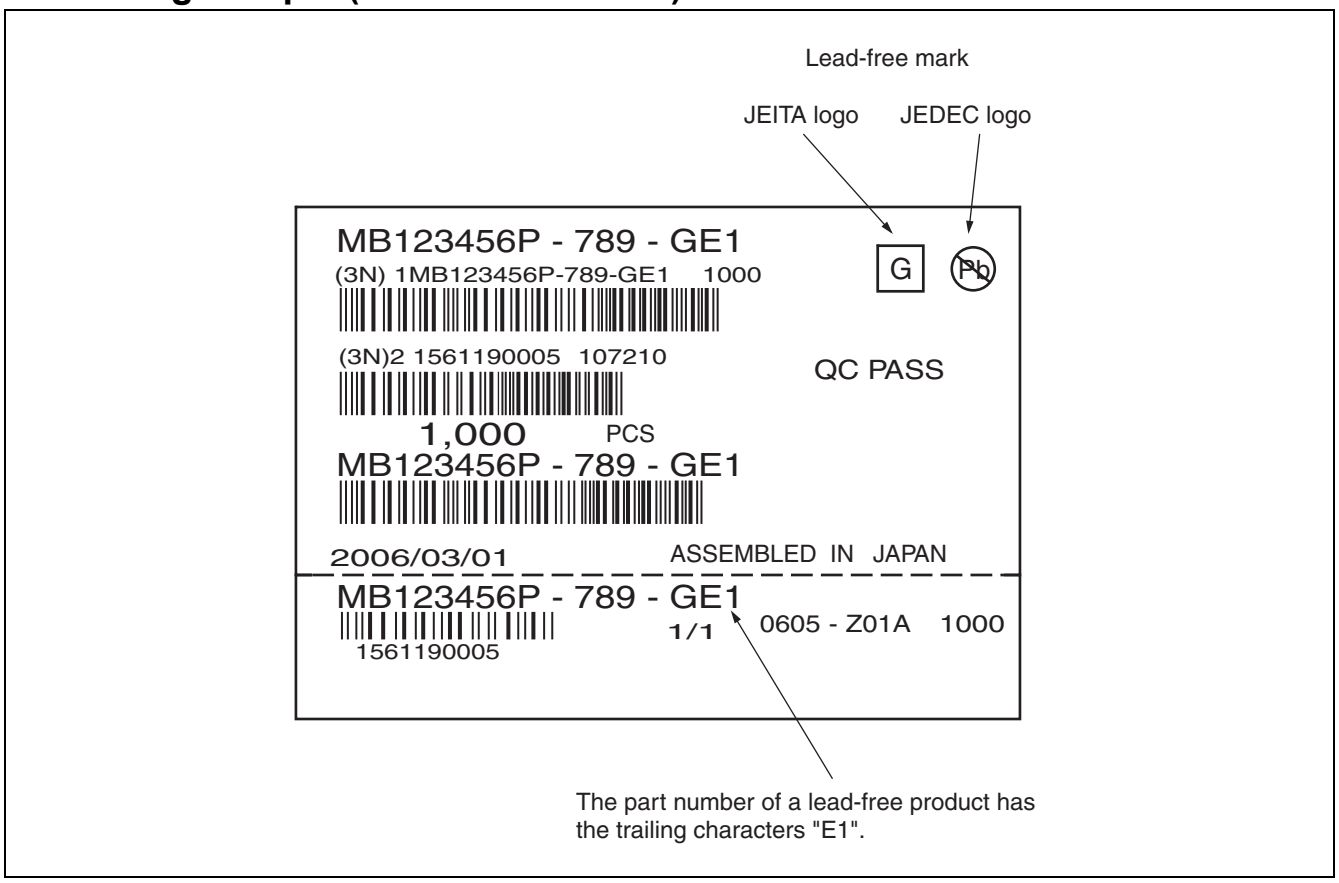
25. RoHS Compliance Information Of Lead (Pb) Free Version

The LSI products with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE). Products that are complied with this standard have “E1” appended to the part number.

26. Marking Format (Lead-free version)



27. Labeling Sample (Lead-free version)



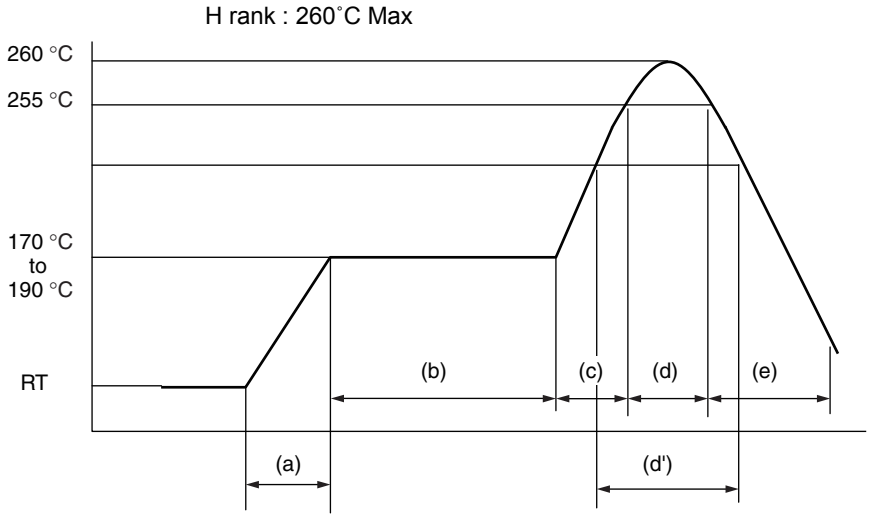
28. MB39C011APFT-❑❑❑E1 Recommended Mounting Conditions

28.1 Recommended Mounting Conditions

Item	Condition	
Mounting Method	IR (infrared reflow), Manual soldering (partial heating method)	
Mounting times	2 times	
Storage period	Before opening	Please use it within two years after Manufacture.
	From opening to the 2nd reflow	Less than 8 days
	When the storage period after opening was exceeded	Please processes within 8 days after baking (125˚C, 24H)
Storage conditions	5˚C to 30˚C, 70%RH or less (the lowest possible humidity)	

28.2 Parameters for Each Mounting Method

28.2.1 IR (infrared reflow)



(a) Temperature Increase gradient	: Average 1˚C/s to 4˚C/s
(b) Preliminary heating	: Temperature 170˚C to 190˚C, 60s to 180s
(c) Temperature Increase gradient	: Average 1˚C/s to 4˚C/s
(d) Actual heating	: Temperature 260˚C Max; 255˚C or more, 10s or less
(d')	: Temperature 230˚C or more, 40s or less or Temperature 225˚C or more, 60s or less or Temperature 220˚C or more, 80s or less
(e) Cooling	: Natural cooling or forced cooling

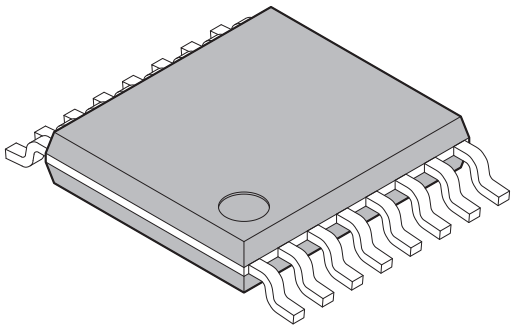
Note : Temperature : the top of the package body

28.2.2 Manual soldering (partial heating method)

Conditions : Temperature 400˚C Max

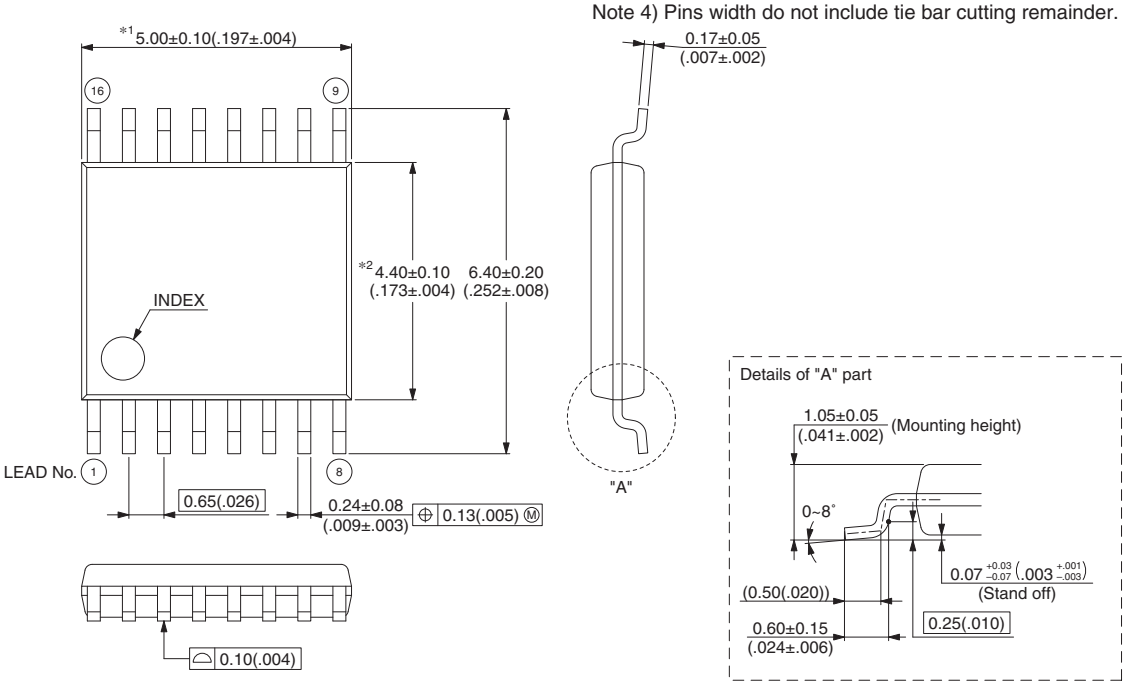
Times : 5 s max/pin

29. Package Dimensions

16-pin plastic TSSOP		
	Lead pitch	0.65 mm
	Package width × package length	4.40 × 5.00 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.10mm MAX
	Weight	0.06g
(FPT-16P-M07)	Code (Reference)	P-TSSOP16-4.4×5.0-0.65

16-pin plastic TSSOP
(FPT-16P-M07)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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**	—	TAOA	08/07/2008	Migrated to Cypress and assigned document number 002-08369. No change to document contents or format.
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