Absolute Maximum Ratings

Supply Voltage, V_{CC} to GND .....-0.3V to +6V
All Other Pins .....-0.3V to (V_{CC} + 0.3V)
Current into Input Pins .....±20mA
Duration of Output Short Circuit to GND or V_{CC} .....Continuous
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 3.90mW/°C above +70°C).....312.6mW/°C
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW/°C
8-Pin µMAX (derate 4.10mW/°C above +70°C).....330mW/°C
14-Pin SO (derate 8.33mW/°C above +70°C).....667mW/°C
16-Pin SO (derate 8.70mW/°C above +70°C).....696mW/°C
16-Pin QSOP (derate 8.33mW/°C above +70°C) ..667mW/°C
Operating Temperature Range
MAX96_E/MAX99_E ..... -40°C to +85°C
MAX999AAUK ..... -40°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = +2.7V to +5.5V, V_{CM} = 0V, C_{OUT} = 5pF, V_{SHDN} = 0V, V_{LE} = 0V, unless otherwise noted. T_{MIN} to T_{MAX} is -40°C to +85°C for all E grade devices. For MAX999AAUK only, T_{MIN} to T_{MAX} is -40°C to +125°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		T_A = +25°C			T_{MIN} to T_{MAX}			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage	V_{CC}	Inferred by PSRR		2.7		5.5	2.7		5.5	V
Input Common-Mode Voltage Range	V_{CMR}	(Note 2)		-0.1		V_{CC} + 0.1	-0.1		V_{CC} + 0.1	V
Input-Referred Trip Points	V_{TRIP}	V_{CM} = -0.1V or 5.1V, V_{CC} = 5V (Note 3)	µMAX, SOT23		±2.0	±3.5			±6.5	mV
			MAX999AAUK		±2.0	±3.5			±8.0	
			All other E packages		±2.0	±3.5			±4.0	
Input-Referred Hysteresis					3.5					mV
Input Offset Voltage	V_{OS}	V_{CM} = -0.1V or 5.1V, V_{CC} = 5V (Note 4)	µMAX, SOT23		±0.5	±1.5			±4.5	mV
			MAX999AAUK		±0.5	±1.5			±6.0	
			All other E packages		±0.5	±1.5			±2.0	
Input Bias Current	I_B	V_{IN+} = V_{IN-} = 0V or V_{CC}, V_{CC} = 5V	µMAX, SOT23			±15			±30	µA
			All other E packages			±15			±15	
Differential Input Clamp Voltage		V_{CC} = 5.5V, V_{IN-} = 0V, I_{IN+} = 100µA			2.1					V
Input Capacitance					3					pF
Differential Input Impedance	R_{IND}	V_{CC} = 5V			8					kΩ
Common-Mode Input Impedance	R_{INCM}	V_{CC} = 5V			130					kΩ

Electrical Characteristics (continued)

(V_{CC} = +2.7V to +5.5V, V_{CM} = 0V, C_{OUT} = 5pF, V_{SHDN} = 0V, V_{LE} = 0V, unless otherwise noted. T_{MIN} to T_{MAX} is -40°C to +85°C for all E grade devices. For MAX999AAUK only, T_{MIN} to T_{MAX} is -40°C to +125°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		T_A = +25ºC			T_{MIN} to T_{MAX}			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Common-Mode Rejection Ratio	CMRR	V_{CC} = 5V, V_{CM} = -0.1V to 5.1V (Note 5)	µMAX, SOT23		0.1	0.3			1.0	mV/V
			All other E packages		0.1	0.3			0.5	
Power-Supply Rejection Ratio	PSRR	V_{CM} = 0V (Note 6)			0.05	0.3			0.3	mV/V
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA	E grade	V_{CC} - 0.52			V_{CC} - 0.52			V
			MAX999AAUK	V_{CC} - 0.52			V_{CC} - 0.55			
Output Low Voltage	V_{OL}	I_{SINK} = 4mA	E grade			0.52			0.52	V
			MAX999AAUK			0.52			0.55	
Capacitive Slew Current		V_{OUT} = 1.4V, V_{CC} = 2.7V		30	60					mA
Output Capacitance					4					pF
Supply Current per Comparator	I_{CC}	MAX961/MAX963, V_{CC} = 5V			7.2	11			11	mA
		MAX962/MAX964, V_{CC} = 5V			5	8			9	
		MAX997/MAX999E, V_{CC} = 5V			5	6.5			6.5	
		MAX999AAUK, V_{CC} = 5V			5	6.5			7.0	
Shutdown Supply Current per Comparator	I_{SHDN}	MAX961/MAX963/MAX964/ MAX997, V_{CC} = 5V			0.27	0.5			0.5	mA
Shutdown Output Leakage Current		MAX961/MAX963/MAX964/ MAX997, V_{OUT} = 5V and V_{CC} - 5V				1			20	µA
Rise/Fall Time	t_R, t_F	V_{CC} = 5V			2.3					ns
Logic-Input High	V_{IH}			V_{CC}/2 + 0.4			V_{CC}/2 + 0.4			V
Logic-Input Low	V_{IL}					V_{CC}/2 - 0.4			V_{CC}/2 - 0.4	V
Logic-Input Current	I_{IL}, I_{IH}	V_{LOGIC} = 0V or V_{CC}				±15			±30	µA
Propagation Delay	t_{PD}	5mV overdrive (Note 7)	E grade		4.5	7.0			8.5	ns
			MAX999AAUK		4.5	7.0			10	
Differential Propagation Delay	t_{PD}	Between any two channels or outputs (Q/$\overline{Q}$)			0.3					ns
Propagation-Delay Skew	t_{SKEW}	Between t_{PD-} and t_{PD+}			0.3					ns

Electrical Characteristics (continued)

(V_{CC} = +2.7V to +5.5V, V_{CM} = 0V, C_{OUT} = 5pF, V_{SHDN} = 0V, V_{LE} = 0V, unless otherwise noted. T_{MIN} to T_{MAX} is -40°C to +85°C for all E grade devices. For MAX999AAUK only, T_{MIN} to T_{MAX} is -40°C to +125°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25ºC			T_{MIN} to T_{MAX}			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Data-to-Latch Setup Time	t_{SU}	MAX961/MAX963 (Note 8)			5			5	ns
Latch-to-Data Hold Time	t_H	MAX961/MAX963 (Note 8)			5			5	ns
Latch Pulse Width	t_{LPW}	MAX961/MAX963 (Note 8)			5			5	ns
Latch Propagation Delay	t_{LPD}	MAX961/MAX963 (Note 8)			10			10	ns
Shutdown Time	t_{OFF}	Delay until output is high-Z (> 10kΩ)		150					ns
Shutdown Disable Time	t_{ON}	Delay until output is valid		250					ns

Note 1: The MAX961EUA/MAX962EUA/MAX997EUA/MAX999EUK are 100% production tested at T_A = +25°C; all temperature specifications are guaranteed by design.

Note 2: Inferred by CMRR. Either input can be driven to the absolute maximum limit without false output inversion, provided that the other input is within the input voltage range.

Note 3: The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone. (See Figure 1.)

Note 4: Input offset voltage is defined as the mean of the trip points.

Note 5: CMRR = (V_{OSL} - V_{OSH}) / 5.2V, where V_{OSL} is the offset at V_{CM} = -0.1V and V_{OSH} is the offset at V_{CM} = 5.1V.

Note 6: PSRR = (V_{OS}2.7 - V_{OS}5.5) / 2.8V, where V_{OS}2.7 is the offset voltage at V_{CC} = 2.7V, and V_{OS}5.5 is the offset voltage at V_{CC} = 5.5V.

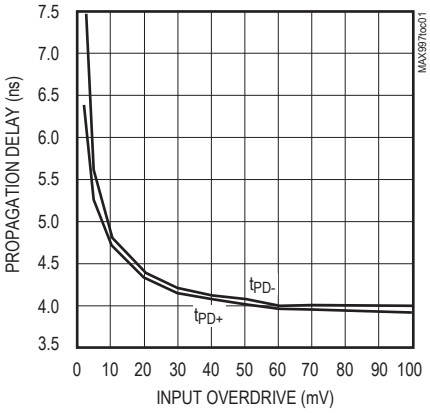
Note 7: Propagation delay for these high-speed comparators is guaranteed by design characterization because it cannot be accurately measured using automatic test equipment. A statistically significant sample of devices is characterized with a 200mV step and 100mV overdrive over the full temperature range. Propagation delay can be guaranteed by this characterization, since DC tests ensure that all internal bias conditions are correct. For low overdrive conditions, V_{TRIP} is added to the overdrive.

Note 8: Guaranteed by design.

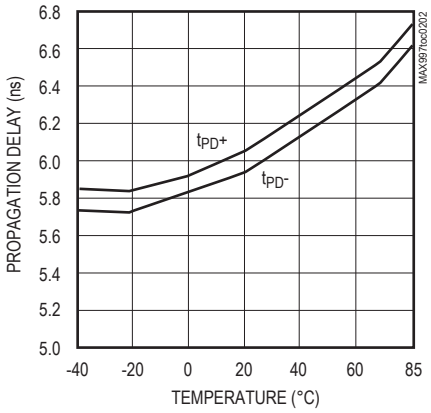
Typical Operating Characteristics

(V_{CC} = +3.0V, C_{LOAD} = 5pF, 5mV of overdrive, T_A = +25°C, unless otherwise noted.)

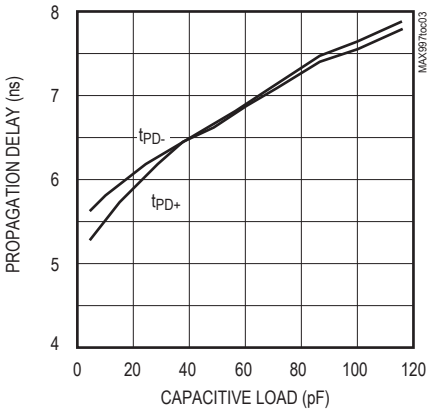
PROPAGATION DELAY vs. INPUT OVERDRIVE



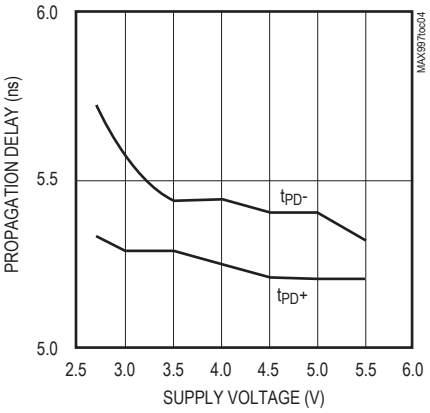
PROPAGATION DELAY vs. TEMPERATURE



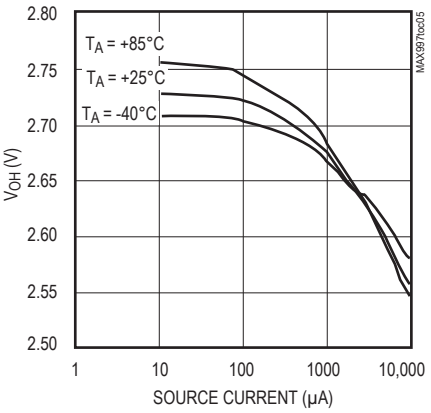
PROPAGATION DELAY vs. CAPACITIVE LOAD



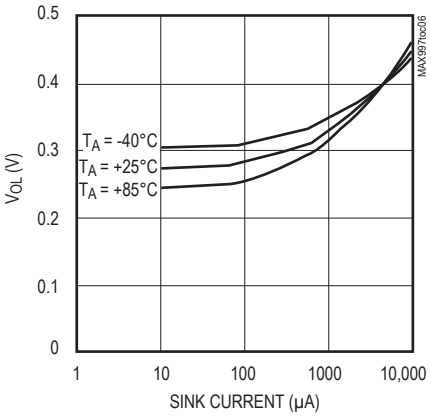
PROPAGATION DELAY vs. SUPPLY VOLTAGE



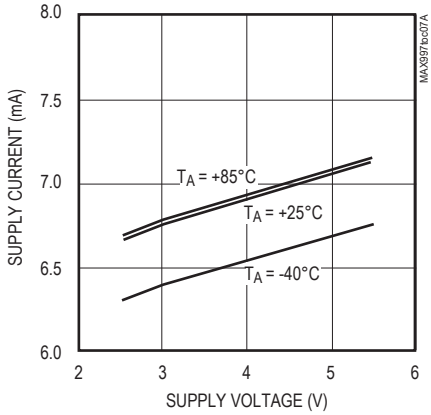
OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



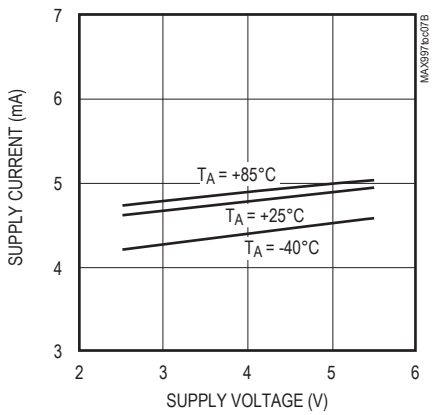
OUTPUT LOW VOLTAGE vs. SINK CURRENT



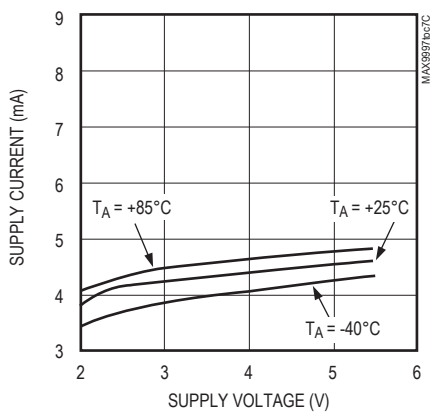
MAX961/MAX963 SUPPLY CURRENT PER COMPARATOR vs. SUPPLY VOLTAGE



MAX962/MAX964 SUPPLY CURRENT PER COMPARATOR vs. SUPPLY VOLTAGE



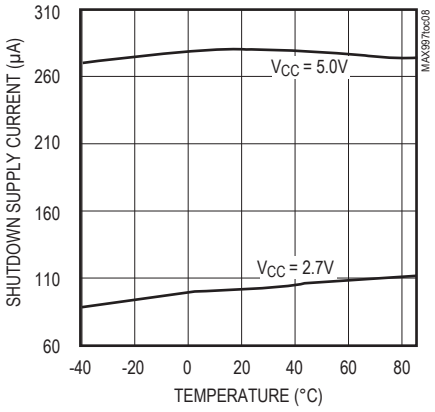
MAX997/MAX999 SUPPLY CURRENT PER COMPARATOR vs. SUPPLY VOLTAGE



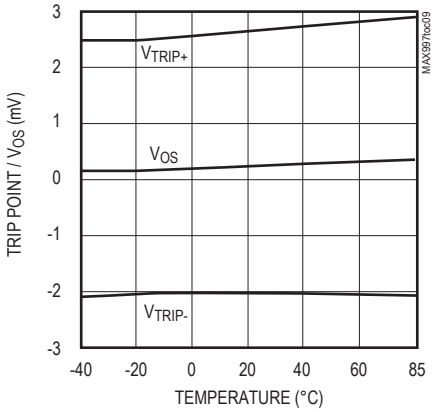
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V, C_{LOAD} = 5pF, 5mV of overdrive, T_A = +25°C, unless otherwise noted.)

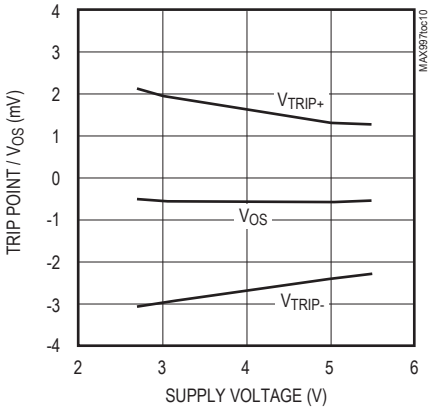
MAX961/MAX963/MAX964/MAX997 SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



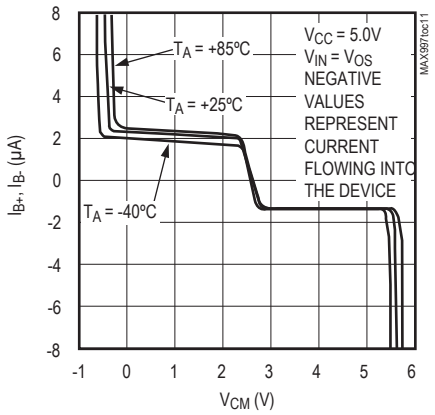
VOLTAGE TRIP POINT/INPUT OFFSET VOLTAGE vs. TEMPERATURE



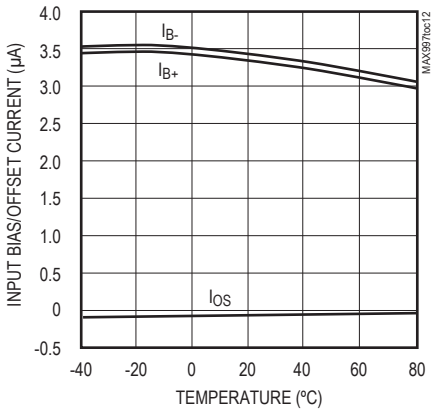
VOLTAGE TRIP POINT/INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



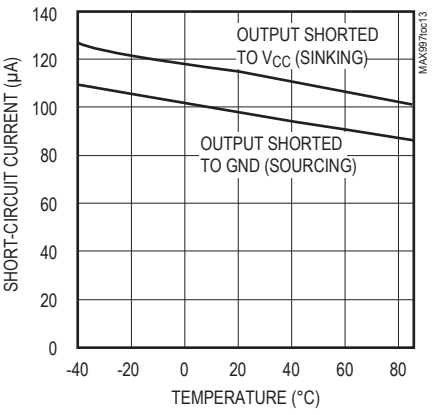
INPUT BIAS CURRENT (I_{B+}, I_{B-}) vs. COMMON-MODE VOLTAGE



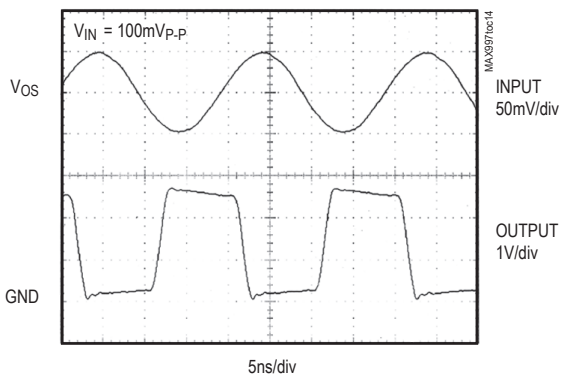
INPUT BIAS CURRENT/INPUT OFFSET CURRENT vs. TEMPERATURE



SHORT-CIRCUIT OUTPUT CURRENT vs. TEMPERATURE



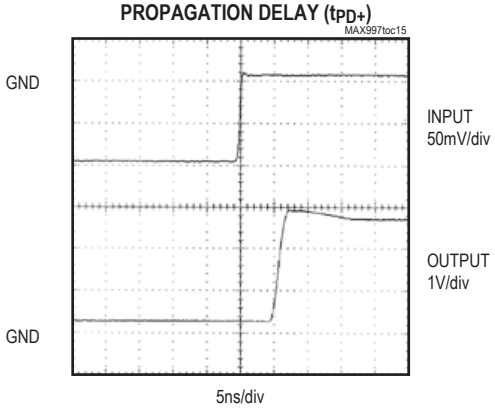
50MHz RESPONSE



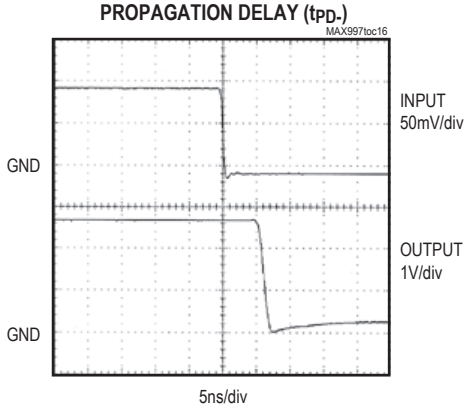
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V, C_{LOAD} = 5pF, 5mV of overdrive, T_A = +25°C, unless otherwise noted.)

PROPAGATION DELAY (t_{PD+})



PROPAGATION DELAY (t_{PD-})



Pin Description

PIN						NAME	FUNCTION
MAX997	MAX999	MAX961	MAX962	MAX963	MAX964		
1, 5	—	—	—	—	—	N.C.	No Connection. Not internally connected.
2	4	2	2	1	1	IN-, INA-	Comparator A Inverting Input
3	3	1	1	2	2	IN+, INA+	Comparator A Noninverting Input
—	—	4	—	3, 5	—	LE, LEA, LEB	Latch-Enable Input. The output latches when LE_ is high. The latch is transparent when LE_ is low.
4	2	5	5	4, 11	12	GND	Ground
—	—	—	—	—	16	N.C.	No Connection. Connect to GND to prevent parasitic feedback.
—	—	—	4	6	3	INB-	Comparator B Inverting Input
—	—	—	3	7	4	INB+	Comparator B Noninverting Input
—	—	—	—	—	5	INC-	Comparator C Inverting Input
—	—	—	—	—	6	INC+	Comparator C Noninverting Input
—	—	—	—	—	7	IND-	Comparator D Inverting Input
—	—	—	—	—	8	IND+	Comparator D Noninverting Input
8	—	3	—	8	9	SHDN	Shutdown Input. The device shuts down when SHDN is high.
—	—	—	6	9	14	QB	Comparator B Output
—	—	—	—	—	11	QC	Comparator C Output
—	—	—	—	—	10	QD	Comparator D Output
—	—	—	—	10	—	$\overline{QB}$	Comparator B Complementary Output
7	5	8	8	12	13	V_{CC}	Positive Supply Input (V_{CC} to GND must be ≤5.5V)
6	1	6	7	13	15	Q, QA	Comparator A TTL Output
—	—	7	—	14	—	$\overline{Q}$, $\overline{QA}$	Comparator A Complementary Output

Detailed Description

The MAX961–MAX964/MAX997/MAX999 single-supply comparators feature internal hysteresis, ultra-high-speed operation, and low power consumption. Their outputs are guaranteed to pull within 0.52V of either rail without external pullup or pulldown circuitry. Beyond-the-Rails input voltage range and low-voltage, single-supply operation make these devices ideal for portable equipment. These comparators all interface directly to CMOS logic.

Timing

Most high-speed comparators oscillate in the linear region because of noise or undesirable parasitic feedback. This can occur when the voltage on one input is close to or equal to the voltage on the other input. These devices have a small amount of internal hysteresis to counter parasitic effects and noise.

The added hysteresis of the MAX961–MAX964/MAX997/MAX999 creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The fixed internal hysteresis eliminates these resistors.

The MAX961/MAX963 include internal latches that allow storage of comparison results. LE has a high input impedance. If LE is low, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is stored when LE is pulled high. All timing constraints must be met when using the latch function (Figure 2).

Input Stage Circuitry

The MAX961–MAX964/MAX997/MAX999 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two groups of three front-to-back diodes between IN+ and IN-, as well as two 200Ω resistors (Figure 3). The diodes limit the differential voltage applied to the comparator's internal circuitry to no more than $3V_F$, where V_F is the diode's forward-voltage drop (about 0.7V at +25°C).

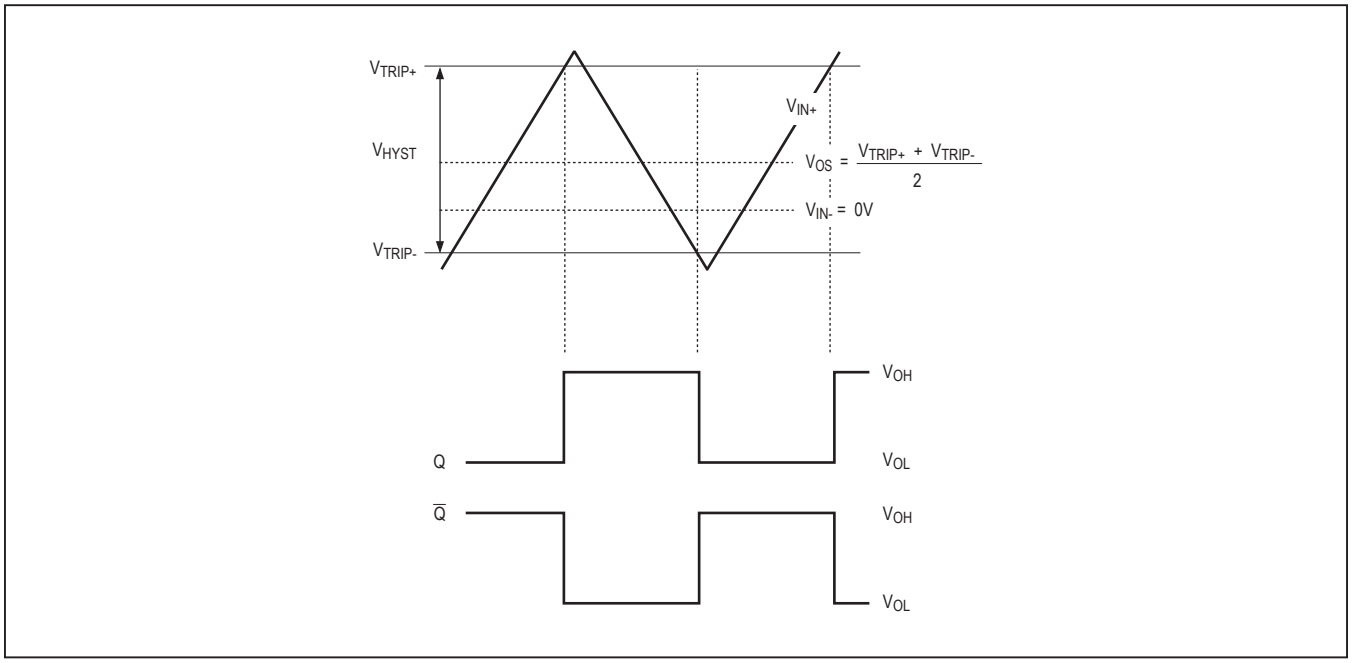


Figure 1. Input and Output Waveforms, Noninverting Input Varied

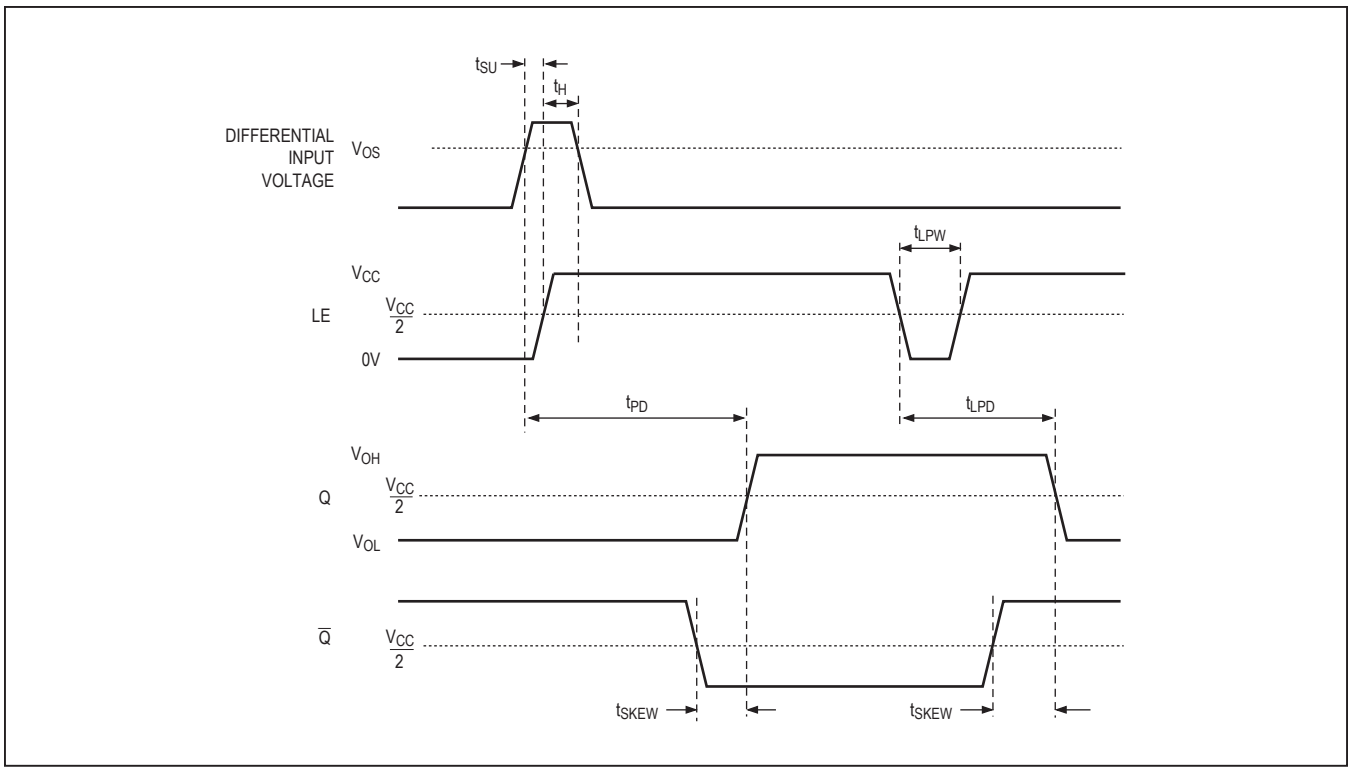


Figure 2. MAX961/MAX963 Timing Diagram

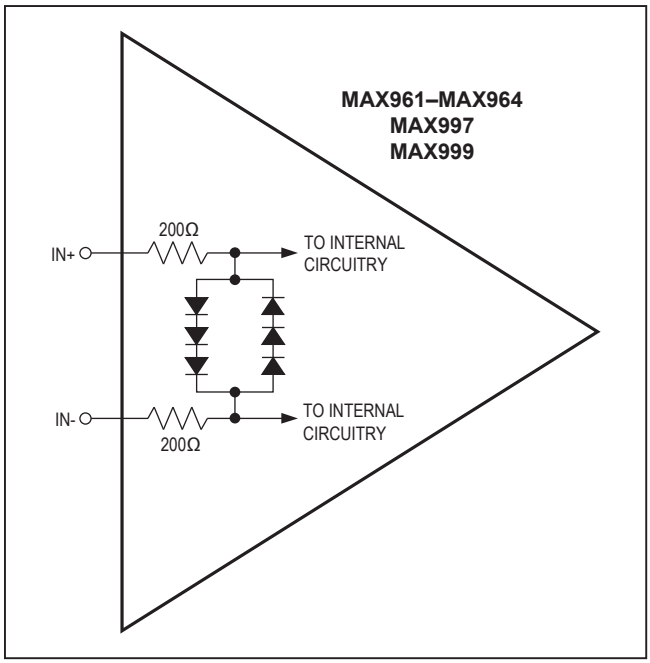


Figure 3. Input Stage Circuitry

For a large differential input voltage (exceeding $3V_F$), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{Input current} = \frac{(IN+ - IN-) - 3V_F}{2 \times 200}$$

Input currents with large differential input voltages should not be confused with input bias currents (I_B). As long as the differential input voltage is less than $3V_F$, this input current is less than $2I_B$.

The input circuitry allows the MAX961–MAX964/MAX997/MAX999's input common-mode range to extend 100mV beyond both power-supply rails. The output remains in the correct logic state if one or both inputs are within the common-mode range. Taking either input outside the common-mode range causes the input to saturate and the propagation delay to increase.

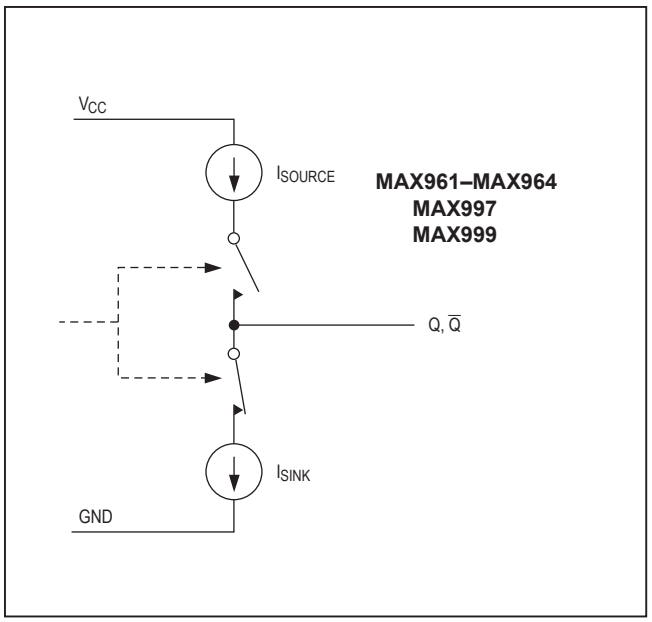


Figure 4. Output Stage Circuitry

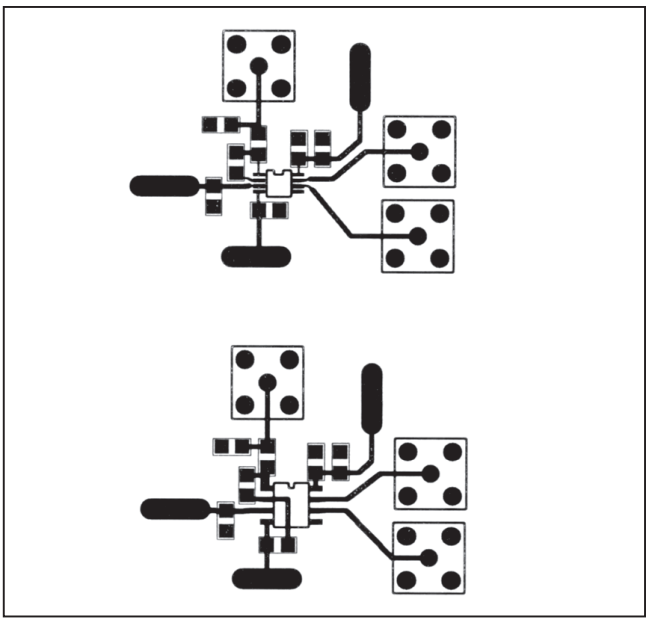


Figure 5. MAX961 PCB Layout

Output Stage Circuitry

The MAX961–MAX964/MAX997/MAX999 contain a current-driven output stage, as shown in Figure 4. During an output transition, I_{SOURCE} or I_{SINK} is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches V_{OH} or V_{OL}, the source or sink current decreases to a small value, capable of maintaining the V_{OH} or V_{OL} in static condition. This decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load slows down the voltage output transition.

Shutdown Mode

When SHDN is high, the MAX961/MAX963/MAX964/MAX997 shut down. When shut down, the supply current drops to 270µA per comparator, and the outputs become high impedance. SHDN has a high input impedance. Connect SHDN to GND for normal operation. Exit shutdown with LE low; otherwise, the output is indeterminate.

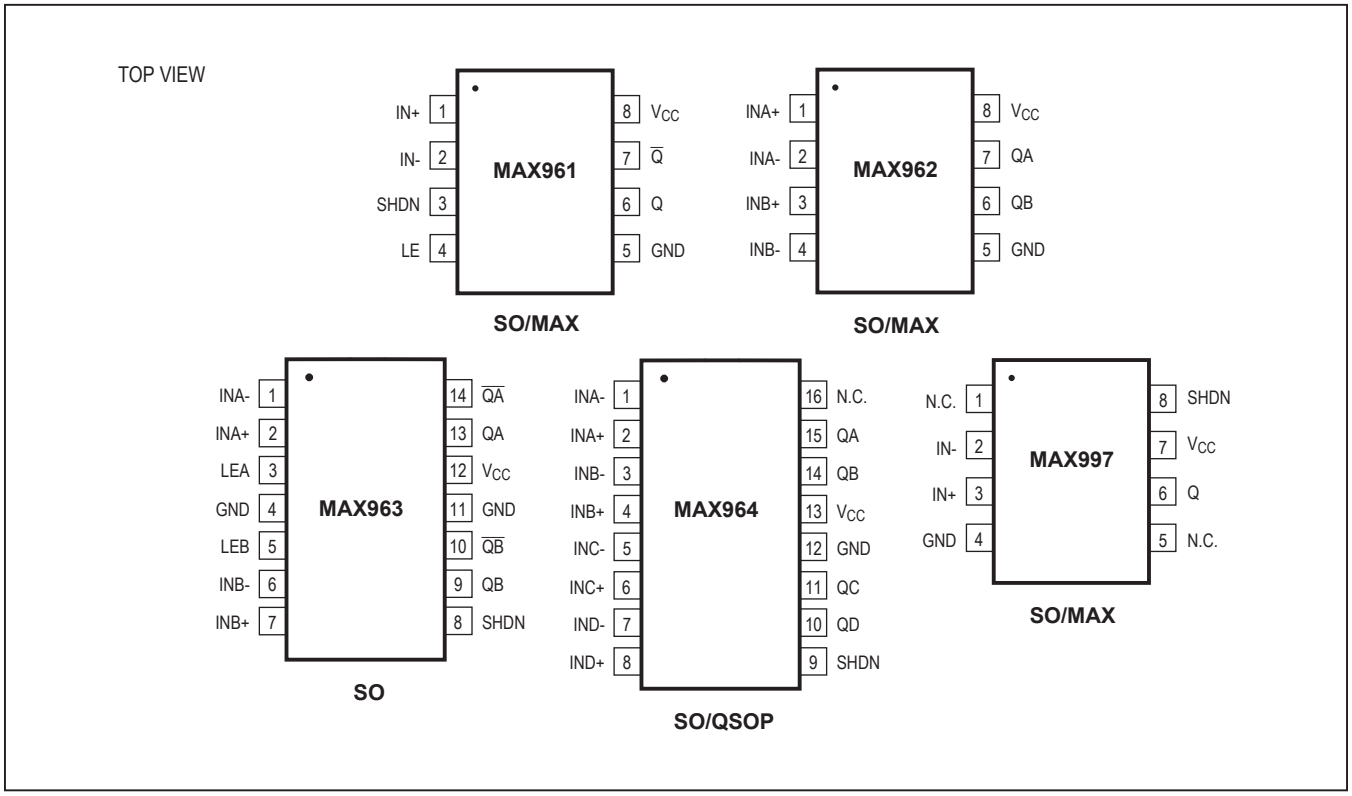
Applications Information

Circuit Layout and Bypassing

The MAX961–MAX964/MAX997/MAX999's high bandwidth requires a high-speed layout. Follow these layout guidelines:

1) Use a PCB with a good, unbroken, low-inductance ground plane.
2) Place a decoupling capacitor (a 0.1µF ceramic surface-mount capacitor is a good choice) as close to V_{CC} as possible.
3) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators. Keep inputs away from outputs. Keep impedance between the inputs low.
4) Solder the device directly to the printed circuit board rather than using a socket.
5) Refer to Figure 5 for a recommended circuit layout.
6) For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes negligible degradation to t_{PD} when the source impedance is low.

Pin Configurations



Chip Information

MAX961/MAX962 TRANSISTOR COUNT: 286
MAX963/MAX964 TRANSISTOR COUNT: 607
MAX997/MAX999 TRANSISTOR COUNT: 142

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.	LAND PATTERN NO.
5 SOT23	U5+2	21-0057	90-0174
8 SO	S8-2	21-0041	90-0096
8 µMAX	U8-1	21-0036	90-0092
14 SO	S14-1	21-0041	90-0112
16 SO	S16-1	21-0041	90-0097
16 QSOP	E16-1	21-0055	90-0167

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/96	Initial release	—
1	12/96	Added 8-pin µMAX packages. Correct minor errors.	1, 2, 3
2	3/97	Added dual and quad MAX963/MAX964 packages.	1, 2, 3
3	7/97	Added new MAX997 and MAX999 parts.	1, 2, 3
4	3/99	New wafer fab/process change to CB20. Update specifications and TOCs.	2, 3, 4, 5, 6
5	2/07	Added new Current into Input Pins in the *Absolute Maximum* Ratings.	2
6	12/08	Added new MAX999AAUK part and specifications.	1, 2, 3
7	9/14	Removed automotive reference from Revision History.	13
8	12/20	Updated *Absolute Maximum Ratings* and *Package Information*.	2, 12