

LVTTTL/TTL-to-Differential LVPECL/PECL Translators

ABSOLUTE MAXIMUM RATINGS

V _{CC} to GND (MAX9370/MAX9371)	-0.3V to +5.5V
V _{CC} to GND (MAX9372)	-0.3V to +4.0V
D ₋ to GND	-0.3V to (V _{CC} + 0.3V)
Q ₋ , $\overline{Q}_-$ to GND	-0.3V to (V _{CC} + 0.3V)
Continuous Output Current	50mA
Surge Output Current	100mA
Junction-to-Ambient Thermal Resistance in Still Air	
8-Pin SOT23	+112°C/W
8-Pin μ MAX	+221°C/W
8-Pin SO	+170°C/W
Junction-to-Ambient Thermal Resistance with 500LFPM Airflow	
8-Pin SOT23	+78°C/W
8-Pin μ MAX	+155°C/W
8-Pin SO	+99°C/W

Junction-to-Case Thermal Resistance

8-Pin SOT23	+80°C/W
8-Pin μ MAX	+39°C/W
8-Pin SO	+40°C/W
Continuous Power Dissipation (T _A = +70°C)	
8-Pin SO (derate 5.9mW/°C above +70°C)	470mW
8-Pin μ MAX (derate 4.5mW/°C above +70°C)	362mW
8-Pin SOT23 (derate 8.9mW/°C above +70°C)	714mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-60°C to +150°C
Soldering Temperature (10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.0V to 5.25V for MAX9370/MAX9371, V_{CC} = 3.0V to 3.6V for MAX9372, outputs terminated with 50 Ω $\pm$ 1% to V_{CC} - 2.0V. Typical values are at V_{CC} = 3.3V, V_{IH} = 2.4V, V_{IL} = 0.4V, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
LVTTTL INPUTS (D ₋)												
Input High Voltage	V _{IH}		2.0			2.0			2.0			V
Input Low Voltage	V _{IL}		0.8			0.8			0.8			V
Input Low Current	I _{IL}	V _D = 0.5V	-100			-100			-100			μA
Input High Current	I _{IH}	V _D = 2.7V	-50	+10		-50	+10		-50	+10		μA
		V _D = V _{CC} , MAX9370/MAX9371	130		130		130					
		V _D = V _{CC} , MAX9372	20		20		20					
Input Clamp Voltage		I _{IL} or I _{IH} = 18mA	-1.2			-1.2			-1.2			V
LVPECL/PECL OUTPUTS (Q ₋ , $\overline{Q}_-$)												
Output High Voltage	V _{OH}	MAX9370	V _{CC} - 1.085	V _{CC} - 0.895		V _{CC} - 1.025	V _{CC} - 0.895		V _{CC} - 1.025	V _{CC} - 0.895		V
		MAX9371/MAX9372	V _{CC} - 1.145	V _{CC} - 0.895		V _{CC} - 1.145	V _{CC} - 0.895		V _{CC} - 1.145	V _{CC} - 0.895		
Output Low Voltage	V _{OL}	MAX9370	V _{CC} - 1.83	V _{CC} - 1.62		V _{CC} - 1.81	V _{CC} - 1.62		V _{CC} - 1.81	V _{CC} - 1.62		V
		MAX9371/MAX9372	V _{CC} - 1.945	V _{CC} - 1.695		V _{CC} - 1.945	V _{CC} - 1.695		V _{CC} - 1.945	V _{CC} - 1.695		

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 3.0V$ to $5.25V$ for MAX9370/MAX9371, $V_{CC} = 3.0V$ to $3.6V$ for MAX9372, outputs terminated with $50\Omega \pm 1\%$ to $V_{CC} - 2.0V$. Typical values are at $V_{CC} = 3.3V$, $V_{IH} = 2.4V$, $V_{IL} = 0.4V$, unless otherwise noted.) (Notes 1, 2, 3)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Differential Output Swing ($V_{OH} - V_{OL}$)			600			600			600			mV
SUPPLY CURRENT												
Power-Supply Current (Note 4)	I_{CC}	MAX9370/ MAX9372	18	28		20	28		22	28		mA
		MAX9371	9.5	16		10.5	16		11.5	16		

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 3.0V$ to $5.25V$ for MAX9370/MAX9371, $V_{CC} = 3.0V$ to $3.6V$ for MAX9372, outputs terminated with $50\Omega \pm 1\%$ to $V_{CC} - 2.0V$, input frequency $\leq 1.0GHz$, input transition time = 125ps (20% to 80%), $V_{IH} = 2.0V$, $V_{IL} = 0.8V$. Typical values are at $V_{CC} = 3.3V$, $V_{IH} = 2.4V$, $V_{IL} = 0.4V$, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	-40°C			+25°C			+85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Maximum Toggle Frequency	f_{MAX}	$V_{OH} - V_{OL} \geq 600mV$	1.0	1.5		1.0	1.5		1.0	1.5		GHz
Input-to-Output Propagation Delay	t_{PLH} , t_{PHL}	Figure 1	200	270	400	200	270	400	200	270	400	ps
Output-to-Output Skew	t_{SKQQ}	MAX9370/ MAX9372 (Note 6)		10	50		7	50		7	50	ps
Output Rise/Fall Time	t_R , t_F	Figure 1	80		250	80		250	80		250	ps
Added Deterministic Jitter	t_{DJ}	1Gbps 2 ²³ - 1 PRBS pattern (Note 7)		40	60		40	60		40	60	ps(P-P)
Added Random Jitter	t_{RJ}	1GHz clock (Note 7)		0.23	0.8		0.23	0.8		0.23	0.8	ps(RMS)

Note 1: Measurements are made with the device in thermal equilibrium.

Note 2: Current into a pin is defined as positive. Current out of a pin is defined as negative.

Note 3: DC parameters are production tested at $T_A = +25^\circ C$. DC limits are guaranteed by design and characterization over the full operating temperature range.

Note 4: All pins are open except V_{CC} and GND.

Note 5: Guaranteed by design and characterization. Limits are set to ± 6 sigma.

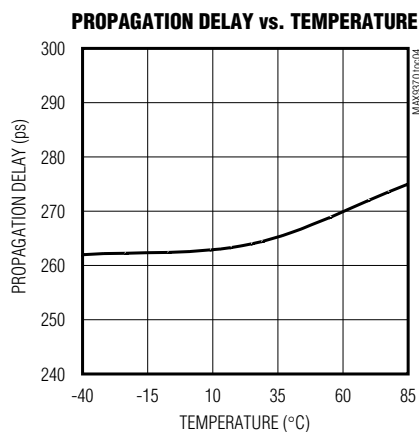
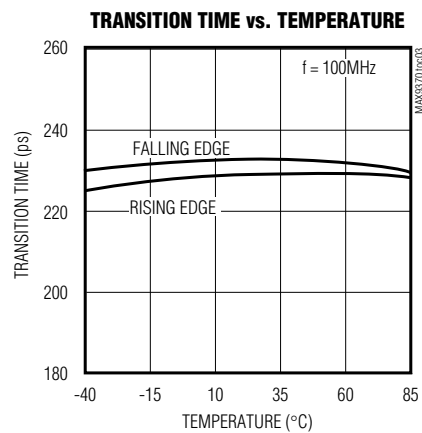
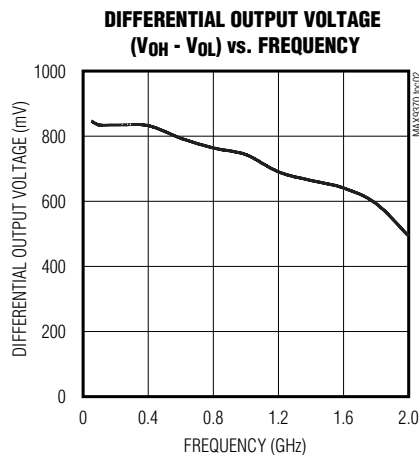
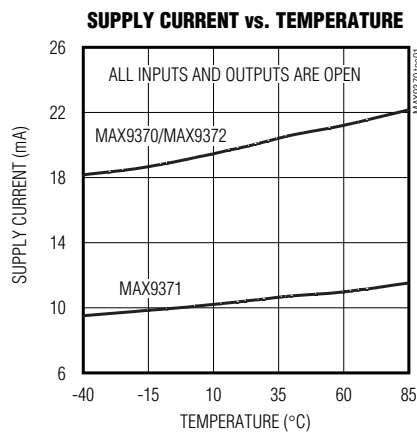
Note 6: Measured between outputs of the same part at the signal crossing points under identical conditions for a same-edge transition.

Note 7: Device jitter added to the input signal.

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Typical Operating Characteristics

(MAX9371, $V_{CC} = 3.3V$, $V_{IH} = 2.4V$, $V_{IL} = 0.4V$, outputs terminated with 50Ω to $V_{CC} - 2V$, input transition time = 125ps (20% to 80%), $T_A = +25^\circ C$, unless otherwise noted.)



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Pin Description for the MAX9370/MAX9372

PIN		NAME	FUNCTION
SO μ MAX	SOT23		
1	8	Q0	Noninverting Differential LVPECL/PECL Output 0. Typically terminate with 50 Ω resistor to $V_{CC} - 2V$.
2	7	$\overline{Q0}$	Inverting Differential LVPECL/PECL Output 0. Typically terminate with 50 Ω resistor to $V_{CC} - 2V$.
3	6	Q1	Noninverting Differential LVPECL/PECL Output 1. Typically terminate with 50 Ω resistor to $V_{CC} - 2V$.
4	5	$\overline{Q1}$	Inverting Differential LVPECL/PECL Output 1. Typically terminate with 50 Ω resistor to $V_{CC} - 2V$.
5	2	GND	Ground. Provide a low-impedance connection to ground plane.
6	4	D1	LVTTL/TTL Input 1. LVTTL/TTL input for translator corresponding to output Q1 and $\overline{Q1}$.
7	3	D0	LVTTL/TTL Input 0. LVTTL/TTL input for translator corresponding to output Q0 and $\overline{Q0}$.
8	1	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to GND with 0.1 μ F and 0.01 μ F ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.

Pin Description for the MAX9371

PIN		NAME	FUNCTION
SO μ MAX	SOT23		
1, 4, 6	4, 5, 8	N.C.	No Connection. No internal connection.
2	7	Q	Noninverting Differential LVPECL/PECL Output. Typically terminate with 50 Ω resistor to $V_{CC} - 2V$.
3	6	$\overline{Q}$	Inverting Differential LVPECL/PECL Output. Typically terminate with 50 Ω resistor to $V_{CC} - 2V$.
5	2	GND	Ground. Provide a low-impedance connection to ground plane.
7	3	D	LVTTL/TTL Input
8	1	V_{CC}	Positive Supply Voltage. Bypass V_{CC} to GND with 0.1 μ F and 0.01 μ F ceramic capacitors. Place the capacitors as close to the device as possible with the smaller value capacitor closest to the device.

Detailed Description

The MAX9370/MAX9371/MAX9372 LVTTL/TTL-to-differential LVPECL/PECL translators are designed for high-speed communication signal and clock driver applications. The MAX9370/MAX9372 are dual LVTTL-to-LVPECL/PECL translators that operate in excess of 1GHz. The MAX9371 is a single translator. The MAX9370/MAX9371 operate over a wide 3.0V to 5.25V supply range, allowing high-performance clock or data distribution in systems with a nominal 3.3V or 5.0V supply. The MAX9372 is optimized for 3.0V to 3.6V operation. These devices feature low 270ps propagation delay and 40ps peak-to-peak deterministic jitter.

Inputs and Outputs

The MAX9370/MAX9371/MAX9372 inputs accept standard LVTTL/TTL levels. The input has pullup circuitry that drives the outputs to a differential high if the inputs are open. The outputs are differential LVPECL/PECL levels.

Applications Information

Output Termination

Terminate outputs with 50 Ω to $V_{CC} - 2V$ or use an equivalent Thevenin termination. Use the same terminate on each output for the lowest output-to-output skew. When a single-ended signal is taken from a differential output, terminate both outputs. For example, if Q is used as a single-ended output, terminate both Q and $\overline{Q}$.

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Ensure that the output currents do not exceed the continuous safe output current limit or surge output current limit as specified in the *Absolute Maximum Ratings* table. Under all operating conditions, the device's total thermal limits should be observed.

Supply Bypassing

Bypass V_{CC} to GND with high-frequency surface-mount ceramic 0.1 μ F and 0.01 μ F capacitors in parallel and as close to the device as possible, with the 0.01 μ F capacitor closest to the device. Use multiple parallel vias to minimize parasitic inductance.

PC Board Traces

Input and output trace characteristics affect the performance of the MAX9370/MAX9371/MAX9372. Connect each differential output to a 50 Ω characteristic impedance trace. Minimize the number of vias to prevent impedance discontinuities. Reduce reflections by maintaining the 50 Ω characteristic impedance through connectors and across cables. Reduce skew within a differential pair by matching the electrical length of the traces.

Chip Information

TRANSISTOR COUNT: 358

PROCESS: Bipolar

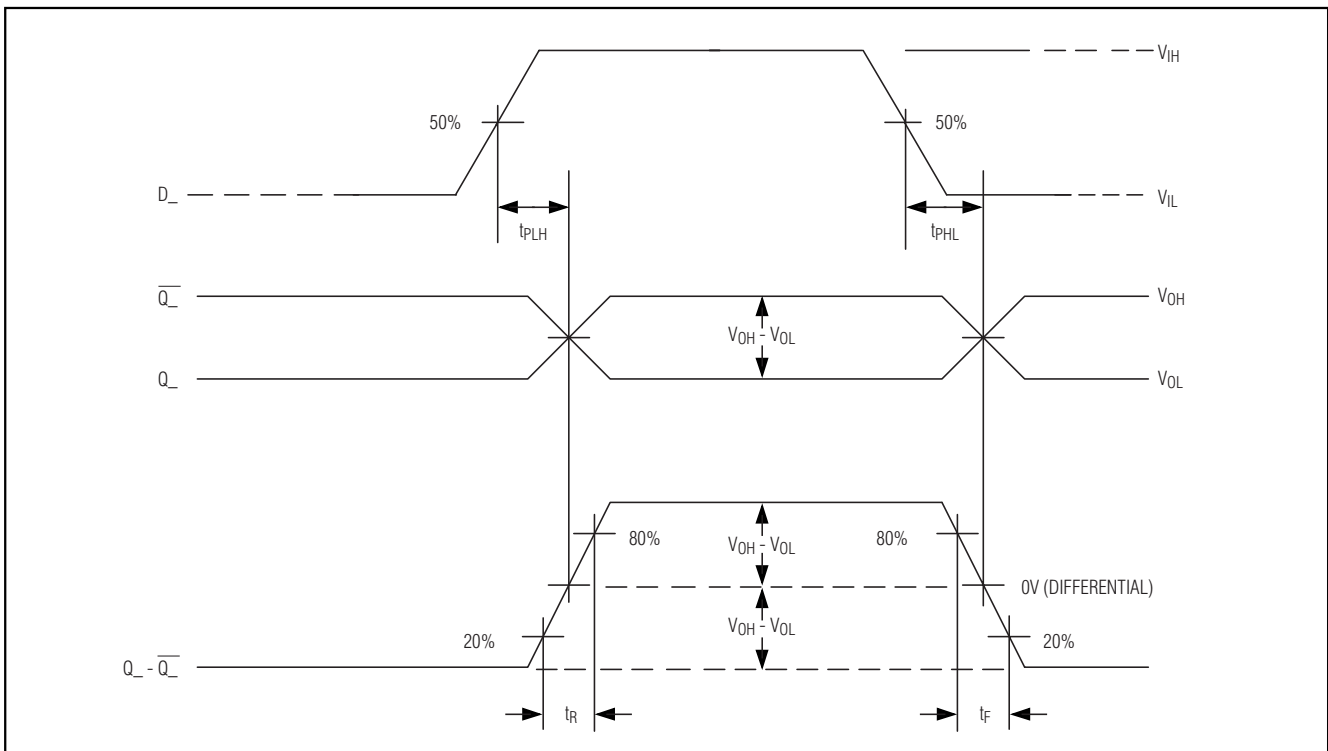
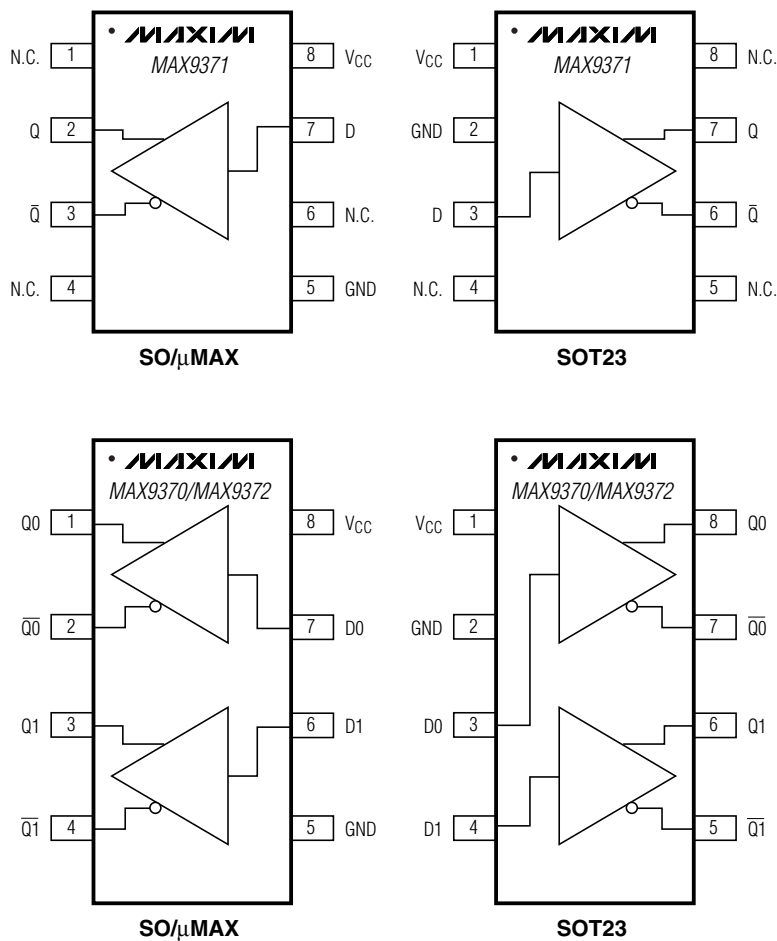


Figure 1. Input-to-Output Propagation Delay and Transition Timing Diagram

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Pin Configurations/Functional Diagrams

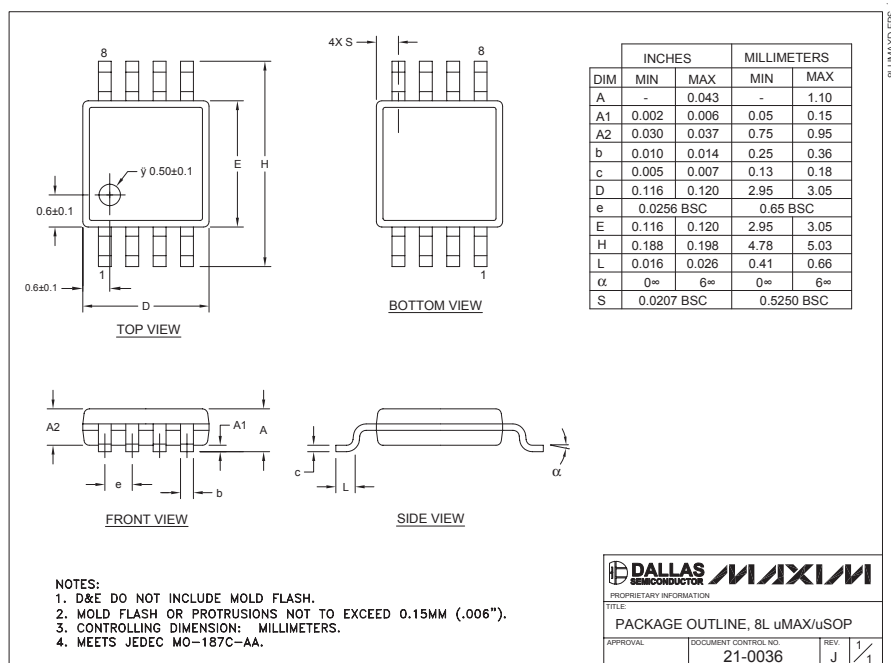
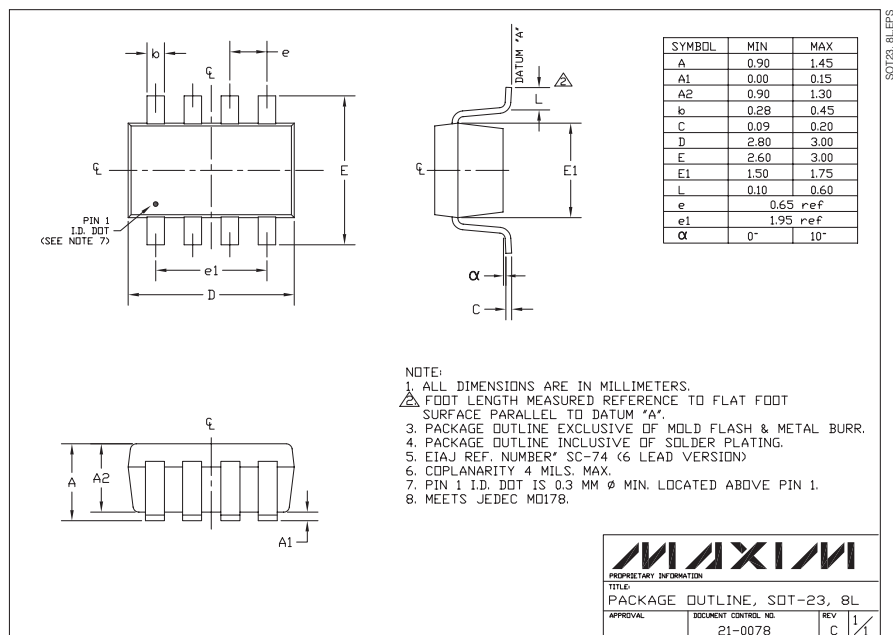


MAX9370/MAX9371/MAX9372

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Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



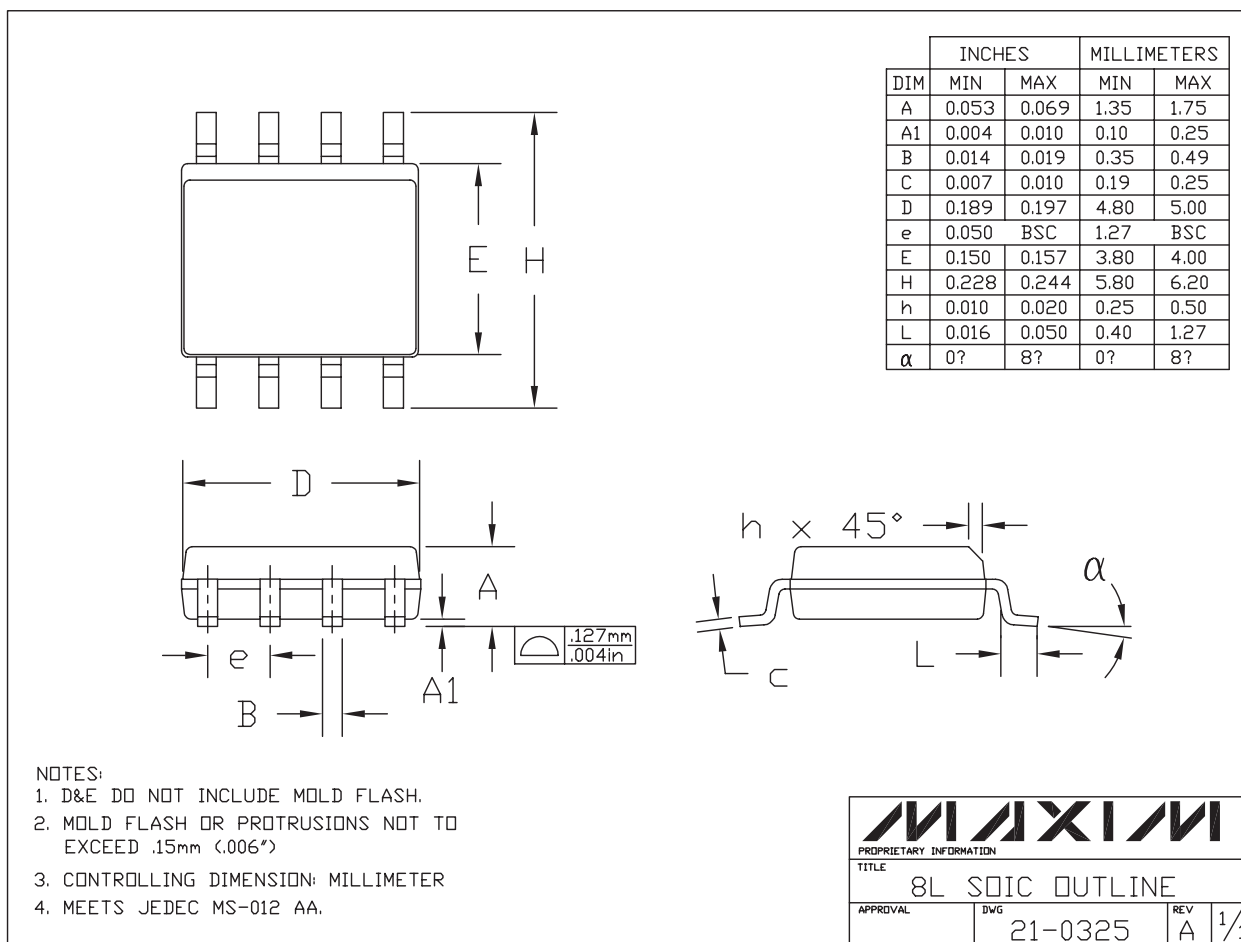
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Package Information (continued)

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9LUCSP, 3x3.EPS



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