

Absolute Maximum Ratings

Supply Voltage (V_{DD} to V_{SS}) -0.3V to +6V
 Voltage Inputs ($IN+$, $IN-$ to V_{SS}) -0.3V to (V_{DD} + 0.3V)
 Differential Input Voltage ($IN+$ to $IN-$) +6.6V
 Output Short-Circuit
 Duration 2s to Either V_{DD} or V_{SS}
 Current into Any Pin 20mA
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)
 5-Pin SC70 (derate 3.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 247mW
 5-Pin SOT23 (derate 7.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 571mW
 6-Pin SC70 (derate 3.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 245mW
 6-Pin SOT23 (derate 8.7mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 696mW

8-Pin SOT23 (derate 9.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 727mW
 8-Pin μMAX (derate 4.5mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 362mW
 8-Pin SO (derate 5.88mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 471mW
 14-Pin TSSOP (derate 9.1mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 727mW
 14-Pin SO (derate 8.33mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 667mW
 Operating Temperature Range
 Automotive Application -40°C to $+125^\circ\text{C}$
 Junction Temperature $+150^\circ\text{C}$
 Storage Temperature Range -65°C to $+150^\circ\text{C}$
 Lead Temperature (soldering, 10s) $+300^\circ\text{C}$
 Soldering Temperature (reflow) $+260^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

($V_{DD} = +5\text{V}$, $V_{SS} = 0$, $V_{CM} = 0$, $V_{SHDN} = +5\text{V}$ (Note 1), $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$, unless otherwise noted. Typical values are at $T_A = +25^\circ\text{C}$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{DD}	Guaranteed by PSRR test	2.5		5.5	V
Supply Current per Comparator	I_{DD}			35	55	μA
Supply Current in Shutdown		$V_{SHDN} = 0$ (Note 1)		0.05	1	μA
Shutdown Input Bias Current		$V_{SHDN} = 0$ to V_{DD} (Note 1)		0.1	2.5	μA
Shutdown Logic High		(Note 1)	$0.7 \times V_{DD}$			V
Shutdown Logic Low		(Note 1)		$0.3 \times V_{DD}$		V
Input Offset Voltage	V_{OS}	(Note 3)		± 1	± 5	mV
Input Offset Voltage Temperature Coefficient	TCV_{OS}			± 1		$\mu\text{V}/^\circ\text{C}$
Hysteresis		(Note 4)		4		mV
Input Bias Current	I_{BIAS}			8	80	nA
Input Offset Current	I_{OS}			± 2	± 60	nA
Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR test	V_{SS}		$V_{DD} - 1.1$	V
Common-Mode Rejection Ratio	CMRR	$V_{SS} \leq V_{CM} \leq (V_{DD} - 1.1\text{V})$, $V_{DD} = +5.5\text{V}$	72	100		dB
Power-Supply Rejection Ratio	PSRR	$V_{DD} = +2.5\text{V}$ to $+5.5\text{V}$	72	100		dB

Electrical Characteristics (continued)

($V_{DD} = +5V$, $V_{SS} = 0$, $V_{CM} = 0$, $V_{SHDN} = +5V$ (Note 1), $T_A = -40^{\circ}C$ to $+125^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage-Swing	V_{OL} , V_{OH}	$V_{OH} = V_{DD} - V_{OUT}$, ($V_{IN+} - V_{IN-}$) $\geq 20mV$	$I_{SOURCE} = 10\mu A$	2		mV
			$I_{SOURCE} = 4mA$	165	400	
		$V_{OL} = V_{OUT} - V_{SS}$, ($V_{IN-} - V_{IN+}$) $\geq 20mV$	$I_{SINK} = 10\mu A$	2		
			$I_{SINK} = 4mA$	165	400	
Output Short-Circuit Current	I_{SC}			45		mA
Shutdown Mode Output Leakage		$V_{SHDN} \leq (0.3 \times V_{DD})$, $V_{OUT} = 0$ to V_{DD} (Note 1)		± 0.01	± 3.5	μA
Propagation Delay	t_{PD+} , t_{PD-}	$R_L = 10k\Omega$, $C_L = 15pF$ (Note 5)	$V_{OD} = 10mV$	228		ns
			$V_{OD} = 100mV$	188		
Rise/Fall-Time	t_R , t_F	$V_{DD} = +5V$, $R_L = 10k\Omega$, $C_L = 15pF$ (Note 6)		20		ns
Shutdown Delay Time ON/OFF		(Note 1)		40		ns
Shutdown Delay Time OFF/ON		(Note 1)		400		ns
Power-On Time		$R_L = 10k\Omega$, $C_L = 15pF$		200		ns
Maximum Capacitive Load	C_L	No sustained oscillations		150		pF

Note 1: MAX9030 only.

Note 2: All devices are production tested at $+25^{\circ}C$. All temperature limits are guaranteed by design.

Note 3: Comparator Input Offset is defined as the center of the hysteresis zone.

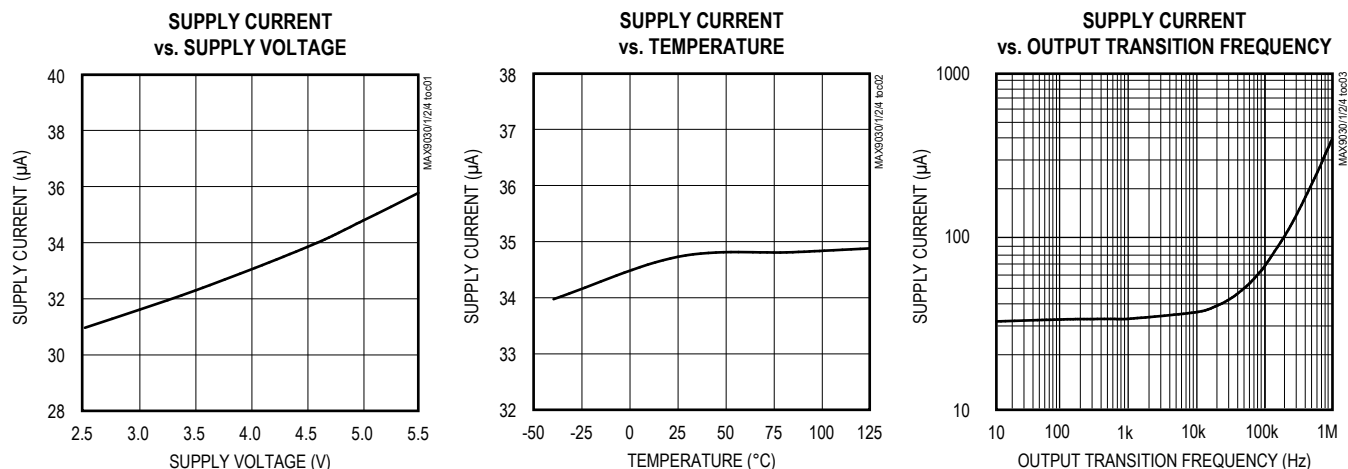
Note 4: Hysteresis is defined as the difference of the trip points required to change comparator output states.

Note 5: V_{OD} is the overdrive that is beyond the offset and hysteresis-determined trip points.

Note 6: Rise and fall times are measured between 10% and 90% at OUT.

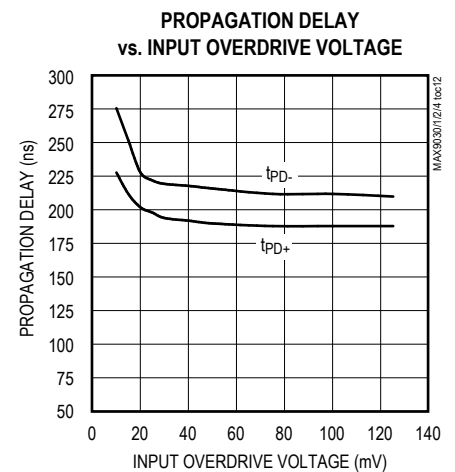
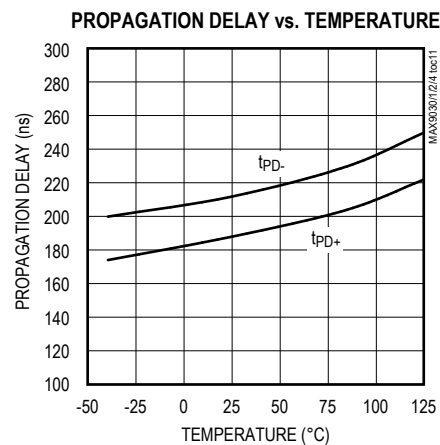
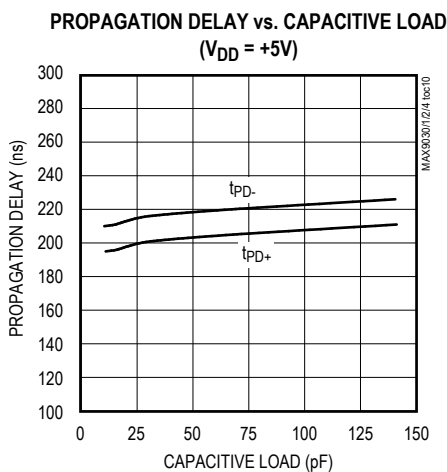
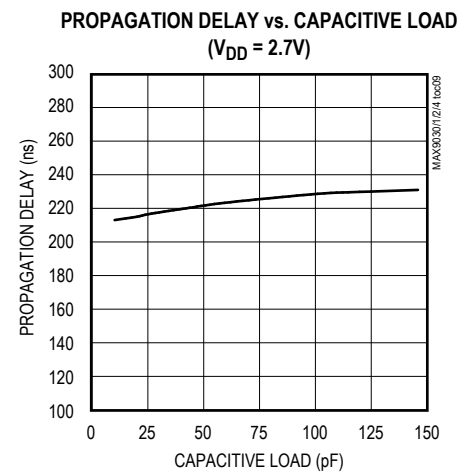
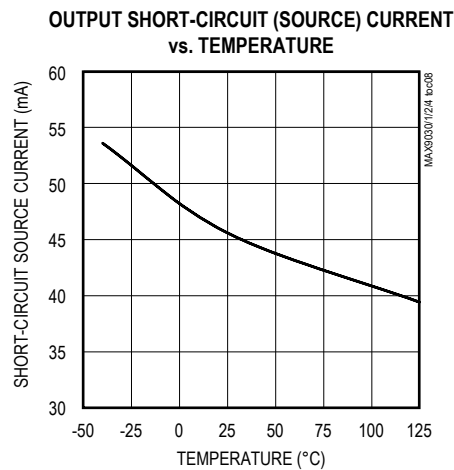
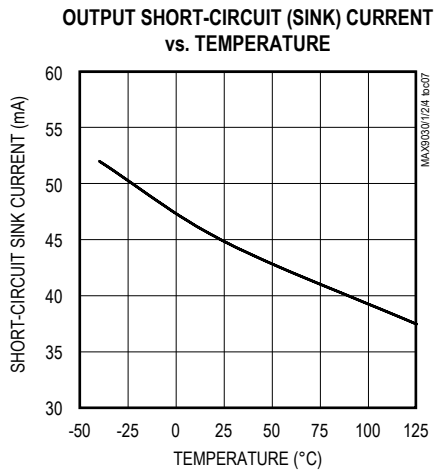
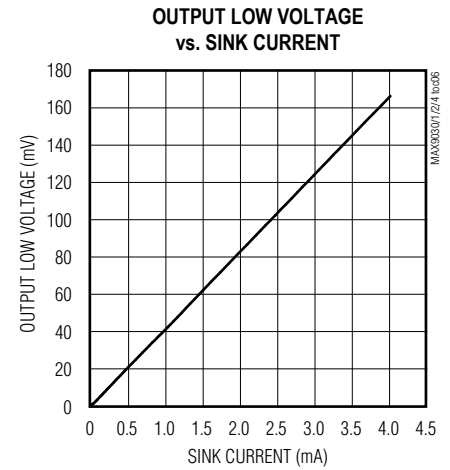
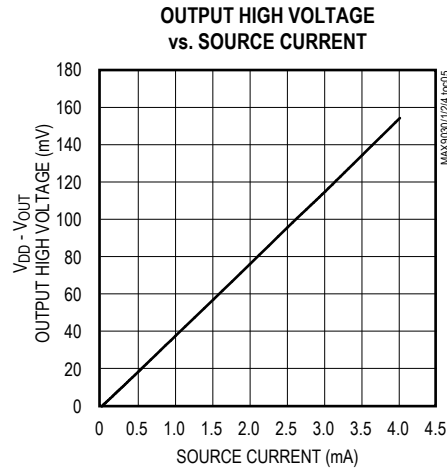
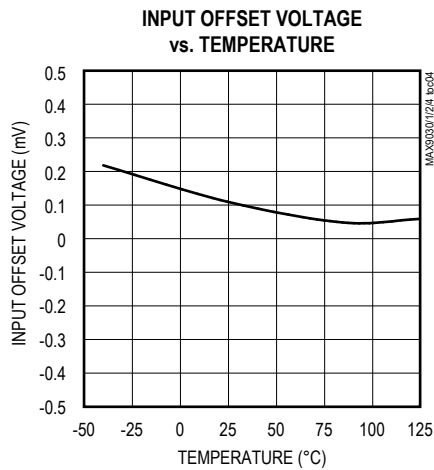
Typical Operating Characteristics

($V_{DD} = +5V$, $V_{SS} = 0$, $V_{CM} = 0$, $R_L = 10k\Omega$, $C_L = 15pF$, $V_{OD} = 100mV$, $T_A = +25^{\circ}C$, unless otherwise noted.)



Typical Operating Characteristics (continued)

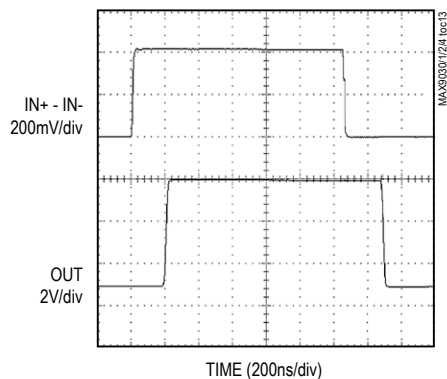
($V_{DD} = +5V$, $V_{SS} = 0$, $V_{CM} = 0$, $R_L = 10k\Omega$, $C_L = 15pF$, $V_{OD} = 100mV$, $T_A = +25^\circ C$, unless otherwise noted.)



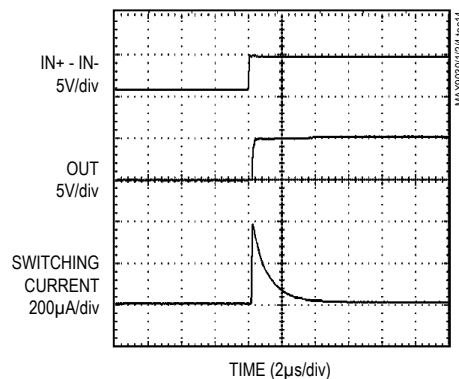
Typical Operating Characteristics (continued)

($V_{DD} = +5V$, $V_{SS} = 0$, $V_{CM} = 0$, $R_L = 10k\Omega$, $C_L = 15pF$, $V_{OD} = 100mV$, $T_A = +25^\circ C$, unless otherwise noted.)

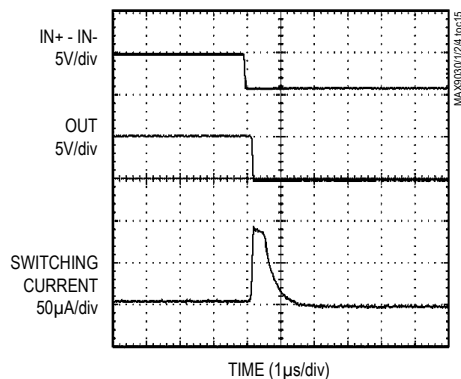
PROPAGATION DELAY



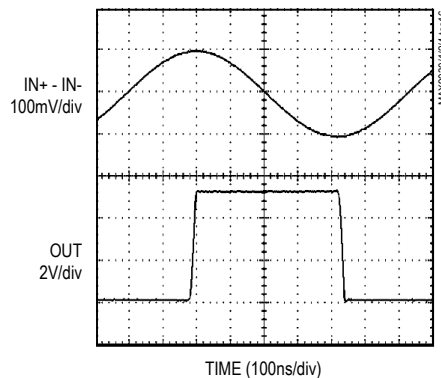
OUTPUT SWITCHING CURRENT, RISING



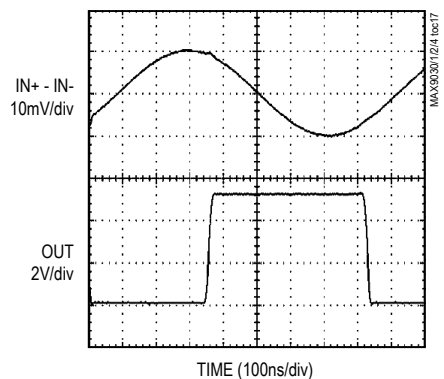
OUTPUT SWITCHING CURRENT, FALLING



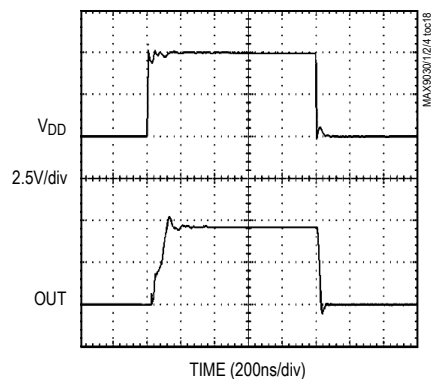
SINUSOID 1MHz RESPONSE AT 1.25MHz
 $V_{OD} = 100mV$



SINUSOID 1MHz RESPONSE AT 1.25MHz
 $V_{OD} = 10mV$



POWER-UP DELAY



Pin Description

PIN				NAME	FUNCTION
MAX9030	MAX9031	MAX9032	MAX9034		
1	1	—	—	IN+	Comparator Noninverting Input
2	2	4	11	V _{SS}	Negative Supply Voltage. Bypass with a 0.1μF capacitor.
3	3	—	—	IN-	Comparator Inverting Input
4	4	—	—	OUT	Comparator Output
5	—	—	—	$\overline{\text{SHDN}}$	Shutdown
6	5	8	4	V _{DD}	Positive Supply Voltage. Bypass with a 0.1μF capacitor.
—	—	1	1	OUTA	Comparator A Output
—	—	2	2	INA-	Comparator A Inverting Input
—	—	3	3	INA+	Comparator A Noninverting Input
—	—	5	5	INB+	Comparator B Noninverting Input
—	—	6	6	INB-	Comparator B Inverting Input
—	—	7	7	OUTB	Comparator B Output
—	—	—	8	OUTC	Comparator C Output
—	—	—	9	INC-	Comparator C Inverting Input
—	—	—	10	INC+	Comparator C Noninverting Input
—	—	—	12	IND+	Comparator D Noninverting Input
—	—	—	13	IND-	Comparator D Inverting Input
—	—	—	14	OUTD	Comparator D Output

Detailed Description

The MAX9030/MAX9031/MAX9032/MAX9034 are single/dual/quad low-cost comparators. They have an operating supply voltage from +2.5V to +5.5V when operating from a single supply and from ±1.25V to ±2.75V when operating from dual power supplies, and consume only 35μA. Their common-mode input voltage range extends from the negative supply to within 1.1V of the positive supply. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

Shutdown Mode

The MAX9030 comparator comes with a power-saving shutdown mode. When in shutdown, the supply current drops from a typical 35μA to 0.05μA, and the outputs become high impedance. $\overline{\text{SHDN}}$ has a high input impedance and typically draws 0.1μA when connected to V_{SS} or V_{DD}. A maximum logic low voltage of 0.3V x V_{DD} applied

to $\overline{\text{SHDN}}$ places the device in the shutdown mode. A minimum logic high voltage of 0.7V x V_{DD} applied to $\overline{\text{SHDN}}$ will enable normal operation. To disable shutdown, connect $\overline{\text{SHDN}}$ to V_{DD}.

Applications Information

Adding Hysteresis

Hysteresis extends the comparator's noise margin by increasing the upper threshold and decreasing the lower threshold. A voltage-divider from the output of the comparator sets the trip voltage. Therefore, the trip voltage is related to the output voltage.

These comparators have 4mV internal hysteresis. Additional hysteresis can be generated with two resistors using positive feedback (Figure 1). Use the following procedure to calculate resistor values:

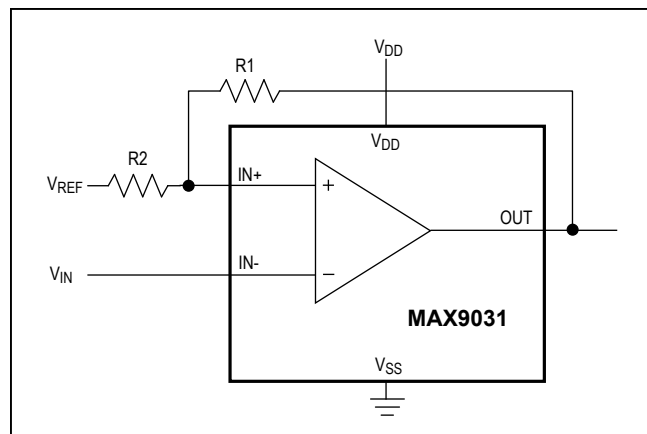


Figure 1. Additional Hysteresis

- 1) Find the trip points of the comparator using these formulas:

$$V_{TH} = V_{REF} + [(V_{DD} - V_{REF})R2] / (R1 + R2)$$

$$V_{TL} = V_{REF}(1 - (R2 / (R1 + R2)))$$

where V_{TH} is the threshold voltage at which the comparator switches its output from high to low as V_{IN} rises above the trip point. V_{TL} is the threshold voltage at which the comparator switches its output from low to high as V_{IN} drops below the trip point.

- 2) The hysteresis band will be:

$$V_{HYS} = V_{TH} - V_{TL} = V_{DD}(R2 / (R1 + R2))$$

- 3) In this example, let $V_{DD} = +5V$ and $V_{REF} = +2.5V$.

$$V_{TH} = 2.5V + 2.5(R2 / (R1 + R2))V$$

and

$$V_{TL} = 2.5[1 - (R2 / (R1 + R2))]$$

- 4) Select $R2$. In this example, we will choose $1k\Omega$.

- 5) Select V_{HYS} . In this example, we will choose $50mV$.

- 6) Solve for $R1$.

$$V_{HYS} = V_{DD}(R2 / (R1 + R2))$$

$$0.050V = 5(1000\Omega / (R1 + 1000\Omega))V$$

where $R1 \approx 100k\Omega$, $V_{TH} = 2.525V$, and $V_{TL} = 2.475V$.

The above-described design procedure assumes rail-to-rail output swing. If the output is significantly loaded, the results should be corrected.

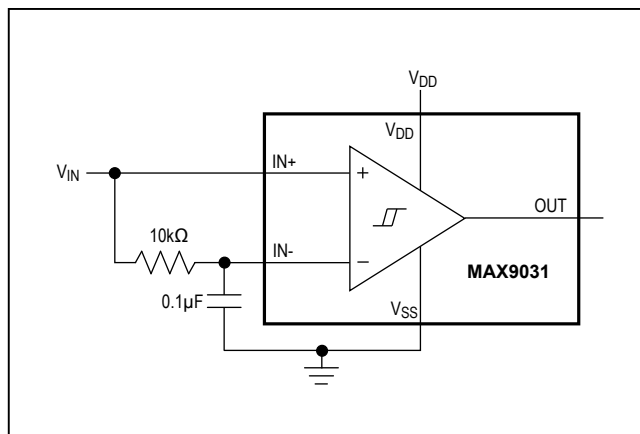


Figure 2. Time Averaging of the Input Signal for Data Recovery

Board Layout and Bypassing

Use $100nF$ bypass as a starting point. Minimize signal trace lengths to reduce stray capacitance. Minimize the capacitive coupling between $IN-$ and OUT . For slow-moving input signals (rise-time $> 1ms$), use a $1nF$ capacitor between $IN+$ and $IN-$.

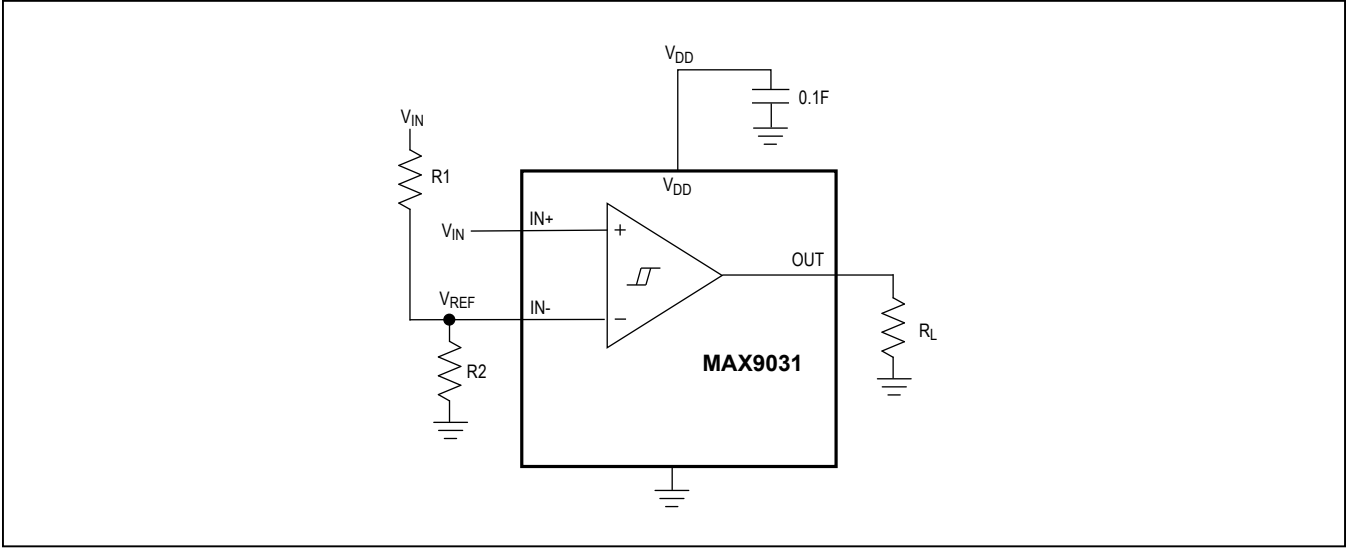
Biasing for Data Recovery

Digital data is often embedded into a bandwidth and amplitude-limited analog path. Recovering the data can be difficult. Figure 2 compares the input signal to a time-averaged version of itself. This self-biases the threshold to the average input voltage for optimal noise margin. Even severe phase distortion is eliminated from the digital output signal. Be sure to choose $R1$ and $C1$ so that:

$$f_{CAR} \gg 1 / (2\pi R1 C1)$$

where f_{CAR} is the fundamental carrier frequency of the digital data stream.

Typical Application Circuit



Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SC70	X5+1	21-0076	90-0188
6 SC70	X6SN+1	21-0077	90-0189
5 SOT23	U5+1	21-0057	90-0174
6 SOT23	U6SN+1	21-0058	90-0175
8 SOT23	K8+5	21-0078	90-0176
8 SO	S8+2	21-0041	90-0096
14 SO	S14+1	21-0041	90-0112
8 μ MAX	U8+1	21-0036	90-0092
14 TSSOP	U14+1	21-0066	90-0113

MAX9030/MAX9031/
MAX9032/MAX9034

Low-Cost, Ultra-Small, Single/Dual/Quad
Single-Supply Comparators

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/00	Initial release	—
1	5/10	Removed future product reference and added lead-free parts	1
2	8/12	Added MAX9032ASA/V+ to data sheet	1
3	4/19	Updated Package Information table	8

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at <https://www.maximintegrated.com/en/storefront/storefront.html>.

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