Absolute Maximum Ratings

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to +6.0V
- VBATT ..... -0.3V to +6.0V

All Other Inputs..... -0.3V to the higher of V_{CC} or VBATT

Continuous Input Current
- V_{CC} 100mA
- VBATT 18mA
- GND 18mA

Output Current
- $\overline{RESET}$, $\overline{PFO}$ 18mA
- V_{OUT} 100mA

Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C)..... 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C)..... 640mW

Operating Temperature Ranges
- MAX690_C_ _/MAX704_C_ _/MAX80_ _C_ _..... 0°C to +70°C
- MAX690_E_ _/MAX704_E_ _/MAX80_ _E_ _.... -40°C to +85°C
- MAX690_M_ _/MAX704_M_ _/MAX80_ _M_ _... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 3.17V to 5.5V for the MAX690T/MAX704T/MAX80_T, V_{CC} = 3.02V to 5.5V for the MAX690S/MAX704S/MAX80_S, V_{CC} = 2.72V to 5.5V for the MAX690R/MAX704R/MAX80_R; VBATT = 3.6V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{CC}, VBATT (Note 1)		MAX690_C, MAX704_C, MAX80_ _C		1.0		5.5	V
		MAX690_E/M, MAX704_E/M, MAX80_ _E/M		1.1		5.5	
V_{CC} Supply Current (excluding I_{OUT})	I_{SUPPLY}	$\overline{MR}$ = V_{CC} (MAX704_/ MAX806_)	MAX690_C/E, MAX704_C/E, MAX80_ _C/E, V_{CC} < 3.6V		40	50	µA
			MAX690_C/E, MAX704_C/E, MAX80_ _C/E, V_{CC} < 5.5V		50	65	
			MAX690_M, MAX704_M, MAX80_ _M, V_{CC} < 3.6V		40	55	
			MAX690_M, MAX704_M, MAX80_ _M, V_{CC} < 5.5V		50	70	
V_{CC} Supply Current in Battery-Backup Mode(excluding I_{OUT})		$\overline{MR}$ = V_{CC} (MAX704_/ MAX806_)	V_{CC} = 2.0V, VBATT = 2.3V		25	50	µA
VBATT Supply Current, Any Mode (excluding I_{OUT}) (Note 2)		MAX690_C/E, MAX704_C/E, MAX80_ _C/E			0.4	1	µA
		MAX690_M, MAX704_M, MAX80_ _M			0.4	10	
Battery Leakage Current (Note 3)		MAX690_C/E, MAX704_C/E, MAX80_ _C/E			0.01	0.5	µA
		MAX690_M, MAX704_M, MAX80_ _M			0.01	5	
V_{OUT} Output Voltage		MAX690_C/E, MAX704_C/E, MAX80_ _C/E, I_{OUT} = 5mA (Note 4)		V_{CC} -0.3	V_{CC} -0.015		V
		MAX690_C/E, MAX704_C/E, MAX80_ _C/E I_{OUT} = 50mA		V_{CC} -0.3	V_{CC} -0.15		
		MAX690_M, MAX704_M, MAX80_ _M I_{OUT} = 5mA (Note 4)		V_{CC} -0.035	V_{CC} -0.015		
		MAX690_M, MAX704_M, MAX80_ _M I_{OUT} = 50mA		V_{CC} -0.35	V_{CC} -0.15		
		I_{OUT} = 250µA, V_{CC} > 2.5V (Note 4)		V_{CC} -0.0015	V_{CC} -0.0006		

Electrical Characteristics (continued)

(V_{CC} = 3.17V to 5.5V for the MAX690T/MAX704T/MAX80_T, V_{CC} = 3.02V to 5.5V for the MAX690S/MAX704S/MAX80_S, V_{CC} = 2.72V to 5.5V for the MAX690R/MAX704R/MAX80_R; VBATT = 3.6V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT} in Battery-Backup Mode		I_{OUT} = 250µA, VBATT = 2.3V		VBATT - 0.1	VBATT - 0.034		V
		I_{OUT} = 1mA, VBATT = 2.3V			VBATT -0.14		
Battery Switch Threshold, V_{CC} Falling		VBATT - V_{CC}, V_{SW} > V_{CC} > 1.75V (Note 5)		65	25		mV
	V_{SW}	VBATT > V_{CC} (Note 6)		2.30	2.40	2.50	V
Battery Switch Threshold, V_{CC} Rising (Note 7)		This value is identical to the reset threshold, V_{CC} rising					V
Reset Threshold (Note 8)	V_{RST}	MAX690T/704T/805T	V_{CC} falling	3.00	3.075	3.15	V
			V_{CC} rising	3.00	3.085	3.17	
		MAX802T/804T/806T	V_{CC} falling	3.00	3.075	3.12	
			V_{CC} rising	3.00	3.085	3.14	
		MAX690S/704S/805S	V_{CC} falling	2.85	2.925	3.00	
			V_{CC} rising	2.85	2.935	3.02	
		MAX802S/804S/806S	V_{CC} falling	2.88	2.925	3.00	
			V_{CC} rising	2.88	2.935	3.02	
		MAX690R/704R/805R	V_{CC} falling	2.55	2.625	2.70	
			V_{CC} rising	2.55	2.635	2.72	
		MAX802R/804R/806S	V_{CC} falling	2.59	2.625	2.70	
			V_{CC} rising	2.59	2.635	2.72	
Reset Timeout Period	t_{WP}	V_{CC} < 3.6V		140	200	280	ms
$\overline{PFO}$, $\overline{RESET}$ Output Voltage	V_{OH}	I_{SOURCE} = 50µA		V_{CC}- 0.3	V_{CC}- 0.05		V
$\overline{PFO}$, $\overline{RESET}$ Output Short to GND Current (Note 4)	I_{OS}	V_{CC} = 3.3V, V_{OH} = 0V			180	500	µV
$\overline{PFO}$, $\overline{RESET}$, RESET Output Voltage	V_{OL}	I_{SINK} = 1.2mA; MAX690_/704_/802_/806_, V_{CC} = V_{RST} min; MAX804_/805_, V_{CC} = V_{RST} max			0.06	0.3	V
$\overline{PFO}$, $\overline{RESET}$ Output Voltage	V_{OL}	VBATT = 0V, V_{CC} = 1.0V, I_{SINK} = 40µA, MAX690_C, MAX704_C, MAX80_ _C			0.13	0.3	V
		VBATT = 0V, V_{CC} = 1.2V, I_{SINK} = 200µA, MAX690_E/M, MAX704_E/M, MAX80_ _E/M			0.17	0.3	
RESET Output Leakage Current (Note 9)		VBATT = 0V, V_{CC} = V_{RST} min; V_{RESET} = 0V, V_{CC}	MAX804_C, MAX805_C	-1		+1	µA
			MAX804_E/M, MAX805_E/M	-10		+10	

Electrical Characteristics (continued)

(V_{CC} = 3.17V to 5.5V for the MAX690T/MAX704T/MAX80_T, V_{CC} = 3.02V to 5.5V for the MAX690S/MAX704S/MAX80_S, V_{CC} = 2.72V to 5.5V for the MAX690R/MAX704R/MAX80_R; VBATT = 3.6V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PFI Input Threshold	V_{PFT}	V_{CC} < 3.6V V_{PFI} falling	MAX802_C/E, MAX804_C/E, MAX806_C/E	1.212	1.237	1.262	V
			MAX690_/MAX704_/MAX805_	1.187	1.237	1.287	
PFI Input Current		MAX690_C/E, MAX704_C/E, MAX80_ _C/E		-25	2	25	nA
		MAX690_M, MAX704_M, MAX80_ _M		-500	2	500	
PFI Hysteresis, PFI Rising	V_{PFH}	V_{CC} < 3.6V	MAX690_C/E, MAX704_C/E, MAX80_ _C/E		10	20	mV
			MAX690_M, MAX704_M, MAX80_ _M		10	25	
PFI Input Current		MAX690_C/E, MAX704_C/E, MAX80_ _C/E		-25	2	25	nA
		MAX690_M, MAX704_M, MAX80_ _M		-500	2	500	
$\overline{MR}$ Input Threshold	V_{IH}	MAX704_/MAX806_ only				0.7 x V_{CC}	V
	V_{IL}					0.3 x V_{CC}	
$\overline{MR}$ Pulse Width	t_{MR}	MAX704_/MAX806_ only		100	20		ns
$\overline{MR}$ to Reset Delay	t_{MD}	MAX704_/MAX806_ only			60	500	ns
$\overline{MR}$ Pull-Up Current		MAX704_/MAX806_ only, $\overline{MR}$ = 0V, V_{CC} = 3V		20	60	350	µA
WDI Input Threshold	V_{IH}	MAX690_/MAX802_/MAX804_/MAX805_ only				0.7 x V_{CC}	V
	V_{IL}					0.3 x V_{CC}	
WDI Input Current		0V< V_{CC} < 5.5V	MAX690_C/E, MAX802_C/E, MAX804_C/E, MAX805_C/E	-1	+0.01	+1	µA
			MAX690_M, MAX802_M, MAX804_M, MAX805_M	-10	+0.01	+10	
Watchdog Timeout Period	t_{WD}	V_{CC} < 3.6V	MAX690/MAX802/MAX804/ MAX805 only	1.12	1.60	2.24	s
WDI Pulse Width		MAX690_/MAX802_/MAX804_/MAX805_ only		100	20		ns

Note 1: V_{CC} supply current, logic input leakage, watchdog functionality (MAX690_/802_/805_/804_), $\overline{MR}$ functionality (MAX704_/806_), PFI functionality, state of $\overline{RESET}$ (MAX690_/704_/802_/806_), and RESET (MAX804_/805_) tested at VBATT = 3.6V, and V_{CC} = 5.5V. The state of $\overline{RESET}$ or RESET and $\overline{PFO}$ is tested at V_{CC} = V_{CC} min.

Note 2: Tested at VBATT = 3.6V, V_{CC} = 3.5V and 0V. The battery current will rise to 10µA over a narrow transition window around V_{CC} = 1.9V.

Note 3: Leakage current into the battery is tested under the worst-case conditions at V_{CC} = 5.5V, VBATT = 1.8V and at V_{CC} = 1.5V, VBATT= 1.0V.

Note 4: Guaranteed by design.

Note 5: When V_{SW} > V_{CC} > VBATT, V_{OUT} remains connected to V_{CC} until V_{CC} drops below VBATT. The V_{CC}-to-VBATT comparator has a small 25mV typical hysteresis to prevent oscillation. For V_{CC} < 1.75V (typ), V_{OUT} switches to VBATT regardless of the voltage on VBATT.

Note 6: When VBATT > V_{CC} > V_{SW}, V_{OUT} remains connected to V_{CC} until V_{CC} drops below the battery switch threshold (V_{SW}).

Note 7: V_{OUT} switches from VBATT to V_{CC} when V_{CC} rises above the reset threshold, independent of VBATT. Switchover back to V_{CC} occurs at the exact voltage that causes $\overline{RESET}$ to go high (on the MAX804_/805_, RESET goes low); however switchover occurs 200ms prior to reset.

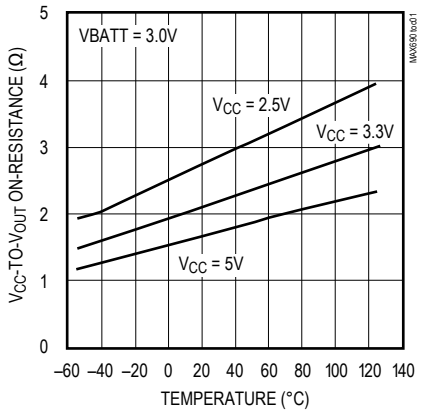
Note 8: The reset threshold tolerance is wider for V_{CC} rising than for V_{CC} falling to accommodate the 10mV typical hysteresis, which prevents internal oscillation.

Note 9: The leakage current into or out of the RESET pin is tested with RESET asserted (RESET output high impedance).

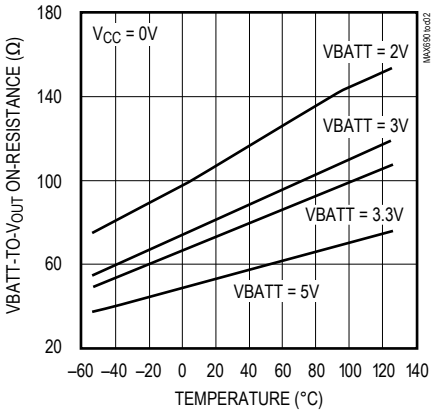
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

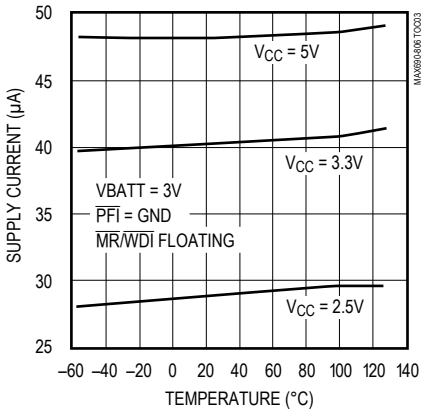
V_{CC}-TO-V_{OUT} ON-RESISTANCE vs. TEMPERATURE



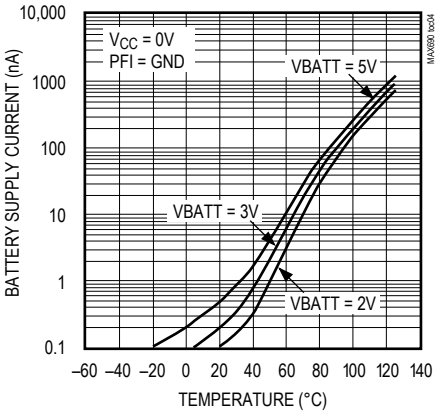
VBATT-TO-V_{OUT} ON-RESISTANCE vs. TEMPERATURE



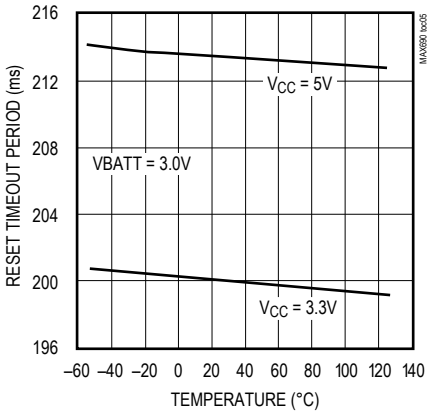
SUPPLY CURRENT vs. TEMPERATURE



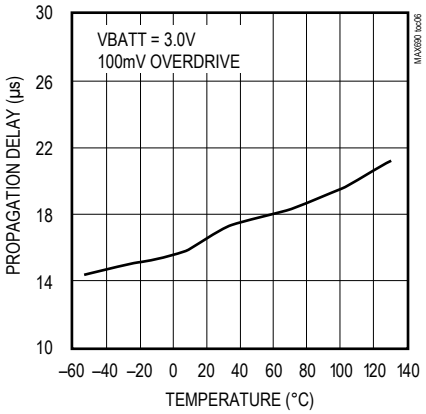
BATTERY SUPPLY CURRENT vs. TEMPERATURE



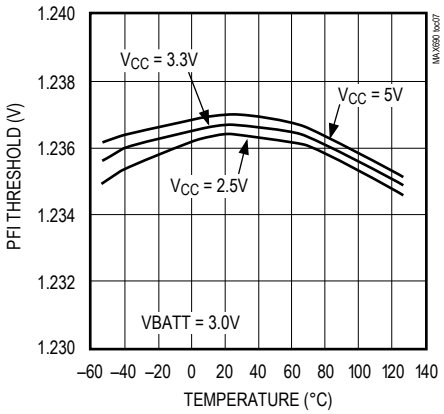
RESET TIMEOUT PERIOD vs. TEMPERATURE



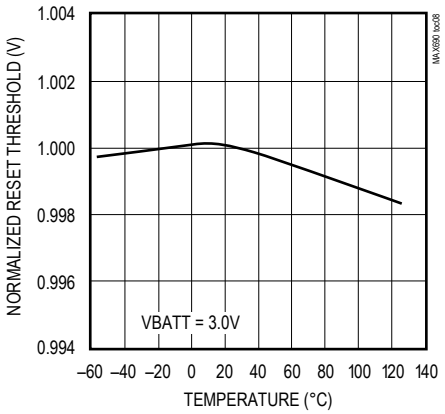
RESET-COMPARATOR PROPAGATION DELAY vs. TEMPERATURE



PFI THRESHOLD vs. TEMPERATURE



NORMALIZED RESET THRESHOLD vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
MAX690 MAX802	MAX704 MAX806	MAX804 MAX805		
1	1	1	V_{OUT}	Supply Output for CMOS RAM. When V_{CC} is above the reset threshold, V_{OUT} is connected to V_{CC} through a p-channel MOSFET switch. When V_{CC} falls below V_{SW} and VBATT, VBATT connects to V_{OUT}. Connect to V_{CC} if no battery is used.
2	2	2	V_{CC}	Main Supply Input
3	3	3	GND	Ground
4	4	4	PFI	Power-Fail Input. When PFI is less than V_{PFT} or when V_{CC} falls below V_{SW}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high. Connect to ground if unused.
5	5	5	$\overline{PFO}$	Power-Fail Output. When PFI is less than V_{PFT}, or V_{CC} falls below V_{SW}, $\overline{PFO}$ goes low; otherwise, $\overline{PFO}$ remains high. Leave open if unused.
6	—	6	WDI	Watchdog Input. If WDI remains high or low for 1.6s, the internal watchdog timer runs out and reset is triggered. The internal watchdog timer clears while reset is asserted or when WDI sees a rising or falling edge. The watchdog function cannot be disabled.
—	6	—	$\overline{MR}$	Manual Reset Input. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted as long as $\overline{MR}$ is low and for 200ms after $\overline{MR}$ returns high. This active-low input has an internal 70µA pullup current. It can be driven from a TTL or CMOS logic line, or shorted to ground with a switch. Leave open if unused.
7	7	—	$\overline{RESET}$	Active-Low Reset Output. Pulses low for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold or when $\overline{MR}$ is a logic low. It remains low for 200ms after either V_{CC} rises above the reset threshold, the watchdog triggers a reset, or $\overline{MR}$ goes from low to high.
—	—	7	$\overline{RESET}$	Active-High, Open-Drain Reset Output is the inverse of $\overline{RESET}$.
8	8	8	VBATT	Backup-Battery Input. When V_{CC} falls below V_{SW} and VBATT, V_{OUT} switches from V_{CC} to VBATT. When V_{CC} rises above the reset threshold, V_{OUT} reconnects to V_{CC}. VBATT may exceed V_{CC}. Connect to V_{CC} if no battery is used.

Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. These µP supervisory circuits assert reset to prevent code execution errors during power-up, power-down, brownout conditions, or a watchdog timeout.

$\overline{RESET}$ is guaranteed to be a logic low for 0V < V_{CC} < V_{RST}, provided that VBATT is greater than 1V. Without a backup battery, $\overline{RESET}$ is guaranteed valid for V_{CC} > 1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for the reset timeout period; after this interval, $\overline{RESET}$ goes high (Figure 2).

If a brownout condition occurs (V_{CC} dips below the reset threshold), $\overline{RESET}$ goes low. Each time $\overline{RESET}$ is asserted, it stays low for the reset timeout period. Any time V_{CC} goes below the reset threshold, the internal timer restarts.

The watchdog timer can also initiate a reset. See the *Watchdog Input* section.

The MAX804_/MAX805_ active-high RESET output is open drain, and the inverse of the MAX690_/MAX704_/MAX802_/MAX806_ $\overline{RESET}$ output.

Reset Threshold

The MAX690T/MAX704T/MAX805T are intended for 3.3V systems with a ±5% power-supply tolerance and a 10% system tolerance. Except for watchdog faults, reset will not assert as long as the power supply remains above 3.15V (3.3V - 5%). Reset is guaranteed to assert before the power supply falls below 3.0V.

The MAX690S/MAX704S/MAX805S are designed for 3.3V ±10% power supplies. Except for watchdog faults, they are guaranteed not to assert reset as long as the supply remains above 3.0V (3.3V - 10%). Reset is guaranteed to assert before the power supply falls below 2.85V (V_{CC} - 14%).

The MAX690R/MAX704R/MAX805R are optimized for monitoring 3.0V ±10% power supplies. Reset will not occu$_r$ until V_{CC} falls below 2.7V (3.0V - 10%), but is guaranteed to occur before the supply falls below 2.59V (3.0V - 14%).

The MAX802R/S/T, MAX804R/S/T, and MAX806R/S/T are respectively similar to the MAX690R/S/T, MAX805R/S/T, and MAX704R/S/T, but with tightened reset and power-fail threshold tolerances.

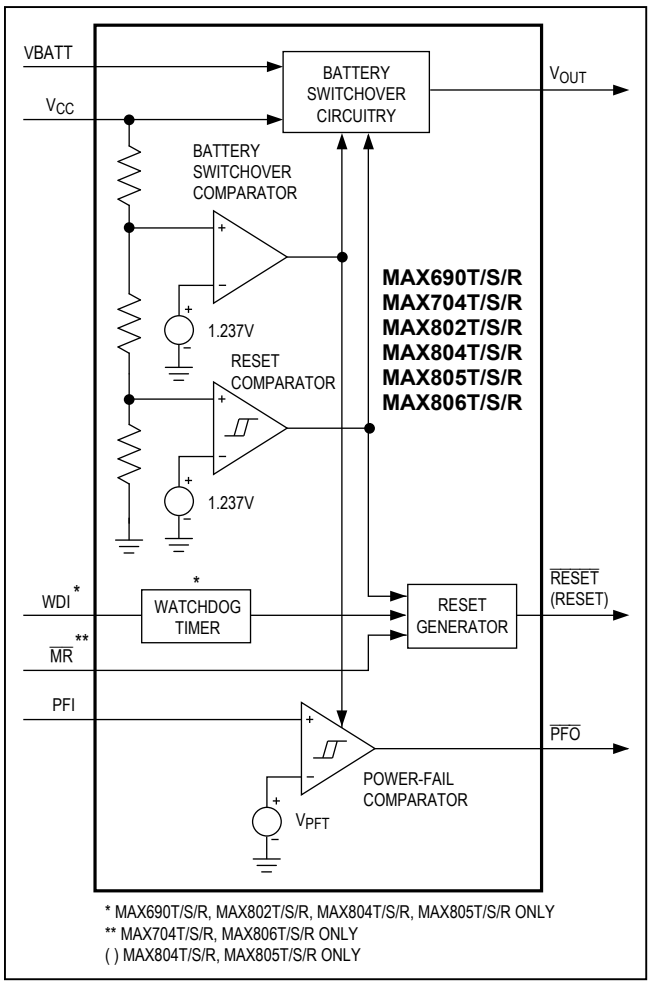


Figure 1. Block Diagram

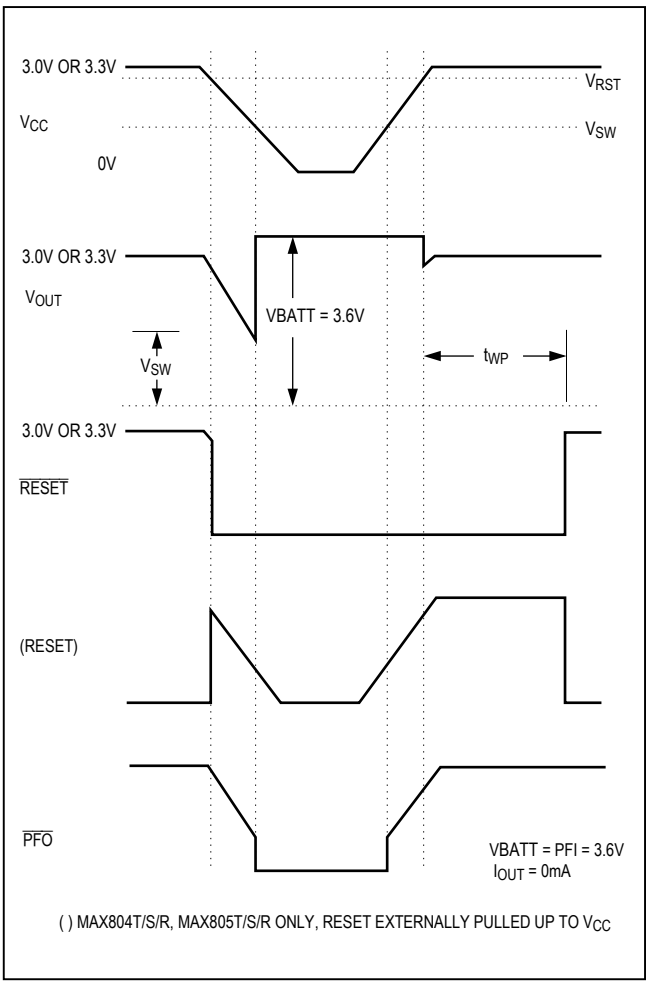


Figure 2. Timing Diagram

Watchdog Input (MAX690_/802_/804_/805_)

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec, a reset pulse is triggered. The internal 1.6sec timer is cleared by either a reset pulse or by a transition (low-to-high or high-to-low) at WDI. If WDI is tied high or low, a $\overline{RESET}$ pulse is triggered every 1.8sec (t_{WD} plus t_{RS}).

As long as reset is asserted, the timer remains cleared and does not count. As soon as reset is deasserted, the timer starts counting. Unlike the 5V MAX690 family, the watchdog function **cannot** be disabled.

Power-Fail Comparator

The PFI input is compared to an internal reference. If PFI is less than V_{PFT}, $\overline{PFO}$ goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply. However, the comparator does not need to be dedicated to this function because it is completely separate from the rest of the circuitry.

The power-fail comparator turns off and $\overline{PFO}$ goes low when V_{CC} falls below V_{SW} on power-down. The power-fail comparator turns on as V_{CC} crosses V_{SW} on power-up. If the comparator is not used, connect PFI to ground and leave $\overline{PFO}$ unconnected. $\overline{PFO}$ can be connected to $\overline{MR}$ on the MAX704_/MAX806_ so that a low voltage on PFI will generate a reset (Figure 5b).

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a back-up battery installed at VBATT, the devices automatically switch RAM to backup power when V_{CC} falls.

This family of µP supervisors (designed for 3.3V and 3V systems) doesn't always connect VBATT to V_{OUT} when VBATT is greater than V_{CC}. VBATT connects to V_{OUT} (through a 140Ω switch) when V_{CC} is below V_{SW} **and** VBATT is greater than V_{CC}, or when V_{CC} falls below 1.75V (typ) regardless of the VBATT voltage. This is done to allow the backup battery (e.g., a 3.6V lithium cell) to have a higher voltage than V_{CC}.

Switchover at V_{SW} (2.40V) ensures that battery-backup mode is entered before V_{OUT} gets too close to the 2.0V minimum required to reliably retain data in CMOS RAM. Switchover at higher V_{CC} voltages would decrease backup-battery life. When V_{CC} recovers, switchover is deferred until V_{CC} rises above the reset threshold (V_{RST}) to ensure a stable supply. V_{OUT} is connected to V_{CC} through a 3Ω PMOS power switch.

Manual Reset

A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for t_{WP} (200ms) after $\overline{MR}$ returns high. This input has an internal 70µA pullup current, so it can be left open if it is not used. $\overline{MR}$ can be driven with TTL or CMOS logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual-reset function; external debounce circuitry is not required.

Table 1. Input and Output Status in Battery-Backup Mode

PIN NAME	STATUS
V_{OUT}	Connected to VBATT through an internal 140Ω switch
V_{CC}	Disconnected from V_{OUT}
PFI	The power-fail comparator is disabled when $V_{CC} < V_{SW}$
$\overline{PFO}$	Logic low when $V_{CC} < V_{SW}$ or PFI < V_{PFT}
WDI	The watchdog timer is disabled
$\overline{MR}$	Disabled
$\overline{RESET}$	Low logic
RESET	High impedance
VBATT	Connected to V_{OUT}

Applications Information

These µP supervisory circuits are not short-circuit protected. Shorting V_{OUT} to ground—excluding power-up transients such as charging a decoupling capacitor—destroys the device. Decouple both V_{CC} and VBATT pins to ground by placing 0.1µF capacitors as close as possible to the device.

Using a SuperCap as a Backup Power Source

SuperCaps are capacitors with extremely high capacitance values (e.g., order of 0.47F) for their size. Figure 3 shows two ways to use a SuperCap as a backup power source. The SuperCap may be connected through a diode to the 3V input (Figure 3a) or, if a 5V supply is also available, the SuperCap may be charged up to the 5V supply (Figure 3b) allowing a longer backup period. Since VBATT can exceed V_{CC} while V_{CC} is a bove the reset threshold, there are no special precautions when using these µP supervisors with a SuperCap.

Operation without a Backup Power Source

These µP supervisors were designed for battery-backed applications. If a backup battery is not used, connect both VBATT and V_{OUT} to V_{CC}, or use a different µP supervisor such as the MAX706T/S/R or MAX708T/S/R.

Replacing the Backup Battery

The backup power source can be removed while V_{CC} remains valid, if VBATT is decoupled with a 0.1µF capacitor to ground, without danger of triggering RESET/$\overline{RESET}$. As long as V_{CC} stays above V_{SW}, battery-back-up mode cannot be entered.

Adding Hysteresis to the Power-Fail Comparator

The power-fail comparator has a typical input hysteresis of 10mV. This is sufficient for most applications where a power-supply line is being monitored through an external voltage divider (see the *Monitoring an Additional Power Supply* section).

If additional noise margin is desired, connect a resistor between $\overline{PFO}$ and PFI as shown in Figure 4a. Select the ratio of R1 and R2 such that PFI sees 1.237V (V_{PFT}) when V_{IN} falls to its trip point (V_{TRIP}). R3 adds the hysteresis and will typically be more than 10 times the value of R1 or R2. The hysteresis window extends both above (V_H) and below (V_L) the original trip point (V_{TRIP}).

Connecting an ordinary signal diode in series with R3, as shown in Figure 4b, causes the lower trip point (V_L) to

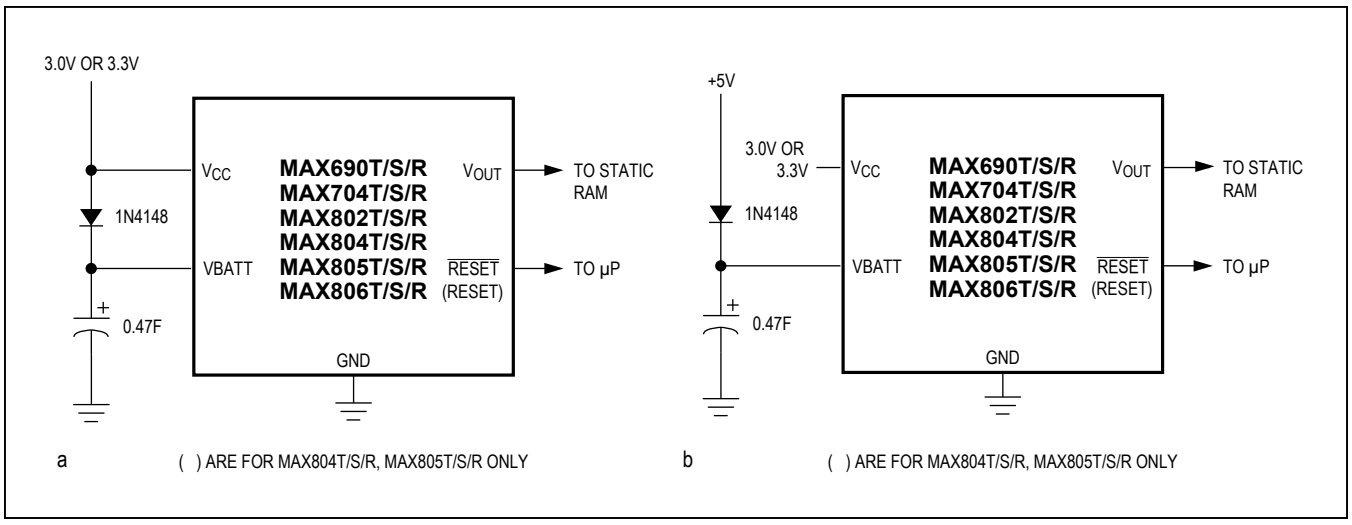


Figure 3. Using a SuperCap as a Backup Power Source

coincide with the trip point without hysteresis (V_{TRIP}), so the entire hysteresis window occurs above V_{TRIP}. This method provides additional noise margin without compromising the accuracy of the power-fail threshold when the monitored voltage is falling. It is useful for accurately detecting when a voltage falls past a threshold.

The current through R1 and R2 should be at least 1µA to ensure that the 25nA (max over extended temperature range) PFI input current does not shift the trip point. R3 should be larger than 10kΩ so it does not load down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring an Additional Power Supply

These µP supervisors can monitor either positive or negative supplies using a resistor voltage divider to PFI. $\overline{PFO}$ can be used to generate an interrupt to the µP (Figure 5). Connecting $\overline{PFO}$ to $\overline{MR}$ on the MAX704 and MAX806 causes reset to assert when the monitored supply goes out of tolerance. Reset remains asserted as long as $\overline{PFO}$ holds $\overline{MR}$ low, and for 200ms after $\overline{PFO}$ goes high.

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the MAX690_/MAX704_/MAX802_/MAX806_ $\overline{RESET}$ output. If, for example, the $\overline{RESET}$ output is driven high and the µP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{RESET}$ output and the µP reset I/O, as in Figure 6. Buffer the $\overline{RESET}$ output to other system components.

Negative-Going V_{CC} Transients

While issuing resets to the µP during power-up, power-down, and brownout conditions, these supervisors are relatively immune to short-duration negative-going V_{CC} transients (glitches). It is usually undesirable to reset the µP when V_{CC} experiences only small glitches.

Figure 7 shows maximum transient duration vs. reset-comparator overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going V_{CC} pulses, starting at 3.3V and ending below the reset threshold by the magnitude indicated (reset comparator overdrive). The graph shows the maximum pulse width a negative-going V_{CC} transient may typically have without causing a reset pulse to be issued. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 40µs or less will not cause a reset pulse to be issued.

A 100nF bypass capacitor mounted close to the V_{CC} pin provides additional transient immunity.

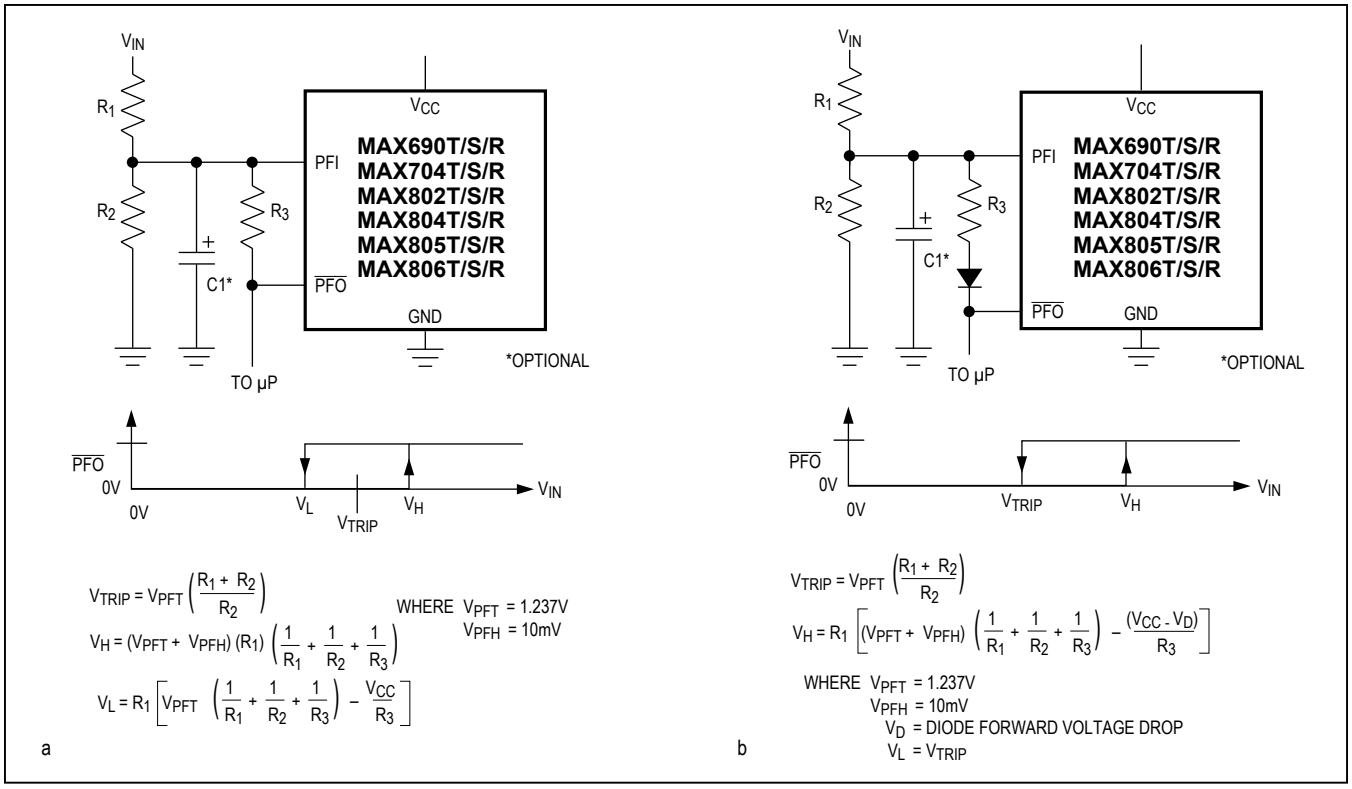


Figure 4. a) Adding Additional Hysteresis to the Power-Fail Comparator b) Shifting the Additional Hysteresis above V_{PFT}

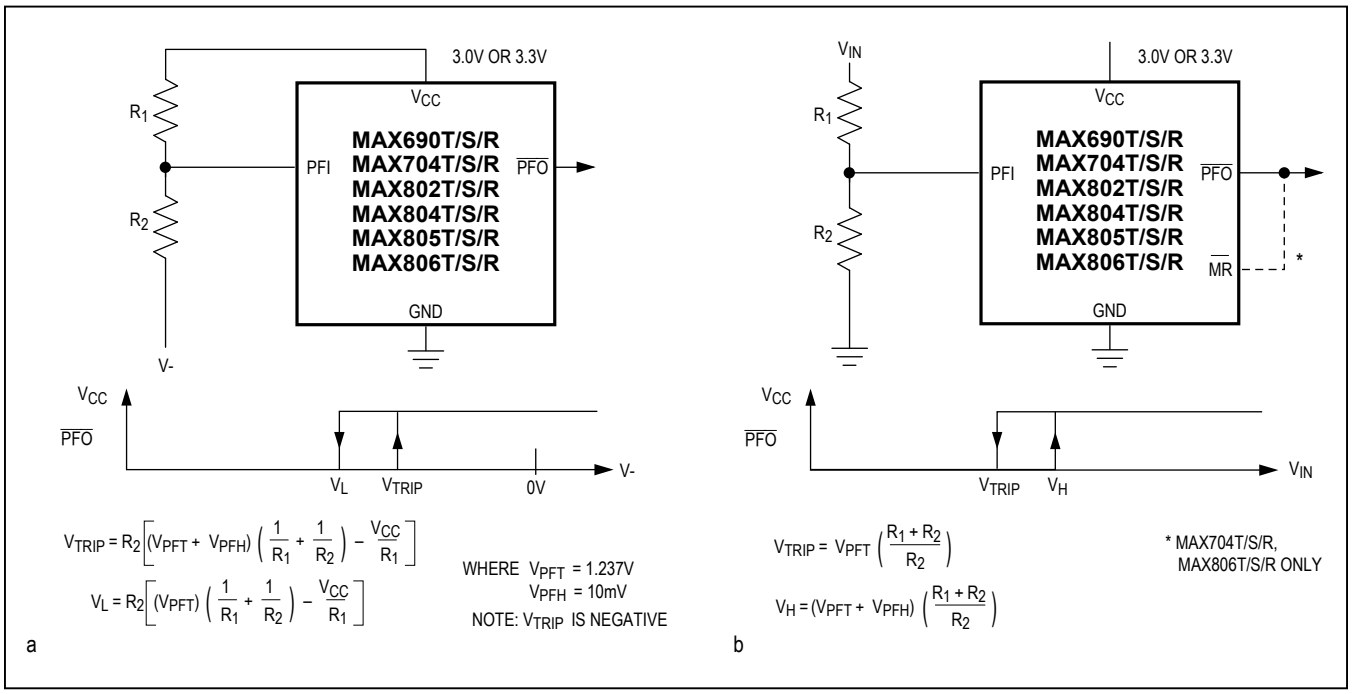


Figure 5. Using the Power-Fail Comparator to Monitor an Additional Power Supply

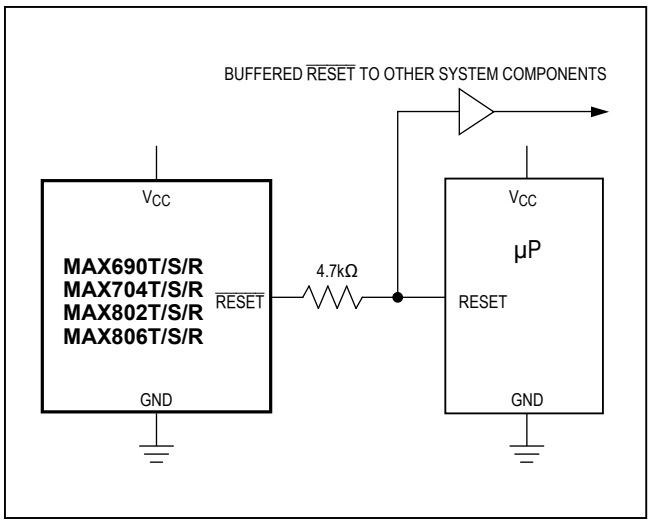


Figure 6. Interfacing to µPs with Bidirectional Reset I/O

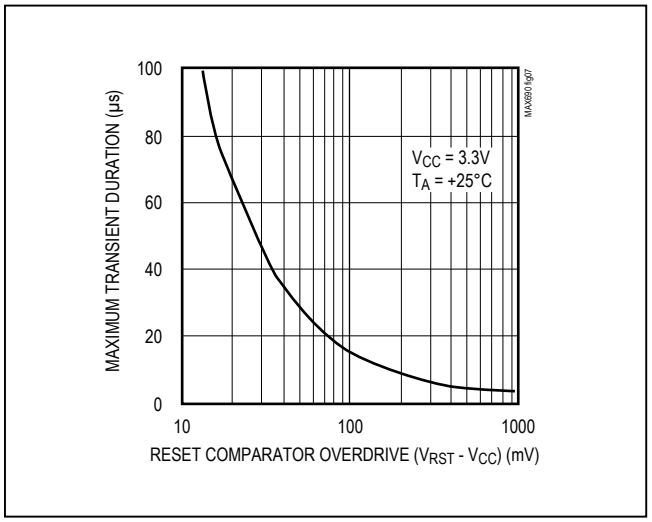


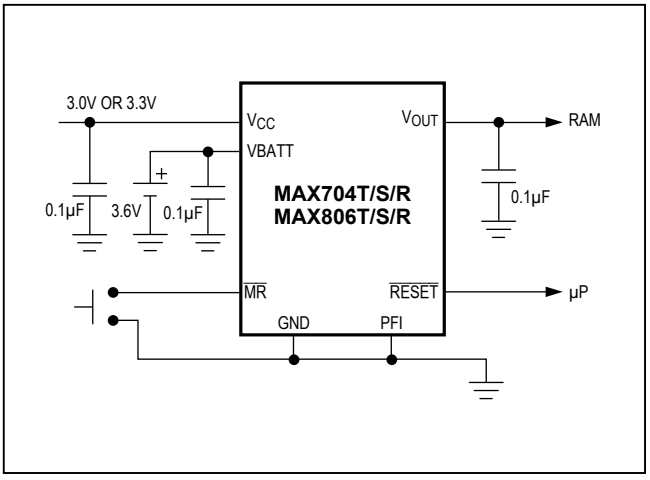
Figure 7. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

Chip Information

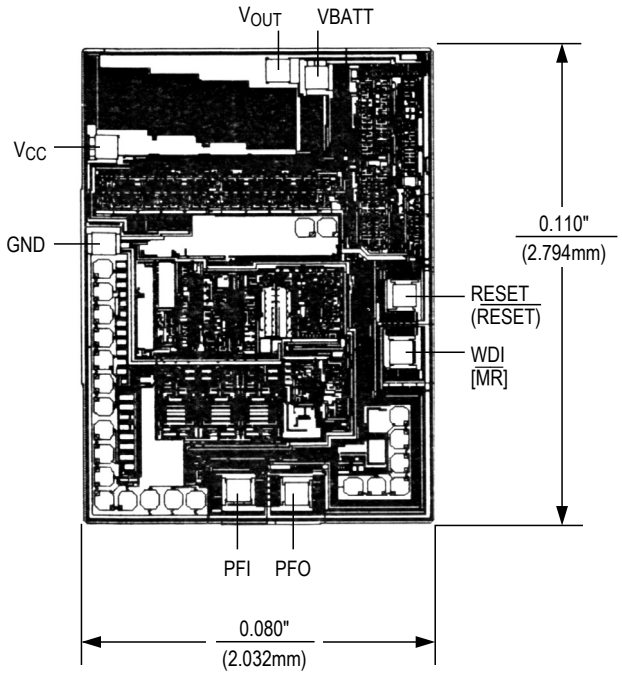
TRANSISTOR COUNT: 802;

SUBSTRATE IS CONNECTED TO THE HIGHER OF V_{CC} OR VBATT, AND MUST BE FLOATED IN ANY HYBRID DESIGN.

Typical Operating Circuits (continued)

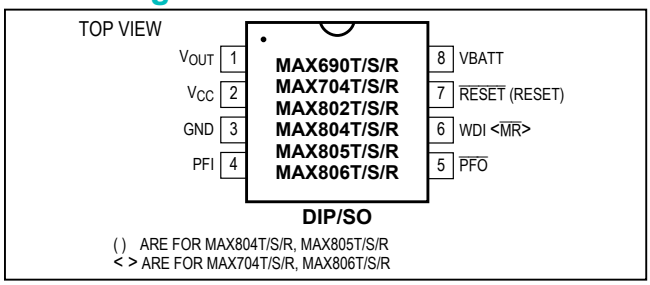


Chip Topography



( ) ARE FOR MAX804T/S/R, MAX805T/S/R.
[ ] ARE FOR MAX704T/S/R, MAX806T/S/R.

Pin Configuration



Package Information

For the latest package outline information and land patterns, go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE e CODE	OUTLINE NO.	LAND PATTERN NO.
8 PDIP	P8+2	21-0043	—
8 CDIP	J8+2	21-0045	—
8 SOIC	S8+4	21-0041	90-0096

Ordering Information (continued)

PART**	TEMP RANGE	PIN-PACKAGE
MAX704_CPA	0°C to +70°C	8 Plastic DIP
MAX704_CSA	0°C to +70°C	8 SO
MAX704_C/D	0°C to +70°C	Dice*
MAX704_EPA	-40°C to +85°C	8 Plastic DIP
MAX704_ESA	-40°C to +85°C	8 SO
MAX704_MJA	-55°C to +125°C	8 CERDIP
MAX802_CPA	0°C to +70°C	8 Plastic DIP
MAX802_CSA	0°C to +70°C	8 SO
MAX802_C/D	0°C to +70°C	Dice*
MAX802_EPA	-40°C to +85°C	8 Plastic DIP
MAX802_ESA	-40°C to +85°C	8 SO
MAX802_MJA	-55°C to +125°C	8 CERDIP
MAX804_CPA	0°C to +70°C	8 Plastic DIP
MAX804_CSA	0°C to +70°C	8 SO
MAX804_C/D	0°C to +70°C	Dice*
MAX804_EPA	-40°C to +85°C	8 Plastic DIP
MAX804_ESA	-40°C to +85°C	8 SO
MAX804_MJA	-55°C to +125°C	8 CERDIP
MAX805_CPA	0°C to +70°C	8 Plastic DIP
MAX805_CSA	0°C to +70°C	8 SO
MAX805_C/D	0°C to +70°C	Dice*
MAX805_EPA	-40°C to +85°C	8 Plastic DIP
MAX805_ESA	-40°C to +85°C	8 SO
MAX805_MJA	-55°C to +125°C	8 CERDIP
MAX806_CPA	0°C to +70°C	8 Plastic DIP
MAX806_CSA	0°C to +70°C	8 SO
MAX806_C/D	0°C to +70°C	Dice*
MAX806_EPA	-40°C to +85°C	8 Plastic DIP
MAX806_ESA	-40°C to +85°C	8 SO
MAX806_MJA	-55°C to +125°C	8 CERDIP

*Contact factory for dice specifications.

**These parts offer a choice of reset threshold voltage. Select the letter corresponding to the desired nominal reset threshold voltage (T = 3.075V, S = 2.925V, R = 2.625V) and insert it into the blank to complete the part number.

Devices in PDIP and SO packages are available in both leaded and lead(Pb)-free packaging. Specify lead free by adding the + symbol at the end of the part number when ordering. Lead free not available for CERDIP package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	4/15	No /V OPNs in *Ordering Information*; deleted Automotive Systems in *Applications Information* section; added *Package Information* and *Revision History* tables	1, 12, 13

