

20-Output, 76V, Serial-Interfaced VFD Tube Drivers

ABSOLUTE MAXIMUM RATINGS

Voltage (with respect to GND)	
V _{BB}	-0.3V to +80V
V _{CC}	-0.3V to +6V
V _{SS} (MAX6931 only)	-12V to +0.3V
V _{BB} - V _{SS} (MAX6931 only)	-0.3V to +80V
OUT ₋ (MAX6921 only)	(GND - 0.3V) to (V _{BB} + 0.3V)
OUT ₋ (MAX6931 only)	(V _{SS} - 0.3V) to (V _{BB} + 0.3V)
All Other Pins	-0.3V to (V _{CC} + 0.3V)
OUT ₋ Continuous Source Current	-45mA
OUT ₋ Pulsed (1ms max, 1/4 max duty) Source Current	-80mA
Total OUT ₋ Continuous Source Current	-540mA
Total OUT ₋ Continuous Sink Current	90mA
Total OUT ₋ Pulsed (1ms max, 1/4 max duty) Source Current	-960mA
OUT ₋ Sink Current	15mA
CLK, DIN, LOAD, BLANK, DOUT Current	±10mA
Continuous Power Dissipation (T _A = +70°C)	
28-Pin TSSOP (derate 12.8mW/°C over +70°C)	1025mW
28-Pin Wide SO (derate 12.5mW/°C over +70°C)	1000mW
28-Pin PLCC (derate 10.5mW/°C over +70°C)	842mW
Operating Temperature Range (T _{MIN} to T _{MAX})	-40°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	
Wide SO, TSSOP lead(Pb)-free	+260°C
PLCC lead(Pb)-free	+245°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Typical Operating Circuit, V_{BB} = 8V to 76V, V_{CC} = 3V to 5.5V, V_{SS} = -11V to 0V, V_{BB} - V_{SS} ≤ 76V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Supply Voltage	V _{CC}		3		5.5	V
Tube Supply Voltage	V _{BB}		8		76	V
Bias Supply Voltage (MAX6931 Only)	V _{SS}		-11		0	V
Total Supply Voltage (MAX6931 Only)	V _{BB} - V _{SS}				76	V
Logic Supply Operating Current	I _{CC}	All outputs OUT ₋ low, CLK = idle	T _A = +25°C		78	μA
			T _A = -40°C to +125°C		200	
		All outputs OUT ₋ high, CLK = idle	T _A = +25°C		540	
			T _A = -40°C to +125°C		1000	
Tube Supply Operating Current	I _{BB}	All outputs OUT ₋ low	T _A = +25°C		1.65	mA
			T _A = -40°C to +125°C		6.9	
		All outputs OUT ₋ high	T _A = +25°C		0.85	
			T _A = -40°C to +125°C		1.4	
Bias Supply Operating Current (MAX6931 Only)	I _{SS}	All outputs OUT ₋ low	T _A = +25°C		-0.8	mA
			T _A = -40°C to +125°C		-1.9	
		All outputs OUT ₋ high	T _A = +25°C		-1.4	
			T _A = -40°C to +125°C		-1.5	

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MAX6921/MAX6931

ELECTRICAL CHARACTERISTICS (continued)

(Typical Operating Circuit, $V_{BB} = 8V$ to $76V$, $V_{CC} = 3V$ to $5.5V$, $V_{SS} = -11V$ to $0V$, $V_{BB} - V_{SS} \leq 76V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
High-Voltage OUT ₋		V _{BB} ≥ 15V I _{OUT} = -25mA	T _A = +25°C	V _{BB} - 2		V	
			T _A = -40°C to +85°C	V _{BB} - 2.5			
			T _A = -40°C to +125°C				
		V _{BB} ≥ 15V I _{OUT} = -40mA	T _A = -40°C to +85°C	V _{BB} - 3.5			
			T _A = -40°C to +125°C	V _{BB} - 4.0			
		8V < V _{BB} < 15V I _{OUT} = -25mA	T _A = +25°C	V _{BB} - 1.2			
			T _A = -40°C to +85°C	V _{BB} - 2.5			
			T _A = -40°C to +125°C	V _{BB} - 3.0			
Low-Voltage OUT ₋ (MAX6921 Only)	V _L	V _{BB} ≥ 15V I _{OUT} = 1mA	T _A = +25°C	0.75	1	V	
			T _A = -40°C to +85°C	1.5			
			T _A = -40°C to +125°C	1.9			
		8V < V _{BB} < 15V I _{OUT} = 1mA	T _A = +25°C	0.8	1.1		
			T _A = -40°C to +85°C	1.6			
			T _A = -40°C to +125°C	2.0			
Low-Voltage OUT ₋ (MAX6931 Only)	V _L	V _{BB} ≥ 15V I _{OUT} = 1mA	T _A = +25°C	V _{SS} + 0.75 V _{SS} + 1		V	
			T _A = -40°C to +85°C	V _{SS} + 1.5			
			T _A = -40°C to +125°C	V _{SS} + 1.9			
		8V < V _{BB} < 15V I _{OUT} = 1mA	T _A = +25°C	V _{SS} + 0.8 V _{SS} + 1.1			
			T _A = -40°C to +85°C	V _{SS} + 1.6			
			T _A = -40°C to +125°C	V _{SS} + 2.0			
Rise Time OUT ₋ (20% to 80%)	t _R	V _{BB} = 60V, C _L = 50pF, R _L =2.3kΩ		0.9	2	μs	
Fall Time OUT ₋ (80% to 20%)	t _F	V _{BB} = 60V, C _L = 50pF, R _L =2.3kΩ		0.6	1.5	μs	
SERIAL INTERFACE TIMING CHARACTERISTICS							
LOAD Rising to OUT ₋ Falling Delay		(Notes 2, 3)		0.9	1.8	μs	
LOAD Rising to OUT ₋ Rising Delay		(Notes 2, 3)		1.2	2.4	μs	
BLANK Rising to OUT ₋ Falling Delay		(Notes 2, 3)		0.9	1.8	μs	
BLANK Falling to OUT ₋ Rising Delay		(Notes 2, 3)		0.5	1.3	2.5	μs
Input Leakage Current CLK, DIN, LOAD, BLANK	I _{IH} , I _{IL}			0.05	10	μA	
Logic-High Input Voltage CLK, DIN, LOAD, BLANK	V _{IH}			0.8 x V _{CC}		V	
Logic-Low Input Voltage CLK, DIN, LOAD, BLANK	V _{IL}			0.3 x V _{CC}		V	
Hysteresis Voltage DIN, CLK, LOAD, BLANK	ΔV _I			0.6		V	
High-Voltage DOUT	V _{OH}	I _{SOURCE} = -1.0mA		V _{CC} - 0.5		V	
Low-Voltage DOUT	V _{OL}	I _{SINK} = 1.0mA		0.5		V	

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ELECTRICAL CHARACTERISTICS (continued)

(Typical Operating Circuit, $V_{BB} = 8V$ to $76V$, $V_{CC} = 3V$ to $5.5V$, $V_{SS} = -11V$ to $0V$, $V_{BB} - V_{SS} \leq 76V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise and Fall Time DOUT		$C_{DOUT} = 10pF$ (Note 2)				
		3V to 4.5V		60	100	ns
		4.5V to 5.5V		30	80	ns
CLK Clock Period	t_{CP}		200			ns
CLK Pulse-Width High	t_{CH}		90			ns
CLK Pulse-Width Low	t_{CL}		90			ns
CLK Rise to LOAD Rise Hold	t_{CSH}	(Note 2)	100			ns
DIN Setup Time	t_{DS}		5			ns
DIN Hold Time	t_{DH}	3.0V to 4.5V	20			ns
		4.5V to 5.5V	15			ns
DOUT Propagation Delay	t_{DO}	$C_{DOUT} = 10pF$				
		3.0V to 4.5V	25	120	240	ns
		4.5V to 5.5V	20	75	150	ns
LOAD Pulse High	t_{CSW}		55			ns

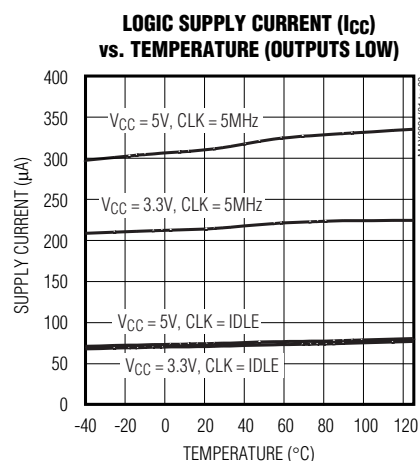
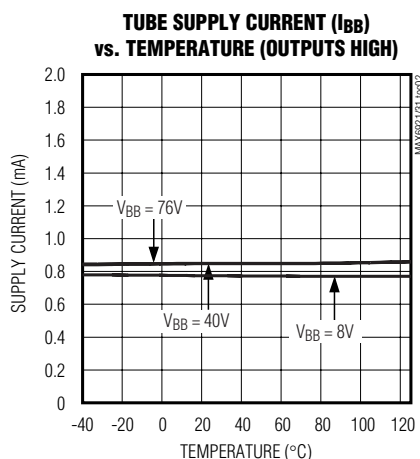
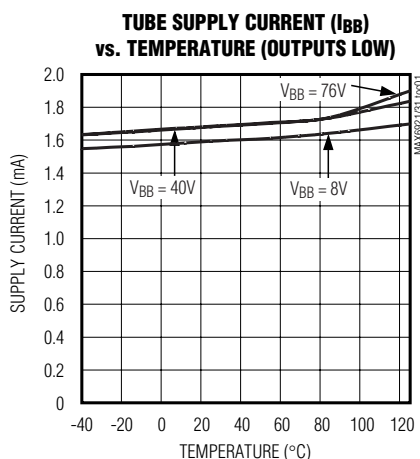
Note 1: All parameters are tested at $T_A = +25^\circ C$. Specifications over temperature are guaranteed by design.

Note 2: Guaranteed by design.

Note 3: Delay measured from control edge to when output OUT_+ changes by 1V.

Typical Operating Characteristics

($V_{CC} = 5.0V$, $V_{BB} = 76V$, and $T_A = +25^\circ C$, unless otherwise noted.)

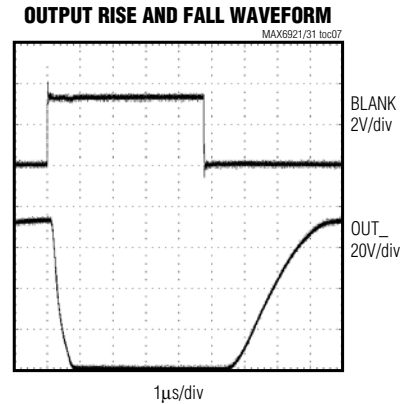
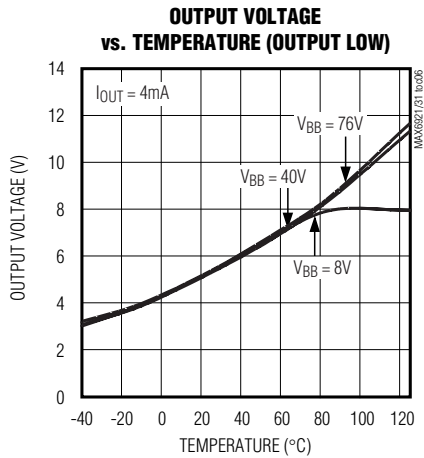
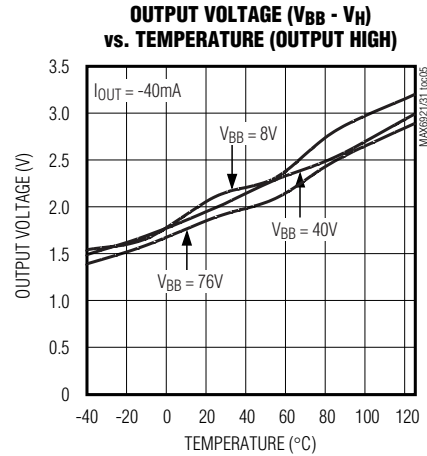
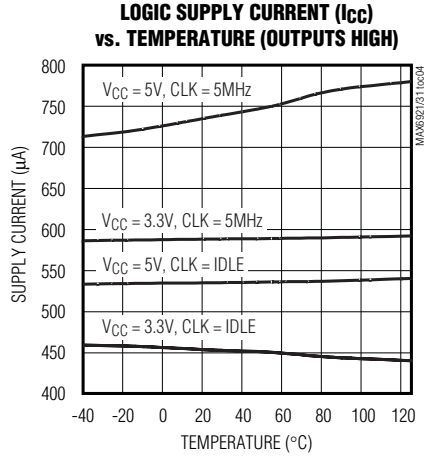


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MAX6921/MAX6931

Typical Operating Characteristics (continued)

($V_{CC} = 5.0V$, $V_{BB} = 76V$, and $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN			NAME	FUNCTION
TSSOP		WIDE SO/PLCC		
MAX6921	MAX6931	MAX6921		
1-5	1-5	—	OUT4 to OUT0	VFD Anode and Grid Drivers. OUT4 to OUT0 are push-pull outputs swinging from V_{BB} to GND (MAX6921 only), and from V_{BB} to V_{SS} (MAX6931 only).
6	6	27	DIN	Serial-Data Input. Data is loaded into the internal shift register on CLK's rising edge.
7	7	28	V_{CC}	Logic Supply Voltage. Bypass to GND with 100nF capacitor.
8	8	1	V_{BB}	VFD Tube Supply Voltage. Bypass to GND with 100nF capacitor.
9	—	2	DOUT	Serial-Clock Output. Data is clocked out of the internal shift register to DOUT on CLK's rising edge.

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Pin Description (continued)

PIN			NAME	FUNCTION
TSSOP		WIDE SO/PLCC		
MAX6921	MAX6931	MAX6921		
—	9	—	V _{SS}	Filament Bias Supply Voltage. Bypass to GND with a 100nF capacitor.
10–19	10–19	—	OUT19 to OUT10	VFD Anode and Grid Drivers. OUT19 to OUT10 are push-pull outputs swinging from V _{BB} to GND (MAX6921 only), and from V _{BB} to V _{SS} (MAX6931 only).
—	—	3–12	OUT19 to OUT10	VFD Anode and Grid Drivers. OUT19 to OUT10 are push-pull outputs swinging from V _{BB} to GND.
20	20	13	BLANK	Blanking Input. High forces outputs OUT0 to OUT19 low, without altering the contents of the output latches. Low enables outputs OUT0 to OUT19 to follow the state of the output latches.
21	21	14	GND	Ground
22	22	15	CLK	Serial-Clock Input. Data is loaded into the internal shift register on CLK's rising edge.
23	23	16	LOAD	Load Input. Data is loaded transparently from the internal shift register to the output latch while LOAD is high. Data is latched into the output latch on LOAD's rising edge, and retained while LOAD is low.
24–28	24–28	—	OUT9 to OUT5	VFD Anode and Grid Drivers. OUT9 to OUT5 are push-pull outputs swinging from V _{BB} to GND (MAX6921 only), and from V _{BB} to V _{SS} (MAX6931 only).
—	—	17–26	OUT9 to OUT0	VFD Anode and Grid Drivers. OUT9 to OUT0 are push-pull outputs swinging from V _{BB} to GND.

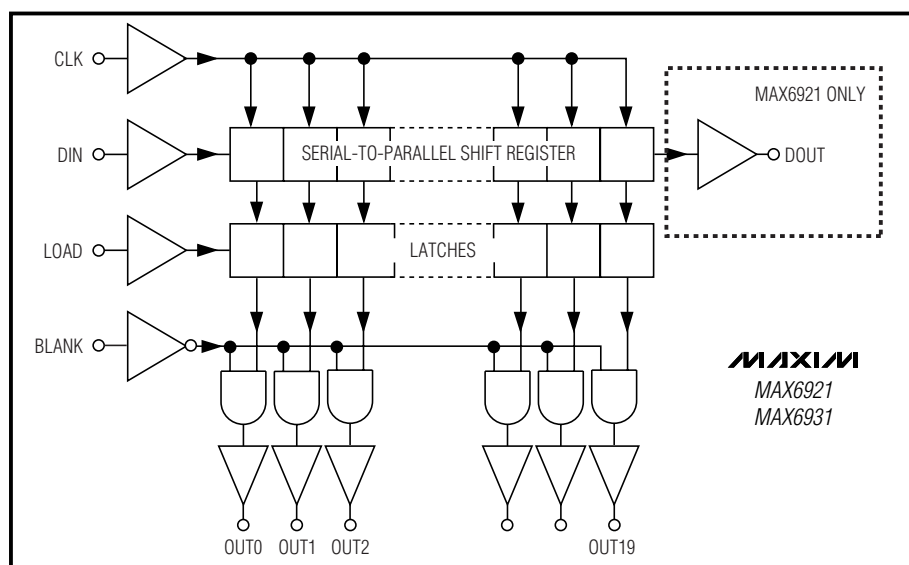


Figure 1. MAX6921/MAX6931 Functional Diagram

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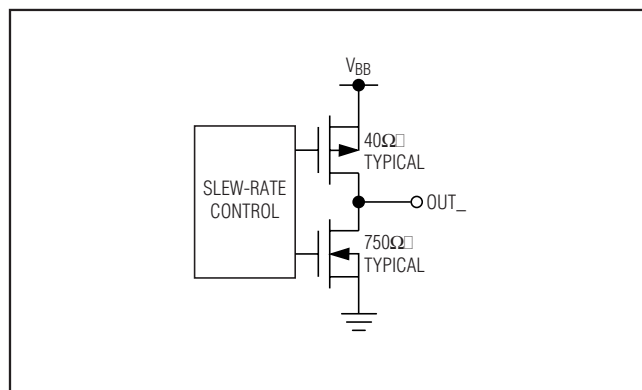


Figure 2. MAX6921 CMOS Output Driver Structure

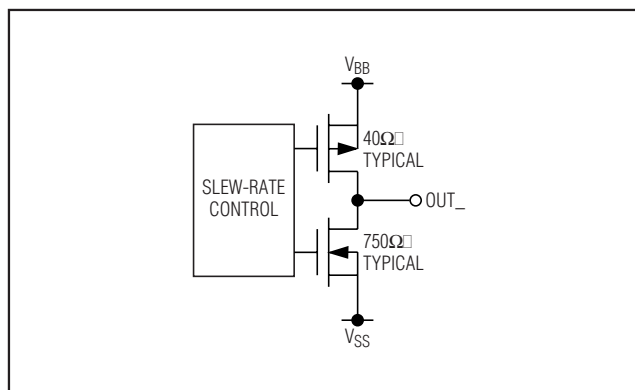


Figure 3. MAX6931 CMOS Output Driver Structure

Detailed Description

The MAX6921/MAX6931 are VFD tube drivers comprising a 4-wire serial interface driving 20 high-voltage rail-to-rail output ports. The driver is suitable for both static and multiplexed displays.

The output ports feature high current-sourcing capability to drive current into grids and anodes of static or multiplex VFDs. The ports also have active current sinking for fast discharge of capacitive display electrodes in multiplexing applications.

The 4-wire serial interface comprises a 20-bit shift register and a 20-bit transparent latch. The shift register is written through a clock input CLK and a data input DIN. For the MAX6921, the data propagates to a data output DOUT. The data output allows multiple drivers to be cascaded and operated together. The output latch is transparent to the shift register outputs when LOAD is high, and latches the current state on the falling edge of LOAD.

Each driver output is a slew-rated controlled CMOS push-pull switch driving between V_{BB} and GND (MAX6921) or V_{SS} (MAX6931). The output rise time is always slower than the output fall time to avoid shoot-through currents during output transitions. The output slew rates are slow enough to minimize EMI, yet are fast enough so as not to impact the typical 100 μ s digit multiplex period and affect the display intensity.

Initial Power-Up and Operation

An internal reset circuit clears the internal registers of the MAX6921/MAX6931 on power-up. All outputs OUT0 to OUT19 and the interface output DOUT (MAX6921 only) initialize low regardless of the initial logic levels of the CLK, DIN, BLANK, and LOAD inputs.

4-Wire Serial Interface

The MAX6921/MAX6931 use 4-wire serial interface with three inputs (DIN, CLK, LOAD) and a data output (DOUT, MAX6921 only). This interface is used to write output data to the MAX6921/MAX6931 (Figure 4) (Table 1). The serial interface data word length is 20 bits, D0–D19.

The functions of the four serial interface pins are:

- CLK input is the interface clock, which shifts data into the MAX6921/MAX6931s' 20-bit shift register on its rising edge.
- LOAD input passes data from the MAX6921/MAX6931s' 20-bit shift register to the 20-bit output latch when LOAD is high (transparent latch), and latches the data on LOAD's falling edge
- DIN is the interface data input, and must be stable when it is sampled on the rising edge of CLK.
- DOUT is the interface data output, which shifts data out from the MAX6921's 20-bit shift register on the rising edge of CLK. Data at DIN is propagated through the shift register and appears at DOUT (20 CLK cycles + t_{DO}) later.

A fifth input, BLANK, can be taken high to force outputs OUT0 to OUT19 low, without altering the contents of the output latches. When the BLANK input is low, outputs OUT0 to OUT19 follow the state of the output latches. A common use of the BLANK input is PWM intensity control.

The BLANK input's function is independent of the operation of the serial interface. Data can be shifted into the serial interface shift register and latched regardless of the state of BLANK.

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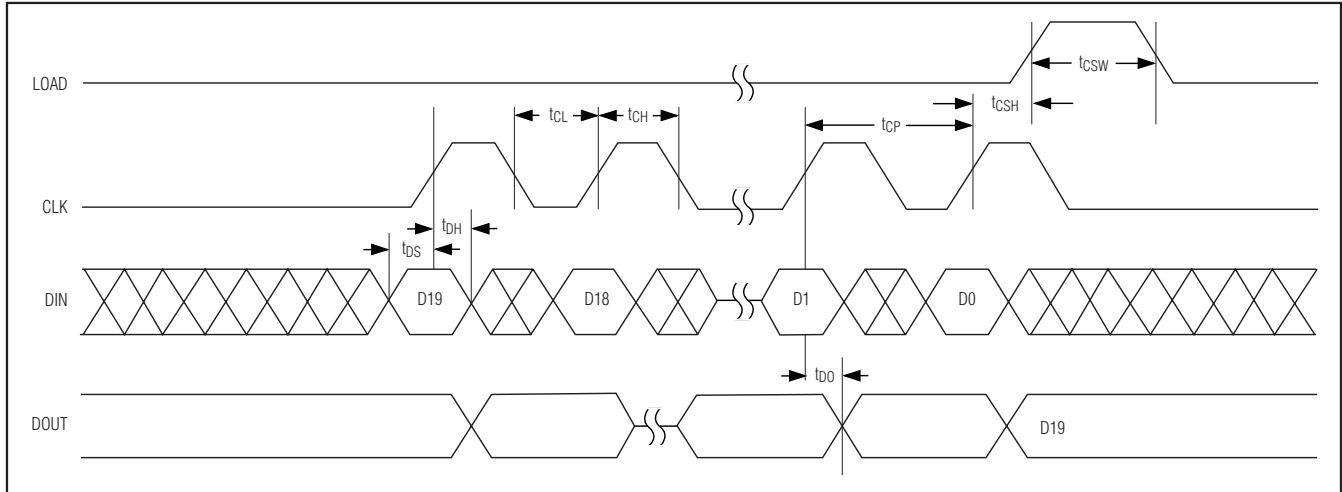


Figure 4. 4-Wire Serial Interface Timing Diagram

Table 1. 4-Wire Serial Interface Truth Table

SERIAL DATA INPUT DIN	CLOCK INPUT	SHIFT REGISTER CONTENTS						LOAD INPUT	LATCH CONTENTS						BLANKING INPUT	OUTPUT CONTENTS					
	CLK	D0	D1	D2	...	Dn-1	Dn	LOAD	D0	D1	D2	...	Dn-1	Dn	BLANK	D0	D1	D2	...	Dn-1	Dn
H		H	R0	R1	...	Rn-2	Rn-1														
L		L	R0	R1	...	Rn-2	Rn-1														
X		R0	R1	R2	...	Rn-1	Rn														
		X	X	X	...	X	X	L	R0	R1	R2	...	Rn-1	Rn							
		P0	P1	P2	...	Pn-1	Pn	H	P0	P1	P2	...	Pn-1	Pn	L	P0	P1	P2	...	Pn-1	Pn
									X	X	X	...	X	X	H	L	L	L	...	L	L

L = Low logic level.

H = High logic level.

X = Don't care.

P = Present state (shift register).

R = Previous state (latched).

Writing Device Registers Using the 4-Wire Serial Interface

The MAX6921/MAX6931 are normally written using the following sequence:

- 1) Take CLK low.
- 2) Clock 20 bits of data in order D19 first to D0 last into DIN, observing the data setup and hold times.
- 3) Load the 20 output latches with a falling edge on LOAD.

LOAD can be high or low during a transmission. If LOAD is high, then the data shifted into the shift register at DIN appear at the OUT0 to OUT19 outputs.

CLK and DIN can be used to transmit data to other peripherals. Activity on CLK always shifts data into the MAX6921/MAX6931s' shift register. However, the MAX6921/MAX6931 only update their output latch on the rising edge of LOAD, and the last 20 bits of data are loaded. Therefore, multiple devices can share CLK and DIN, as long as they have unique LOAD controls.

Determining Driver Output Voltage Drop

The outputs are CMOS drivers, and have a resistive characteristic. The typical and maximum sink and source output resistances can be calculated from the V_H and V_L electrical characteristics. Use this calculated resistance to determine the output voltage drop at different output currents.

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Output Current Ratings

The continuous current-source capability is 40mA per output. Outputs can drive up to 75mA as a repetitive peak current, subject to the on-time (output high) being no longer than 1ms, and the duty cycle being such that the output power dissipation is no more than the dissipation for the continuous case. The repetitive peak rating allows outputs to drive a higher current in multiplex grid driver applications, where only one grid is on at a time, and the multiplex time per grid is no more than 1ms.

Since dissipation is proportional to current squared, the maximum current that can be delivered for a given multiplex ratio is given by:

$$I_{PEAK} = (\text{grids} \times 1600)^{1/2} \text{ mA}$$

where grids is the number of grids in a multiplexed display.

This means that a duplex application (two grids) can use a repetitive peak current of 56.5mA, a triplex (three grids) application can use a repetitive peak current of 69.2mA, and higher multiplex ratios are limited to 75mA.

Paralleling Outputs

Any number of outputs within the same package can be paralleled in order to raise the current drive or reduce the output resistance. Only parallel outputs directly (by shorting outputs together) if the interface control can be guaranteed to set the outputs to the same level. Although the sink output is relatively weak (typically 750Ω), that resistance is low enough to dissipate 530mW when shorted to an opposite level output at a V_{BB} voltage of only 20V. A safe way to parallel outputs is to use diodes to prevent the outputs from sinking current (Figure 5). Because the outputs cannot sink current from the VFD tube, an external discharge resistor, R, is required. For static tubes, R can be a large value such as 100kΩ. For multiplexed tubes, the value

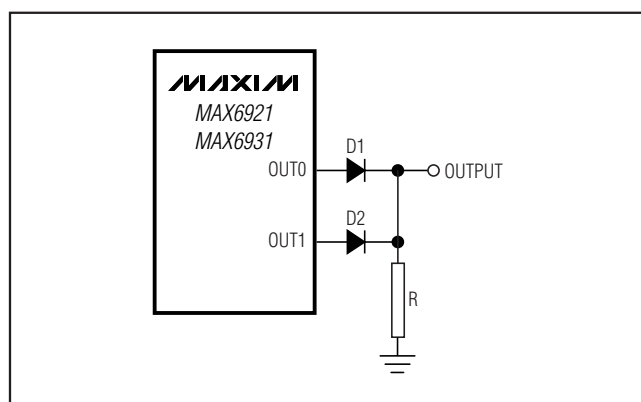


Figure 5. Paralleling Outputs

of the resistor can be determined by the load capacitance and timing characteristics required. Resistor R discharges tube capacitance C to 10% of the initial voltage in $2.3 \times RC$ seconds. So, for example, a 15kΩ value for R discharges 100pF tube grid or anode from 40V to 4V in 3.5μs, but draws an additional 2.7mA from the driver when either output is high.

Power Dissipation

Take care to ensure that the maximum package dissipation ratings for the chosen package are not exceeded. Over-dissipation is unlikely to be an issue when driving static tubes, but the peak currents are usually higher for multiplexed tubes. When using multiple driver devices, try to share the average dissipation evenly between the drivers.

Determine the power dissipation (P_D) for the MAX6921/MAX6931 for static tube drivers with the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (V_{BB} \times I_{BB}) + ((V_{BB} - V_H) \times I_{ANODE} \times A)$$

where:

A = number of anodes driven (the MAX6921/MAX6931 can drive a maximum of 20).

I_{ANODE} = maximum anode current.

(V_{BB} - V_H) is the output voltage drop at the given maximum anode current I_{OUT}.

A static tube dissipation example follows:

$$V_{CC} = 5V \pm 5\%, V_{BB} = 10V \text{ to } 18V, A = 20, I_{OUT} = 2mA$$

$$P_D = (5.25V \times 1mA) + (18V \times 1.4mA) + ((2.5V \times 2mA/25mA) \times 2mA \times 20) = 38mW$$

Determine the power dissipation (P_D) for the MAX6921/MAX6931 for multiplex tube drivers with the following equation:

$$P_D = (V_{CC} \times I_{CC}) + (V_{BB} \times I_{BB}) + ((V_{BB} - V_H) \times I_{ANODE} \times A) + ((V_{BB} - V_H) \times I_{GRID})$$

where:

A = number of anodes driven.

G = number of grids driven.

I_{ANODE} = maximum anode current.

I_{GRID} = maximum grid current.

The calculation presumes all anodes are on, but only one grid is on. The calculated P_D is the worst case, presuming one digit is always being driven with all its anodes lit. Actual P_D can be estimated by multiplying this P_D figure by the actual tube drive duty cycle, taking into account interdigit blanking and any PWM intensity control.

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A multiplexed tube dissipation example follows:

$$V_{CC} = 5V \pm 5\%, V_{BB} = 36V \text{ to } 42V, A = 12, G = 8, \\ I_{ANODE} = 0.4mA, I_{GRID} = 24mA$$

$$P_D = (5.25V \times 1mA) + (42V \times 1.4mA) \\ + ((2.5V \times 0.4mA/25mA) \times 0.4mA \times 12) \\ + ((2.5V \times 24mA/25mA) \times 24mA) = 122mW$$

Thus, for a 28-pin wide TSSOP package ($T_{JA} = 1 / 0.0128 = 78.125^\circ C/W$ from *Absolute Maximum Ratings*), the maximum allowed ambient temperature T_A is given by:

$$T_{J(MAX)} = T_A + (P_D \times T_{JA}) = 150^\circ C = T_A + (0.122 \times 78.125^\circ C/W)$$

So $T_A = +140.5^\circ C$.

This means that the driver can be operated in this application up to the MAX6921/MAX6931s' $+125^\circ C$ maximum operating temperature.

Power-Supply Considerations

The MAX6921/MAX6931 operate with multiple power-supply voltages. Bypass the V_{CC} , V_{BB} , and V_{SS} (MAX6931 only) power-supply pins to GND with $0.1\mu F$ capacitors close to the device. The MAX6931 can be operated with V_{SS} connected to GND if a negative bias supply is not required. For multiplex applications, it may be necessary to add an additional bulk electrolytic capacitor of $1\mu F$ or greater to the V_{BB} supply.

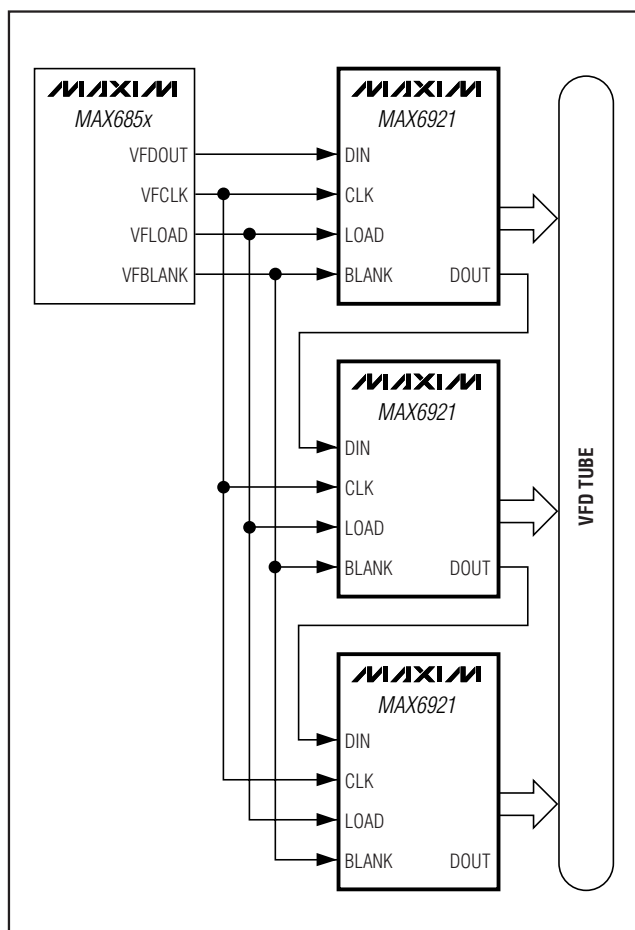
Power-Supply Sequencing

The order of the power-supply sequencing is not important. The MAX6921/MAX6931 will not be damaged if any combination of V_{CC} , V_{BB} , and V_{SS} (MAX6931 only) is grounded while the other supply or supplies are maintained up to their maximum ratings. However, as with any CMOS device, do not drive the MAX6921/MAX6931s' logic inputs if the logic supply V_{CC} is not operational because the input protection diodes clamp the signals.

Cascading Drivers (MAX6921 Only)

Multiple MAX6921s can be cascaded, as shown in the *Typical Application Circuit*, by connecting each driver's DOUT to DIN of the next drivers. Devices can be cascaded at the full 5MHz CLK speed when $V_{CC} \geq 4.5V$. When $V_{CC} < 4.5V$, the longer propagation delay (t_{DO}) limits the maximum cascaded CLK to 4MHz.

Typical Application Circuit

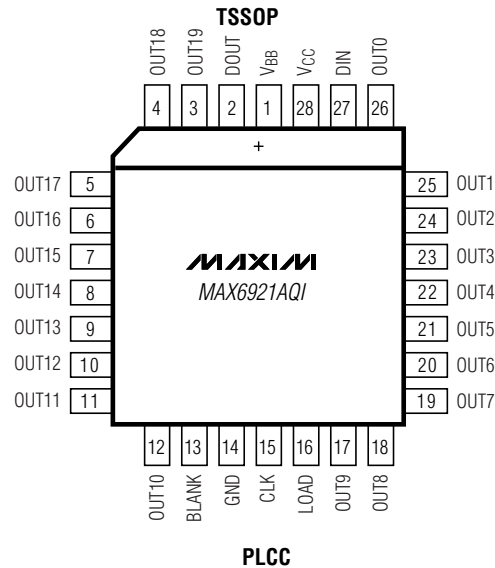
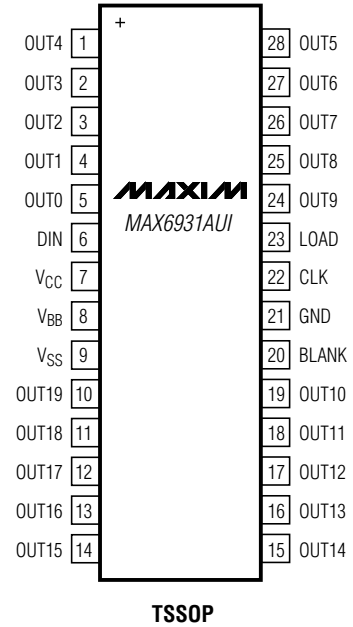
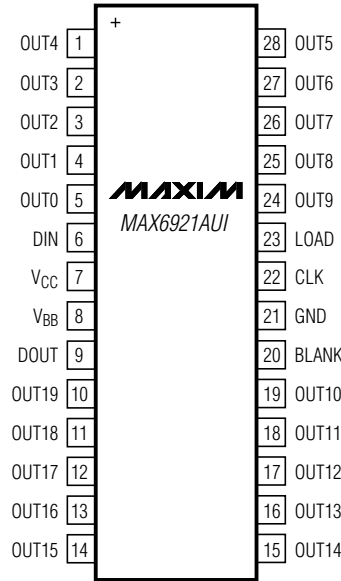
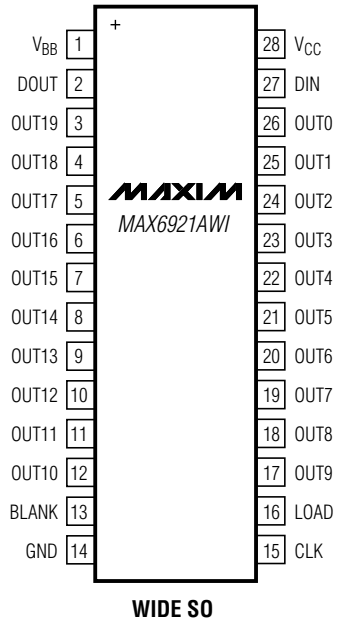


20-Output, 76V, Serial-Interfaced VFD Tube Drivers

Pin Configurations

MAX6921/MAX6931

TOP VIEW



20-Output, 76V, Serial-Interfaced VFD Tube Drivers

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TSSOP	U28+1	21-0066
28 Wide SO	W28+1	21-0042
28 PLCC	Q28+1	21-0049

20-Output, 76V, Serial-Interfaced VFD Tube Drivers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/03	Initial release	—
1	4/10	Added automotive and lead-free parts to <i>Ordering Information</i>	1

MAX6921/MAX6931

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