-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

ABSOLUTE MAXIMUM RATINGS

All Voltages Are Referenced to V_{EE}, Unless Otherwise Noted
Supply Voltage (V_{DD} - V_{EE}).....-0.3V to +100V
DRAIN, PWRGD, $\overline{PWRGD}$ .....-0.3V to +100V
PWRGD to DRAIN ..... -0.3V to +95V
PWRGD to V_{DD}.....-95V to +85V
SENSE (Internally Clamped) .....-0.3V to +1.0V
GATE (Internally Clamped) .....-0.3V to +18V
UV and OV.....-0.3V to +60V
Current into SENSE.....+40mA
Current into GATE.....+300mA
Current into Any Other Pin.....+20mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C).....471mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = 0V, V_{DD} = 48V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Operating Input Voltage Range	V_{DD}		20		80	V
Supply Current	I_{DD}	Current into V_{DD} with UV = 3V, OV, DRAIN, SENSE = V_{EE}, GATE = floating		0.7	2	mA
GATE DRIVER AND CLAMPING CIRCUITS						
Gate Pullup Current	I_{PU}	GATE drive on, V_{GATE} = V_{EE}	-30	-45	-60	µA
Gate Pulldown Current	I_{PD}	V_{SENSE} - V_{EE} = 100mV, V_{GATE} = 2V (Note 2)	24	50	70	mA
External Gate Drive	ΔV_{GATE}	V_{GATE} - V_{EE}, steady state, 20V ≤ V_{DD} ≤ 80V	10	13.5	18	V
GATE to V_{EE} Clamp Voltage	V_{GSCLMP}	V_{GATE} - V_{EE}, I_{GS} = 30mA	15	16.4	18	V
CIRCUIT BREAKER						
Current-Limit Trip Voltage	V_{CL}	V_{CL} = V_{SENSE} - V_{EE}	40	50	60	mV
SENSE Input Current	I_{SENSE}	V_{SENSE} = 50mV	-1	-0.2	0	µA
UNDERVOLTAGE LOCKOUT						
Supply Internal Undervoltage Lockout Voltage High	V_{UVLOH}	V_{DD} increasing	13.8	15.4	17.0	V
Supply Internal Undervoltage Lockout Voltage Low	V_{UVLOL}	V_{DD} decreasing	11.8	13.4	15.0	V
UV INPUT						
UV High Threshold	V_{UVH}	UV voltage increasing	1.240	1.255	1.270	V
UV Low Threshold	V_{UVL}	UV voltage decreasing	1.105	1.125	1.145	V
UV Hysteresis	V_{UVHY}			130		mV
UV Input Current	I_{INUV}	UV = V_{EE}	-0.5		0	µA
OV INPUT						
OV High Threshold	V_{OVH}	OV voltage rising	1.235	1.255	1.275	V
OV Low Threshold	V_{OVL}	OV voltage decreasing	1.189	1.205	1.221	V
OV Voltage Reference Hysteresis	V_{OVHY}			50		mV
OV Input Current	I_{INOV}	OV = V_{EE}	-0.5		0	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = 0V, V_{DD} = 48V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C, unless otherwise noted.) (Notes 1, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWRGD OUTPUT SIGNAL (REFERENCED TO DRAIN)							
DRAIN Input Current	I_{DRAIN}	V_{DRAIN} = 48V		10	80	250	µA
DRAIN Threshold for PWRGD	V_{DL}	V_{DRAIN} - V_{EE} threshold for power-good condition, DRAIN decreasing		1.1	1.7	2.0	V
GATE High Threshold	V_{GH}	ΔV_{GATE} - V_{GATE}, decreasing		1.0	1.6	2.0	V
PWRGD, $\overline{PWRGD}$ Output Leakage	I_{OH}	$V_{\overline{PWRGD}}$ = 80V, V_{DRAIN} = 48V				10	µA
		V_{PWRGD} = 80V, V_{DRAIN} = 0V				10	
$\overline{PWRGD}$ Low Voltage ($V_{\overline{PWRGD}}$ - V_{EE})	V_{OL}	V_{DRAIN} - V_{EE} < V_{DL}, I_{SINK} = 5mA (A, E versions)			0.11	0.4	V
PWRGD Low Voltage (V_{PWRGD} - V_{DRAIN})	V_{OL}	V_{DRAIN} = 5V, I_{SINK} = 5mA (B, F versions)			0.11	0.4	V
OVERTEMPERATURE PROTECTION							
Overtemperature Threshold	$T_{OT(TH)}$	Junction temperature, temperature rising			135		°C
Overtemperature Hysteresis	T_{HYS}	See *Thermal Shutdown* section			20		°C
AC PARAMETERS							
OV High to GATE Low	t_{PHLOV}	Figures 1a, 2			0.5		µs
UV Low to GATE Low	t_{PHLUV}	Figures 1a, 3			0.4		µs
OV Low to GATE High	t_{PLHOV}	Figures 1a, 2			3.3		µs
UV High to GATE High	t_{PLHUV}	Figures 1a, 3			8.4		ms
SENSE High to GATE Low	$t_{PHLSENSE}$	Figures 1a, 4a			1		µs
Current Limit to GATE Low	t_{PHLCL}	Time from continuous current limit to GATE shutdown (see *Overcurrent Fault Integrator* section), Figures 1b, 4b	A, B versions	0.35	0.5	0.65	ms
			E, F versions	1.4	2.0	2.6	
DRAIN Low to $\overline{PWRGD}$ Low DRAIN Low to (PWRGD - DRAIN) High	t_{PHLDL}	Figures 1a, 5a; A and E versions			8.2		ms
		Figures 1a, 5a; B and F versions			8.2		
GATE High to $\overline{PWRGD}$ Low GATE High to (PWRGD - DRAIN) High	t_{PHLGH}	Figures 1a, 5b; A and E versions			8.2		ms
		Figures 1a, 5b; B and F versions			8.2		
TURN-OFF							
Latch-Off Period	t_{OFF}	(Note 3)	A, B, E, F versions		128 x t_{PHLCL}		ms

Note 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{EE}, unless otherwise specified.

Note 2: Gate pulldown current after the current limit to GATE low (t_{PHLCL}) time has elapsed.

Note 3: Minimum duration of GATE pulldown following a circuit breaker fault. The MAX5921_ automatically restarts after a circuit breaker fault. The MAX5939_ is latched off and can be reset by toggling UV low. The GATE pulldown does not release until t_{OFF} has elapsed.

Note 4: The min/max limits are 100% production tested at +25°C and +85°C and guaranteed by design at -40°C.

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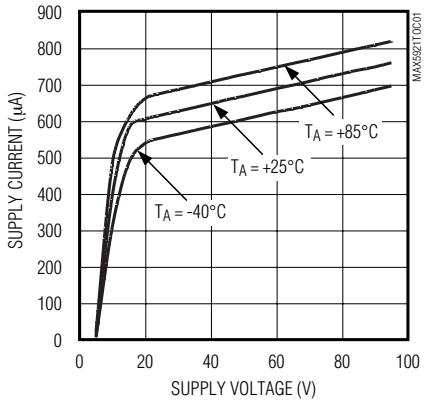
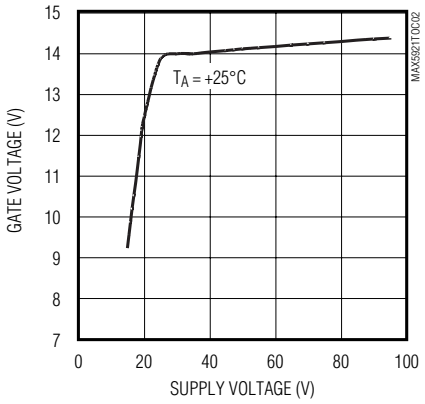
Typical Operating Characteristics

(V_{DD} = +48V, V_{EE} = 0V, T_A = +25°C, unless otherwise noted.)

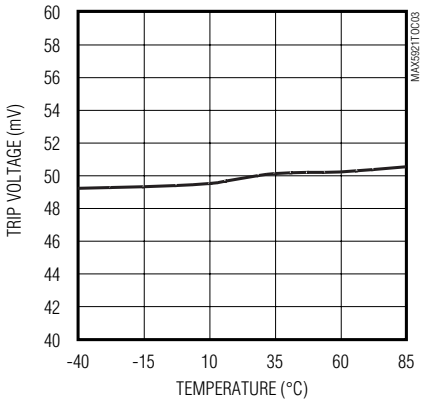
SUPPLY CURRENT vs. SUPPLY VOLTAGE



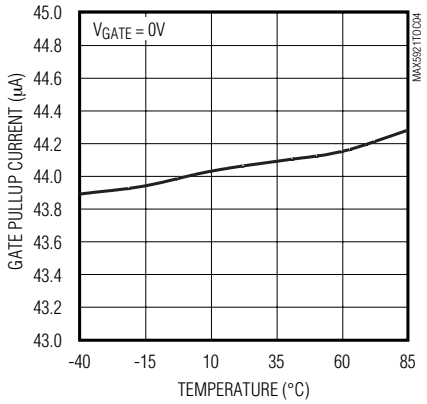
GATE VOLTAGE vs. SUPPLY VOLTAGE



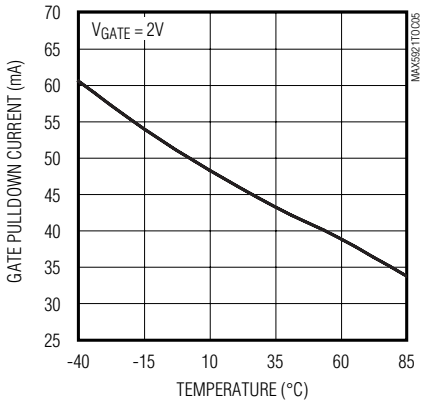
CURRENT-LIMIT TRIP VOLTAGE vs. TEMPERATURE



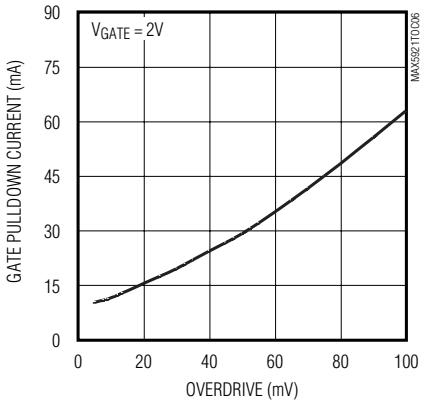
GATE PULLUP CURRENT vs. TEMPERATURE



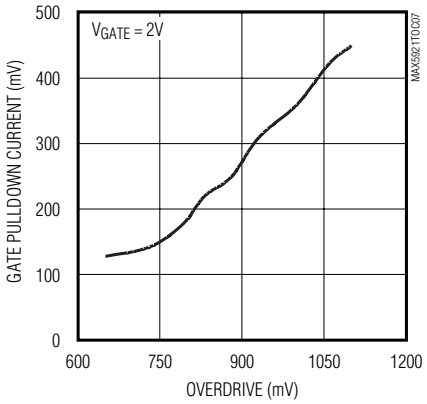
GATE PULLDOWN CURRENT vs. TEMPERATURE AFTER A FAULT



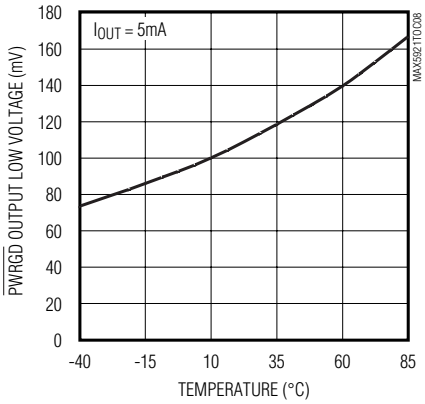
GATE PULLDOWN CURRENT vs. OVERDRIVE DURING A CURRENT FAULT



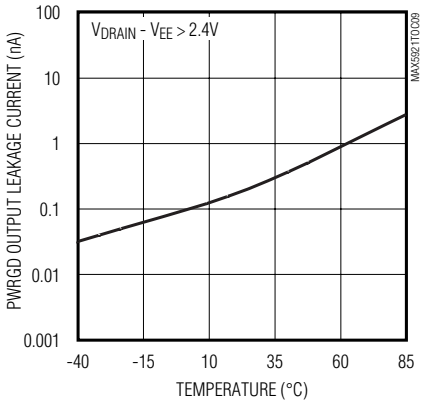
GATE PULLDOWN CURRENT vs. OVERDRIVE DURING A SHORT CIRCUIT



$\overline{PWRGD}$ OUTPUT LOW VOLTAGE vs. TEMPERATURE (MAX5921A)



PWRGD OUTPUT LEAKAGE CURRENT vs. TEMPERATURE (MAX5921B)



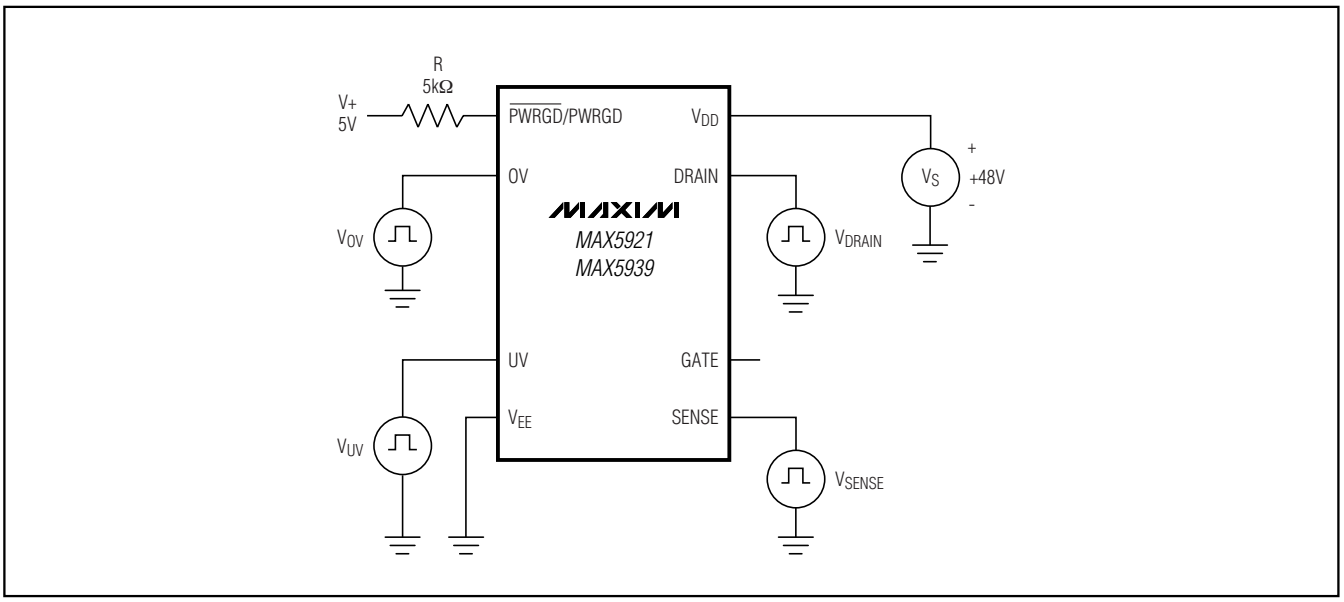


Figure 1a. Test Circuit 1

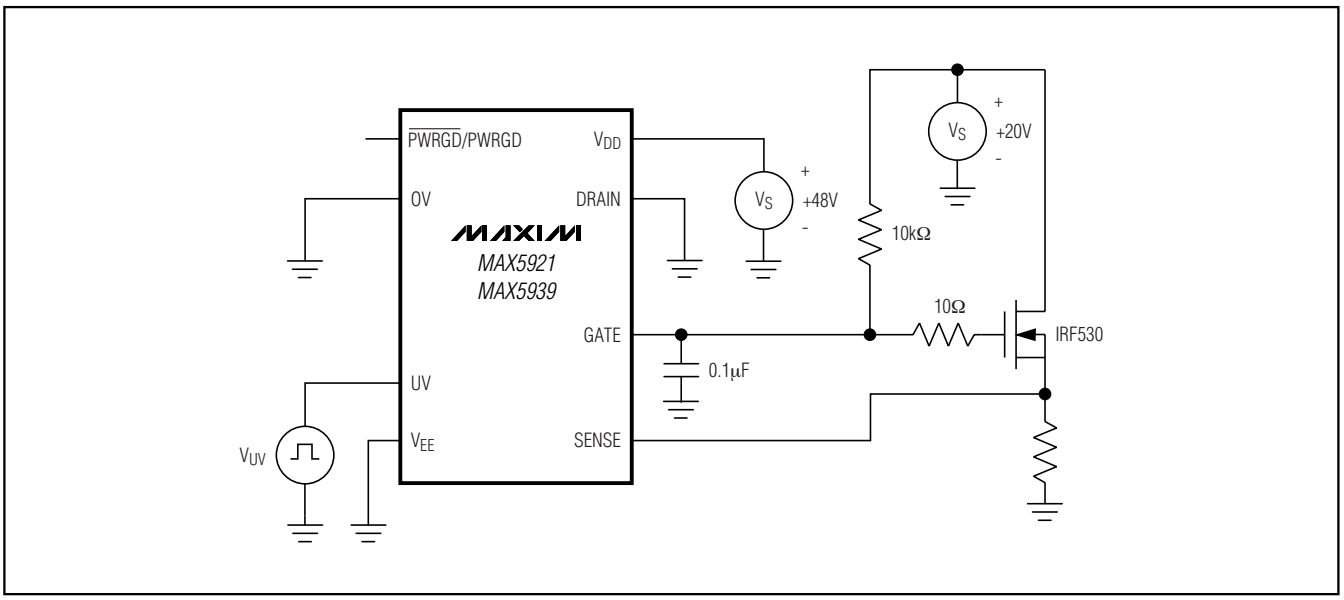


Figure 1b. Test Circuit 2

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

Timing Diagrams

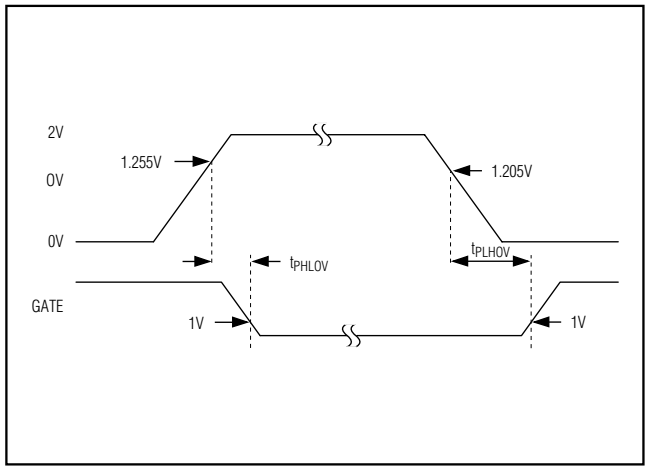


Figure 2. OV to GATE Timing

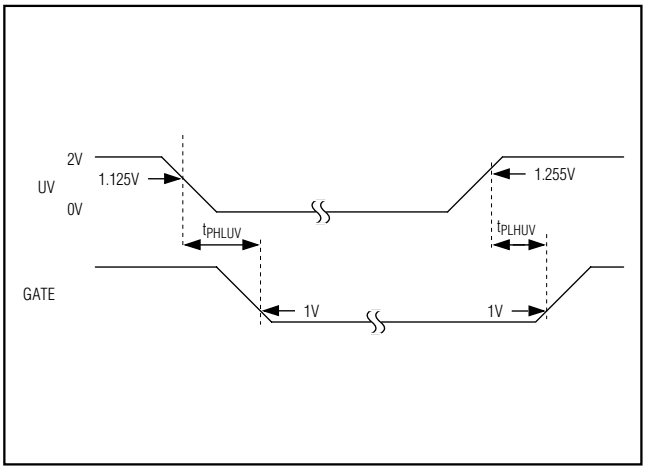


Figure 3. UV to GATE Timing

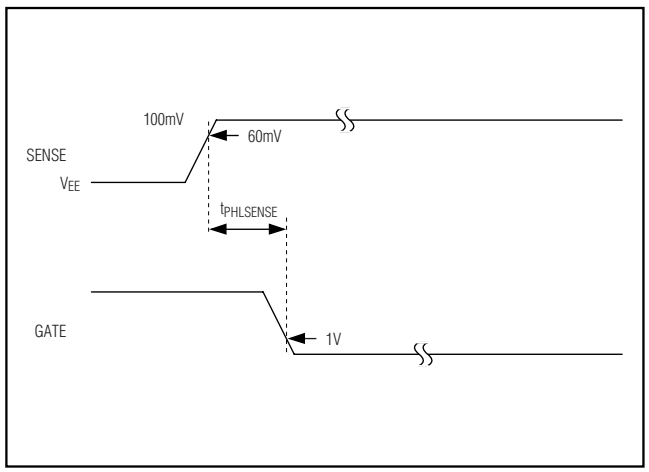


Figure 4a. SENSE to GATE Timing

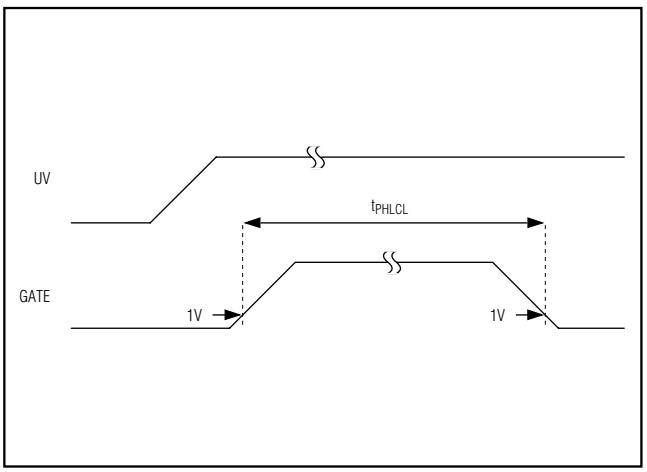


Figure 4b. Active Current-Limit Threshold

Timing Diagrams (continued)

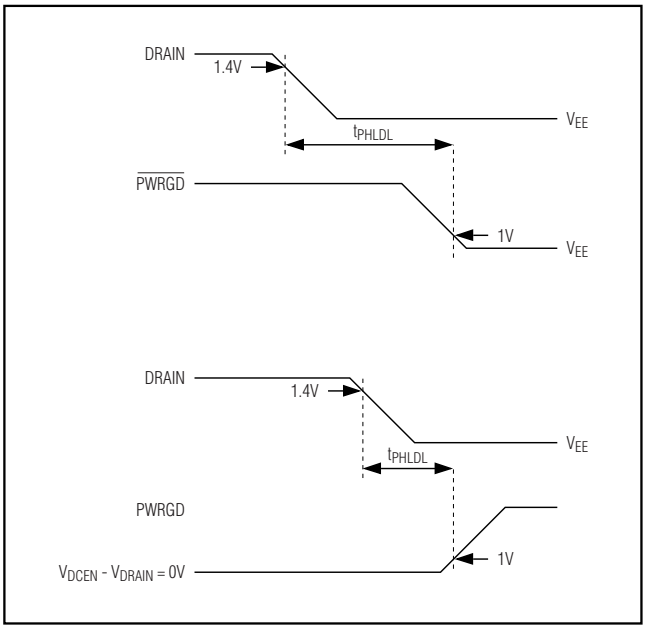


Figure 5a. DRAIN to $\overline{PWRGD}$/PWRGD Timing

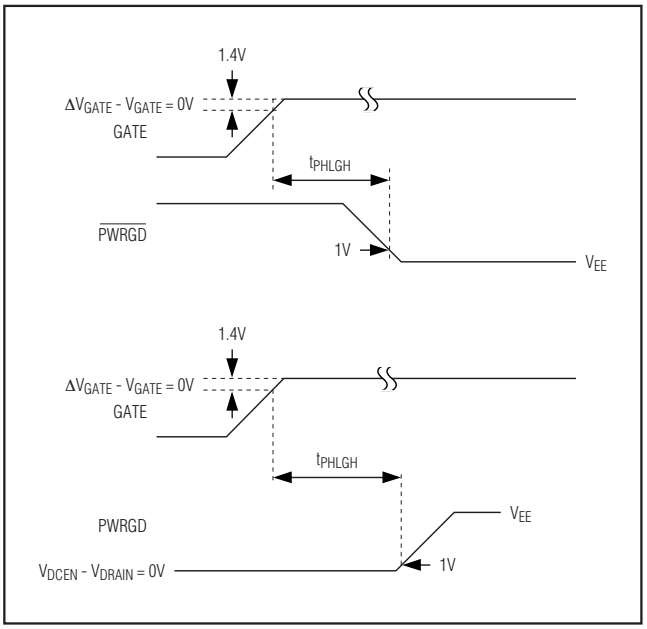
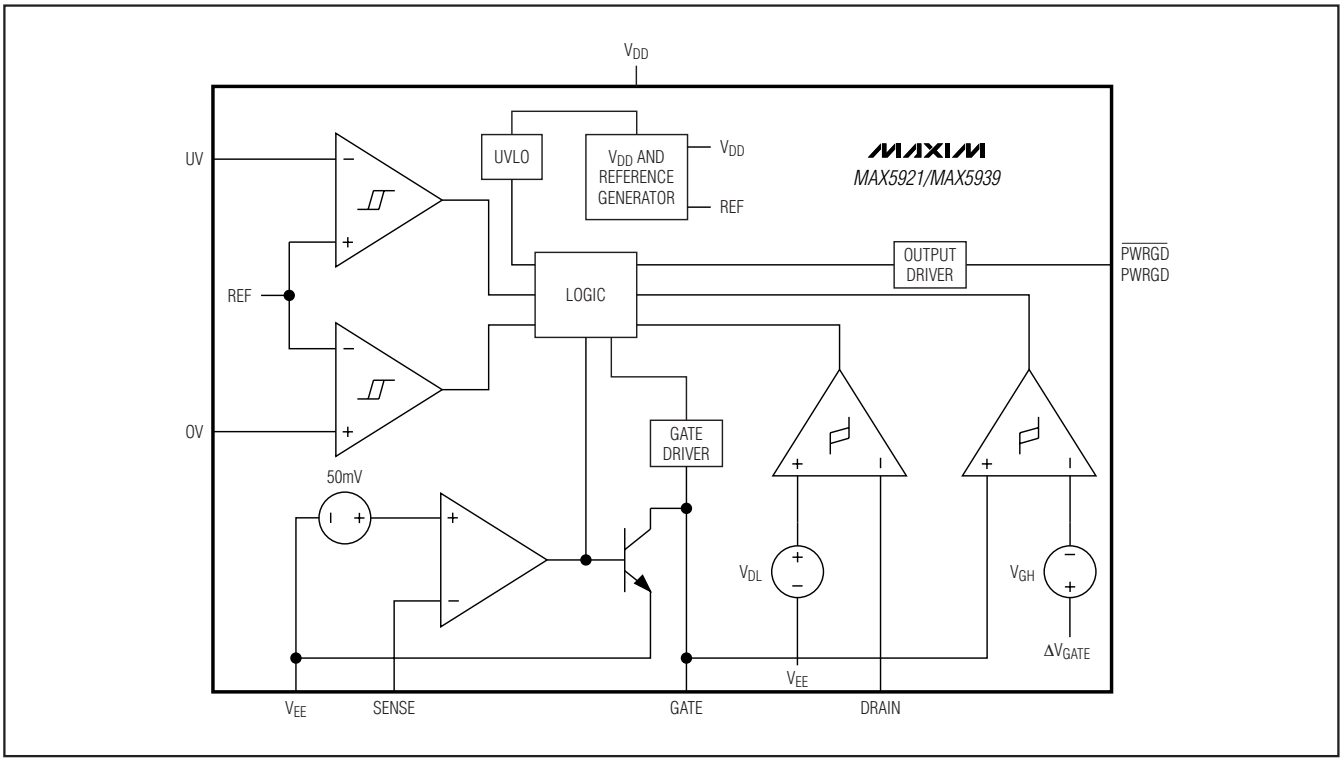


Figure 5b. GATE to $\overline{PWRGD}$/PWRGD Timing

Block Diagram



-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

Pin Description

PIN		NAME	FUNCTION
MAX5921A/ MAX5921E MAX5939A/ MAX5939E	MAX5921B/ MAX5921F MAX5939B/ MAX5939F		
1	—	$\overline{PWRGD}$	Power-Good Signal Output. $\overline{PWRGD}$ is an active-low open-drain status output referenced to V_{EE}. $\overline{PWRGD}$ latches low when $V_{DRAIN} - V_{EE} \le V_{DL}$ and $V_{GATE} > \Delta V_{GATE}$ indicating a power-good condition. $\overline{PWRGD}$ is open drain otherwise.
—	1	PWRGD	Power-Good Signal Output. PWRGD is an active-high open-drain status output referenced to DRAIN. PWRGD latches in a high-impedance state when $V_{DRAIN} - V_{EE} \le V_{DL}$ and $V_{GATE} > \Delta V_{GATE} - V_{GH}$ indicating a power-good condition. PWRGD is pulled low to DRAIN otherwise.
2	2	OV	Overvoltage Detection Input. OV is referenced to V_{EE}. When OV is pulled above V_{OVH} voltage, GATE pulls low. GATE remains low until the OV voltage reduces to $V_{OVH} - V_{OVHY}$.
3	3	UV	Undervoltage Detection Input. UV is referenced to V_{EE}. When UV is pulled above V_{UVH} voltage, the GATE is enabled. When UV is pulled below V_{UVL}, GATE pulls low. UV is also used to reset the circuit breaker after a fault condition. To reset the circuit breaker, pull UV below V_{UVL}. The reset command can be issued immediately after a fault condition; however, the device will not restart until a t_{OFF} delay time has elapsed after the fault condition is removed.
4	4	V_{EE}	Negative Power-Supply Input. Connect to the negative power-supply rail.
5	5	SENSE	Current-Sense Input. Connect to the external sense resistor and the source of the external MOSFET. The voltage drop across the external sense resistor is monitored to detect overcurrent or short-circuit fault conditions. Connect SENSE to V_{EE} to disable the current-limiting feature.
6	6	GATE	Gate Drive Output. Connect to the gate of the external N-channel MOSFET.
7	7	DRAIN	Output Voltage Sense Input. Connect to the output voltage node (drain of external N-channel MOSFET). Place the MAX5921/MAX5939 such that DRAIN is close to the drain of the external MOSFET for the best thermal protection.
8	8	V_{DD}	Positive Power-Supply Input. This is the power ground in the negative supply voltage system. Connect to the higher potential of the power-supply inputs.

Detailed Description

The MAX5921/MAX5939 integrated hot-swap controllers for -48V power systems allow circuit boards to be safely hot plugged into a live backplane without causing a glitch on the power-supply rail. When circuit boards are inserted into a live backplane, the bypass capacitors at the input of the board's power module or switching power supply can draw large inrush currents as they charge. Uncontrolled inrush currents can cause glitches on the system power supply and damage components on the board.

The MAX5921/MAX5939 provide a controlled turn-on to circuit cards preventing damage to connectors, board components, and prevent glitches on the power-supply rail. Both the MAX5921/MAX5939 provide undervoltage, overvoltage, and overcurrent protection. The MAX5921/MAX5939 ensure that the input voltage is stable and within tolerance before applying power to the load. The device also provides protection against input voltage steps by limiting the load current to a safe level without turning off power to the load.

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

Board Insertion

Figure 6a shows a typical hot-swap circuit for -48V systems. When the circuit board first makes contact with the backplane, the DRAIN to GATE capacitance (C_{gd}) of Q1 pulls up the GATE voltage to roughly $IV_{EE} \times (C_{gd}/C_{gd} + C_{gs})I$. The MAX5921/MAX5939 feature an internal dynamic clamp between GATE and V_{EE} to keep the gate-to-source voltage of Q1 low during hot insertion preventing Q1 from passing an uncontrolled current to the load. For most applications, the internal clamp between GATE and V_{EE} of the MAX5921/MAX5939 eliminates the need for an external gate-to-source capacitor. The resistor R3 limits the current into the clamp circuitry during card insertion.

Power-Supply Ramping

The MAX5921/MAX5939 can reside either on the backplane or the removable circuit board (Figure 6a). Power is delivered to the load by placing an external N-channel MOSFET pass transistor in the power-supply path.

After the circuit board is inserted into the backplane, and the supply voltage at V_{EE} is stable and within the undervoltage and overvoltage tolerance, the MAX5921/MAX5939 gradually turn on the external MOSFET by charging the gate of Q1 with a 45µA current source. Capacitor C2 provides a feedback signal to accurately limit the inrush current.

The inrush current can be calculated:

$$I_{INRUSH} = I_{PU} \times C_L / C2$$

where C_L is the total load capacitance, C3 + C4, and I_{PU} is the gate pullup current.

Figure 6b shows the inrush current waveform. The current through C2 controls the GATE voltage. At the end of the DRAIN ramp, the GATE voltage is charged to its final value. The GATE-to-SENSE clamp limits the maximum ΔV_{GATE} to 18V.

Board Removal

If the circuit card is removed from the backplane, the voltage at the UV falls below the UVLO detect threshold, and the MAX5921/MAX5939 turn off the external MOSFET.

Current Limit and Electronic Circuit Breaker

The MAX5921/MAX5939 provide current-limiting and circuit-breaker features that protect against excessive load current and short-circuit conditions. The load current is monitored by sensing the voltage across an external sense resistor connected between V_{EE} and SENSE.

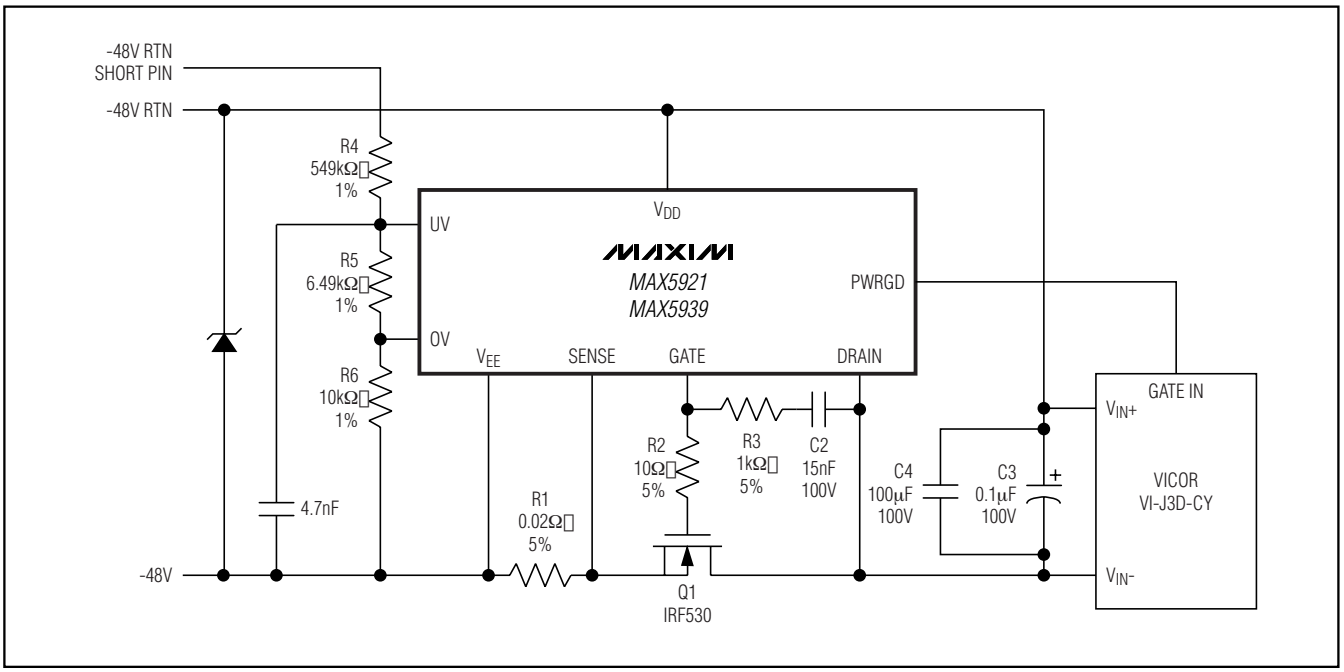


Figure 6a. Inrush Control Circuitry/Typical Application Circuit

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

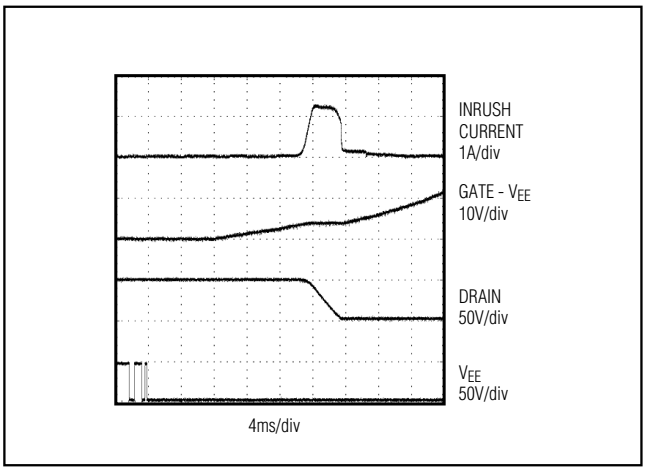


Figure 6b. Inrush Control Waveforms

If the voltage between V_{EE} and SENSE reaches the current-limit trip voltage (V_{CL}), the MAX5921/MAX5939 pull down the GATE and regulate the current through the external MOSFET such that $V_{SENSE} - V_{EE} \leq V_{CL}$. If the current drawn by the load drops below V_{CL} / R_{SENSE} limit, the GATE voltage rises again. However, if the load current is at the regulation limit of V_{CL} / R_{SENSE} for a period of t_{PHLCL}, the electronic circuit breaker trips, causing the MAX5921/MAX5939 to turn off the external MOSFET.

After an overcurrent fault condition, the MAX5921 automatically restarts after t_{OFF} has elapsed. The MAX5939 circuit breaker is reset by toggling UV or by cycling power. Unless power is cycled to the MAX5939, the device waits until t_{OFF} has elapsed before turning on the gate of the external FET.

Load-Current Regulation

The MAX5921/MAX5939 accomplish load-current regulation by pulling current from GATE whenever $V_{SENSE} - V_{EE} > V_{CL}$. This decreases the gate-to-source voltage of the external MOSFET, thereby reducing the load current. When $V_{SENSE} - V_{EE} < V_{CL}$, the MAX5921/MAX5939 pulls GATE high by a 45µA (I_{PU}) current.

Exponential Current Regulation

The MAX5921/MAX5939 provide an exponential pulldown current to turn off the external FET in response to overcurrent conditions. The GATE pulldown current increases (see *Typical Operating Characteristics*) in response to $V_{SENSE} - V_{EE}$ potentials greater than 50mV (V_{CL}).

Load Current Regulation (Short-Circuit Condition)

The MAX5921/MAX5939 devices also include a very fast high-current pulldown source connected to GATE (see *Typical Operating Characteristics*). The high-current pulldown activates if V_{SENSE} exceeds V_{EE} by 650mV (typ) during a catastrophic overcurrent or short-circuit fault condition. The high-current pulldown circuit sinks as much as 450mA from GATE to turn off the external MOSFET.

Immunity to Input Voltage Steps

The MAX5921/MAX5939 guard against input voltage steps on the input supply. A rapid increase in the input supply voltage ($V_{DD} - V_{EE}$ increasing) causes a current step equal to $I = C_L \times \Delta V_{IN} / \Delta t$, proportional to the input voltage slew rate ($\Delta V_{IN} / \Delta t$). If the load current exceeds V_{CL} / R_{SENSE} during an input voltage step, the MAX5921/MAX5939 current limit activates, pulling down the gate voltage and limiting the load current to V_{CL} / R_{SENSE}. The DRAIN voltage (V_{DRAIN}) then slews at a slower rate than the input voltage. As the drain voltage starts to slew down, the drain-to-gate feedback capacitor C2 pushes back on the gate, reducing the gate-to-source voltage (V_{GS}) and the current through the external MOSFET. Once the input supply reaches its final value, the DRAIN slew rate (and therefore the inrush current) is limited by the capacitor C2 just as it is limited in the startup condition (see the *Power-Supply Ramping* section). To ensure correct operation, R_{SENSE} must be chosen to provide a current limit larger than the sum of the load current and the dynamic current into the load capacitance in the slewing mode.

If the load current plus the capacitive charging current is below the current limit, the circuit breaker does not trip.

Undervoltage and Overvoltage Protection

Use UV and OV to detect undervoltage and overvoltage conditions. UV and OV internally connect to analog comparators with 130mV (UV) and 50mV (OV) of hysteresis. When the UV voltage falls below its threshold or the OV voltage rises above its threshold, GATE pulls low. GATE is held low until UV goes high and OV is low, indicating that the input supply voltage is within specification. The MAX5921/MAX5939 includes an internal lockout (UVLO) that keeps the external MOSFET off until the input supply voltage exceeds 15.4V, regardless of the UV input.

UV is also used to reset the circuit breaker after a fault condition has occurred. Pull UV below V_{UVL} to reset the circuit breaker.

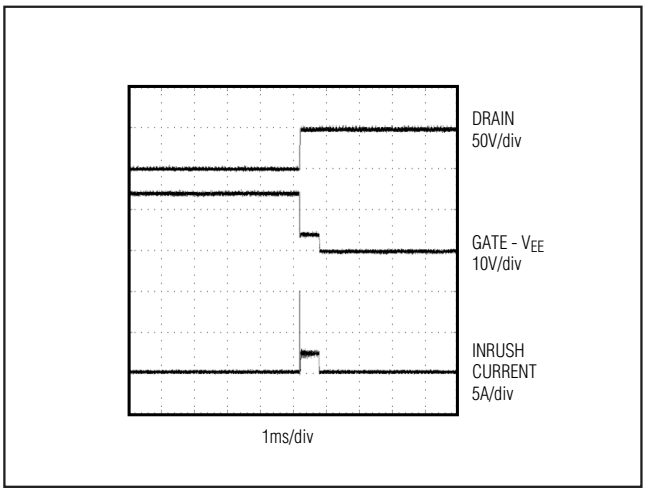


Figure 7. Short-Circuit Protection Waveform

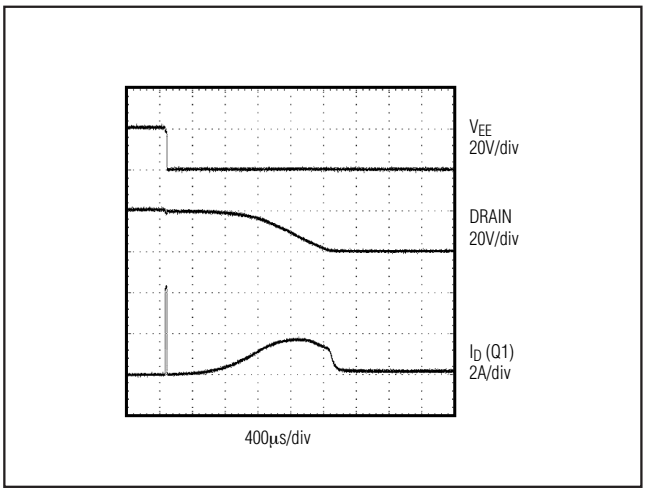


Figure 8. Voltage Step-On Input Supply

Figure 10 shows how to program the undervoltage and overvoltage trip thresholds using three resistors. With R4 = 549kΩ, R5 = 6.49kΩ, and R6 = 10kΩ, the undervoltage threshold is set to 38.5V (with a 43V release from undervoltage), and the overvoltage is set to 71V. The resistor-divider also increases the hysteresis and overvoltage lockout to 4.5V and 2.8V at the input supply, respectively.

$\overline{\text{PWRGD}}$/PWRGD Output

Use the $\overline{\text{PWRGD}}$ (PWRGD) output to enable a power module after hot insertion. Use the MAX59__A ($\overline{\text{PWRGD}}$) to enable modules with an active-low enable input (Figure 12), or use the MAX59__B (PWRGD) to enable modules with an active-high enable input (Figure 11).

The PWRGD signal is referenced to the DRAIN terminal, which is the negative supply of the power module. The $\overline{\text{PWRGD}}$ signal is referenced to V_{EE}.

When the DRAIN voltage of the MAX5921A (see *Selector Guide* for complete selection) or MAX5939A is high with respect to V_{EE} or the GATE voltage is low from an undervoltage condition, then the internal pulldown MOSFET Q2 is off. The $\overline{\text{PWRGD}}$ output goes into a high-impedance state (Figure 13). $\overline{\text{PWRGD}}$ is pulled high by the module's internal pullup current source, turning the module off. When the DRAIN voltage drops below V_{DL} and the GATE voltage is greater than ΔV_{GATE} - V_{GH}, Q2 turns on and $\overline{\text{PWRGD}}$ pulls low, enabling the module.

The $\overline{\text{PWRGD}}$ signal can also be used to turn on an LED or optoisolator to indicate that the power is good (Figure 13) (see the *Component Selection Procedure* section).

When the DRAIN voltage drops below V_{DL} and the GATE voltage is greater than ΔV_{GATE} - V_{GH}, MOSFET Q3 turns on, shorting I_1 to V_{EE} and turning Q2 off. The pullup current in the module pulls the PWRGD high, enabling the module.

When the DRAIN voltage of the MAX5921B/MAX5939B (see *Selector Guide* for complete selection) is high with respect to V_{EE} (Figure 12) or the GATE voltage is low due to an undervoltage condition, the internal MOSFET Q3 is turned off so that I_1 and the internal MOSFET Q2 clamp PWRGD to the DRAIN turning off the module.

Once the PWRGD and $\overline{\text{PWRGD}}$ outputs are active, the MAX5921/MAX5939 output does not toggle due to an overvoltage (OV) fault.

GATE Voltage Regulation

GATE goes high when the following startup conditions are met: UV is high, OV is low, the supply voltage is above V_{UVLOH}, and (V_{SENSE} - V_{EE}) is less than 50mV. The gate is pulled up with a 45µA current source and is regulated at 13.5V above V_{EE}. The MAX5921/MAX5939 include an internal clamp that ensures the GATE voltage of the external MOSFET never exceeds 18V. During a fast-rising V_{DD}, an additional dynamic clamp keeps the GATE and SENSE potentials as close as possible to prevent the FET from accidentally turning on. When a fault condition is detected, GATE is pulled low (see the *Load Current Regulation* section).

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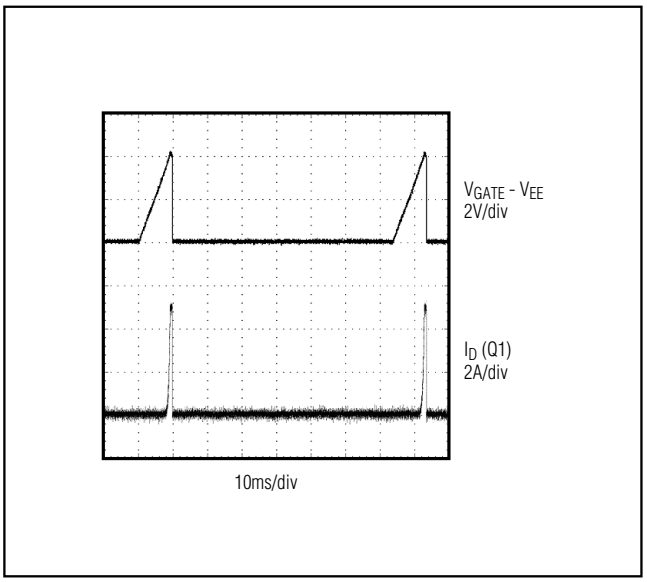

Figure 9. Automatic Restart After a Short Circuit

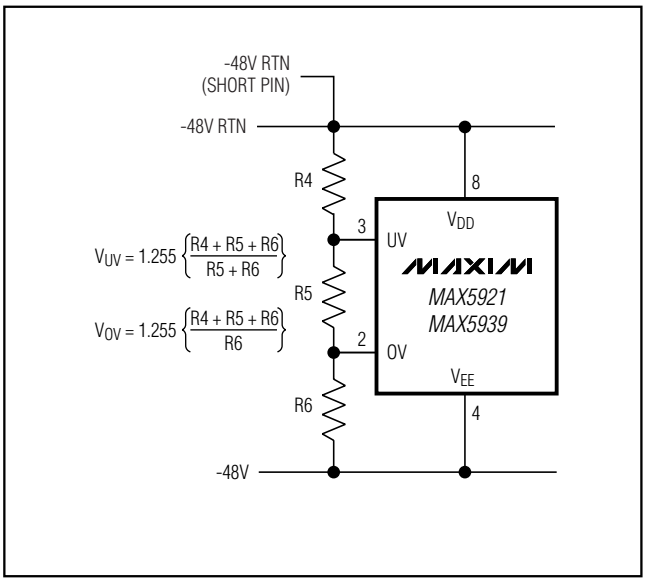

Figure 10. Undervoltage and Overvoltage Sensing

Overcurrent Fault Integrator

The MAX5921/MAX5939 feature an overcurrent fault integrator. When an overcurrent condition is detected, an internal digital counter is incremented. The clock period for the digital counter is 32µs for the 500µs maximum current-limit duration version and 128µs for 2ms maximum current-limit duration devices. An overcurrent of less than 32µs is interpreted as an overcurrent of 32µs. When the counter reaches 500µs (the maximum current-limit duration) for the MAX5921/MAX5939A, an overcurrent fault is generated. If the overcurrent fault does not last 500µs, then the counter begins decrementing at a rate 128 (maximum current-limit duty cycle) times slower than the counter was incrementing. Repeated overcurrent conditions generate a fault if the duty cycle of the overcurrent condition duty ratio is greater than the maximum current-limit duty cycle (see Figure 14).

Thermal Shutdown

The MAX5921/MAX5939 include internal die-temperature monitoring. When the die temperature reaches the thermal-shutdown threshold, T_{OT}, the MAX5921/MAX5939 pull GATE low and turn off the external MOSFET. If a good thermal path is provided between the MOSFET and the MAX5921/MAX5939, the device offers thermal protection for the external MOSFET. Placing the MAX5921/MAX5939 near the drain of the external MOSFET offers the best thermal protection because most of the power is dissipated in its drain.

After a thermal shutdown fault has occurred, the MAX5921_ turns the external FET off for a minimum time of t_{OFF}, allowing the MOSFET to cool down. The MAX5921_ device restarts after the temperature drops 20°C below the thermal-shutdown threshold.

The MAX5939_ latches off after a thermal shutdown fault. The MAX5939_ can be restarted by toggling UV low or cycling power. However, the device keeps the external FET off for a minimum time of t_{OFF} when toggling UV.

Applications Information

Sense Resistor

The circuit-breaker current-limit threshold is set to 50mV (typ). Select a sense resistor that causes a drop equal to or above the current-limit threshold at a current level above the maximum normal operating current. Typically, set the overload current to 1.5 to 2.0 times the nominal load current plus the dynamic load-capacitance charging current during startup. Choose the sense resistor power rating to be greater than $(V_{CL})^2 / R_{SENSE}$.

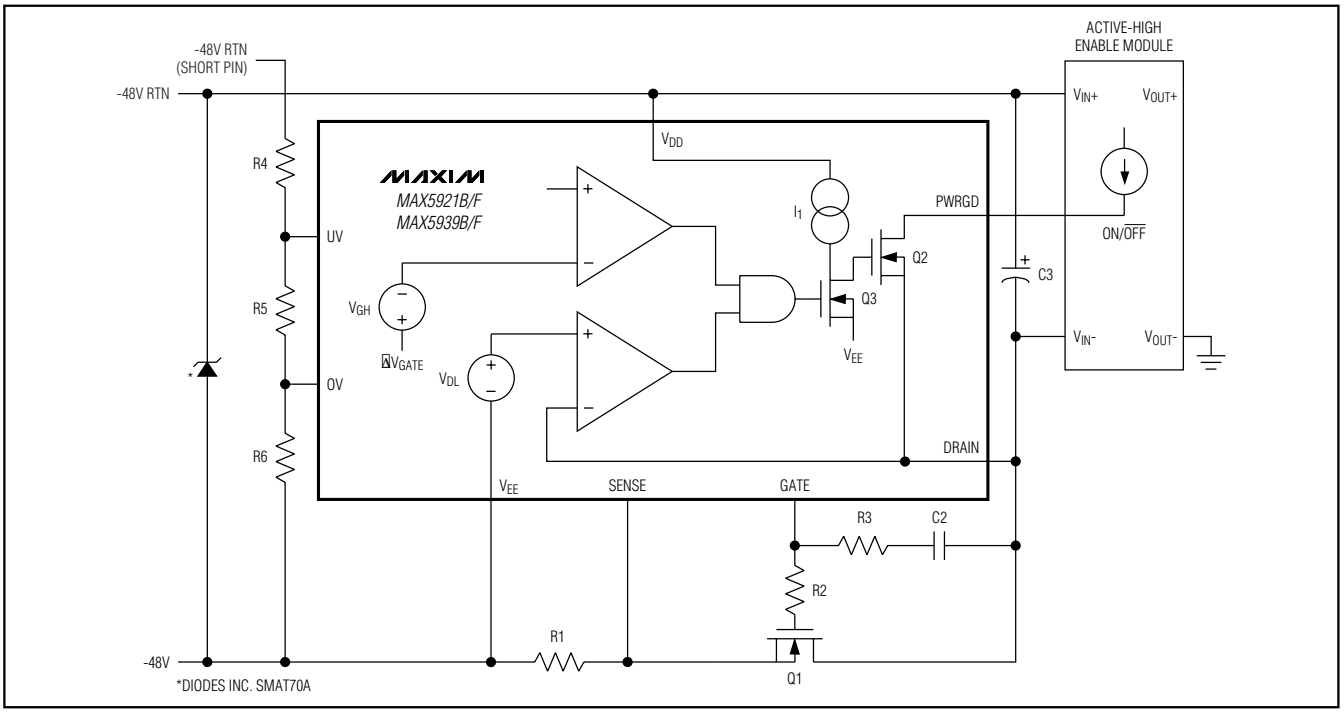

Figure 11. Active-High Enable Module

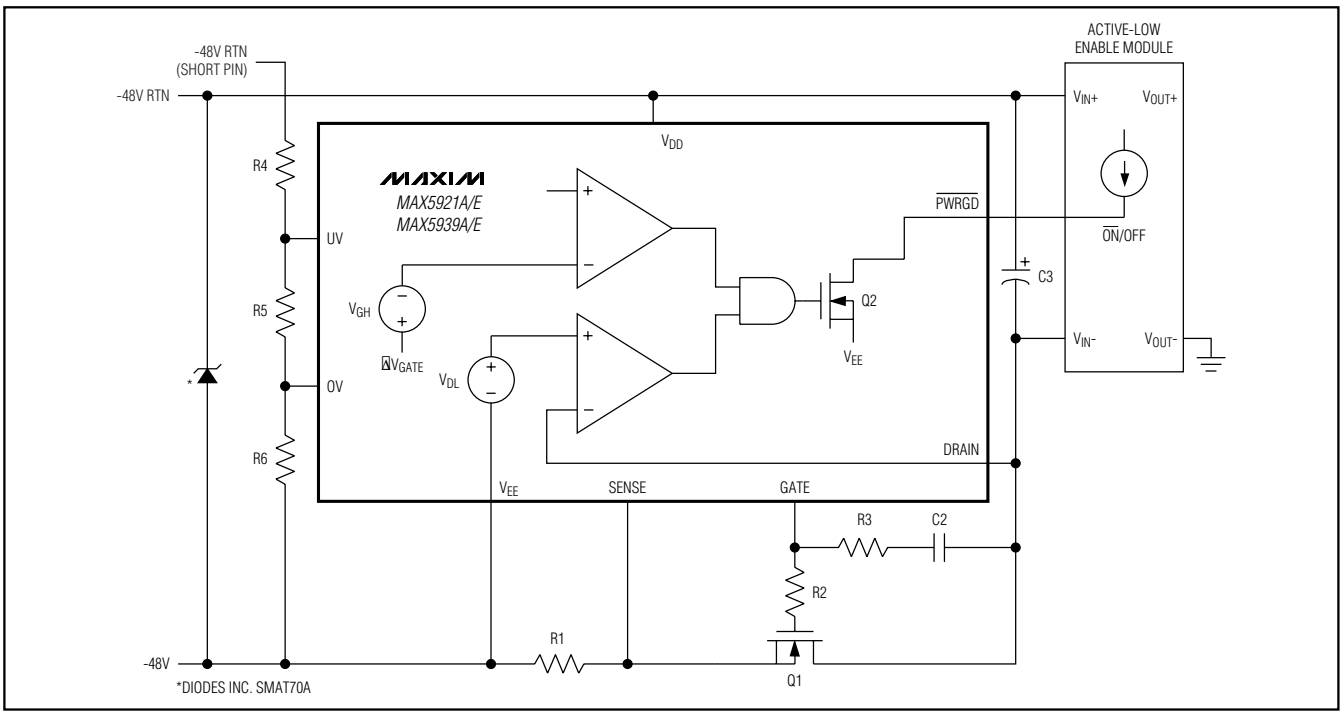

Figure 12. Active-Low Enable Module

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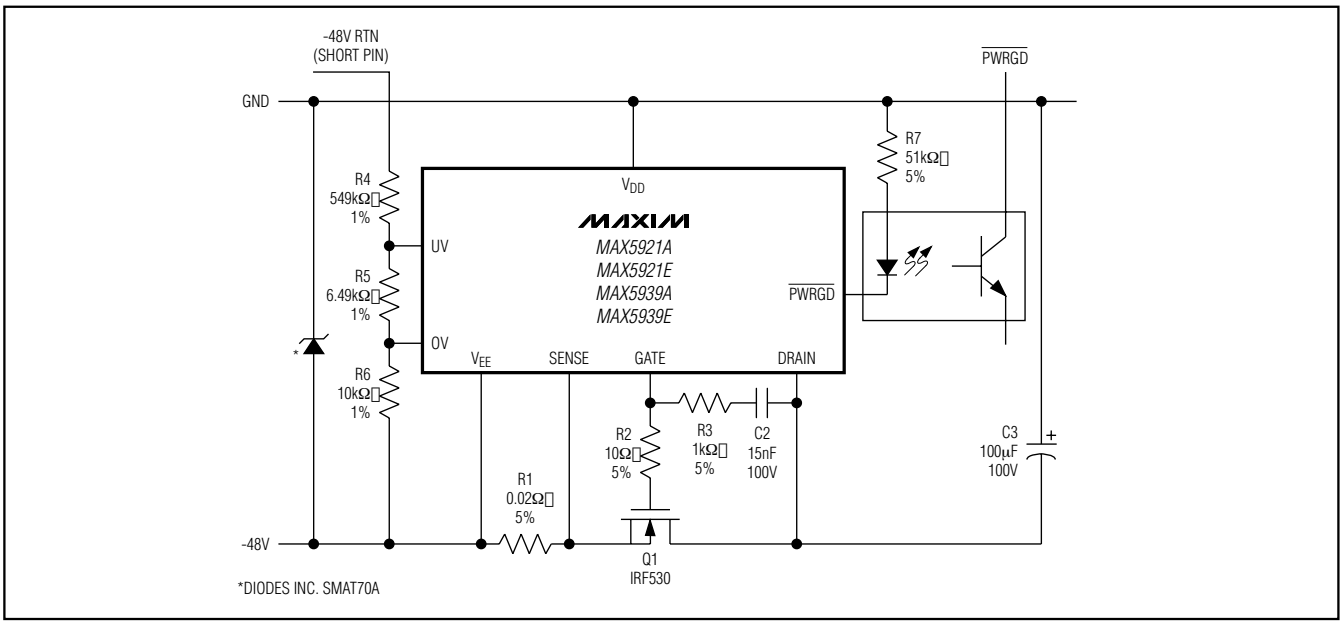


Figure 13. Using $\overline{PWRGD}$ to Drive an Optoisolator

Component Selection Procedure:

- Determine load capacitance:

  C_L = C2 + C3 + module input capacitance
- Determine load current, I_{LOAD}.
- Select circuit-breaker current, for example:

  $$I_{CB} = 2 \times I_{LOAD}$$
- Calculate R_{SENSE}:

  $$R_{SENSE} = \frac{50mV}{I_{CB}}$$

  Realize that I_{CB} varies ±20% due to trip-voltage tolerance.
- Set allowable inrush current:

  $$I_{INRUSH} \le 0.8 \times \frac{40mV}{R_{SENSE}} - I_{LOAD} \text{ or}$$

  $$I_{INRUSH} + I_{LOAD} \le 0.8 \times I_{CB(MIN)}$$
- Determine value of C2:

  $$C2 = \frac{45\mu A \times C_L}{I_{INRUSH}}$$
- Calculate value of C1:

  $$C1 = (C2 + C_{gd}) \times \left(\frac{V_{IN(MAX)} - V_{GS(TH)}}{V_{GS(TH)}} \right)$$
- Determine value of R3:

  $$R3 = \frac{150\mu s}{C2}$$
- Set R2 = 10Ω.
- If an optocoupler is utilized as in Figure 14, determine the LED series resistor:

  $$R7 = \frac{V_{IN(NOMINAL)} - 2V}{3 \le I_{LED} \le 5mA}$$

Although the suggested optocoupler is not specified for operation below 5mA, its performance is adequate for 36V temporary low-line voltage where LED current would then be ≈2.2mA to 3.7mA. If R7 is set as high as 51kΩ, optocoupler operation should be verified over the expected temperature and input voltage range to ensure suitable operation when LED current ≈0.9mA for 48V input and ≈0.7mA for 36V input.

If input transients are expected to momentarily raise the input voltage to >100V, select an input transient-voltage-suppression diode (TVS) to limit maximum voltage on the MAX5921/MAX5939 to less than 100V. A suitable device is the Diodes Inc. SMAT70A telecom-specific TVS.

Select Q1 to meet supply voltage, load current, efficiency, and Q1 package power-dissipation requirements:

$BV_{DSS} \ge 100V$

$I_{D(ON)} \ge 3 \times I_{LOAD}$

DPAK, D^2PAK, or TO-220AB

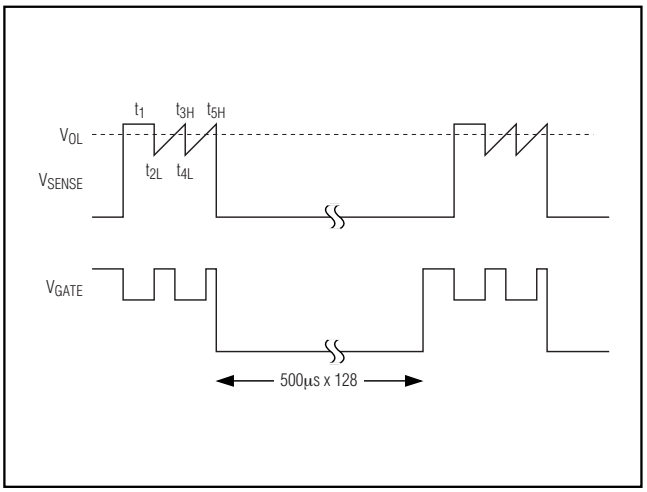


Figure 14. MAX5921A Overcurrent Fault Example

The lowest practical $R_{DS(ON)}$, within budget constraints and with values from 14mΩ to 540mΩ, are available at 100V breakdown.

Ensure that the temperature rise of Q1 junction is not excessive at normal load current for the package selected. Ensure that I_{CB} current during voltage transients does not exceed allowable transient-safe operating-area limitations. This is determined from the SOA and transient-thermal-resistance curves in the Q1 manufacturer's data sheet.

Example 1:

I_{LOAD} = 2.5A, efficiency = 98%, then V_{DS} = 0.96V is acceptable, or $R_{DS(ON)} \leq 384m\Omega$ at operating temperature is acceptable. An IRL520NS 100V NMOS with $R_{DS(ON)} \leq 180m\Omega$ and $I_{D(ON)}$ = 10A is available in D^2PAK. (A Vishay Siliconix SUD40N10-25 100V NMOS with $R_{DS(ON)} \leq 25m\Omega$ and $I_{D(ON)}$ = 40A is available in DPAK but may be more costly because of a larger die size).

Using the IRL520NS, $V_{DS} \leq 0.625V$ even at +80°C so efficiency ≥ 98.6% at 80°C. $P_D \leq 1.56W$ and junction temperature rise above case temperature would be 5°C due to the package θ_{JC} = 3.1°C/W thermal resistance. Of course, using the SUD40N10-25 will yield an efficiency greater than 99.8% to compensate for the increased cost.

If I_{CB} is set to twice I_{LOAD}, or 5A, V_{DS} momentarily doubles to ≤ 1.25V. If C_{OUT} = 4000µF, transient-line input voltage is Δ36V, the 5A charging-current pulse is:

$$t = \frac{4000\mu F \times 1.25V}{5A} = 1ms$$

Entering the data sheet transient-thermal-resistance curves at 1ms provides a θ_{JC} = 0.9°C/W. P_D = 6.25W, so Δt_{JC} = 5.6°C. Clearly, this is not a problem.

Example 2:

I_{LOAD} = 10A, efficiency = 98%, allowing V_{DS} = 0.96V but $R_{DS(ON)} \leq 96m\Omega$. An IRF530 in a D^2PAK exhibits $R_{DS(ON)} \leq 90m\Omega$ at +25°C and ≤ 135mΩ at +80°C. Power dissipation is 9.6W at +25°C or 14.4W at +80°C. Junction-to-case thermal resistance is 1.9°C/W, so the junction temperature rise would be approximately 5°C above the +25°C case temperature. For higher efficiency, consider IRL540NS with $R_{DS(ON)} \leq 44m\Omega$. This allows η = 99%, $P_D \leq 4.4W$, and T_{JC} = +4°C (θ_{JC} = 1.1°C/W) at +25°C.

Thermal calculations for the transient condition yield I_{CB} = 20A, V_{DS} = 1.8V, t = 0.5ms, transient θ_{JC} = 0.12°C/W, P_D = 36W and Δt_{JC} = 4.3°C.

Layout Guidelines

Good thermal contact between the MAX5921/MAX5939 and the external MOSFET is essential for the thermal-shutdown feature to operate effectively. Place the MAX5921/MAX5939 as close as possible to the drain of the external MOSFET and use wide circuit-board traces for good heat transfer. See Figure 15 for an example of recommended layout for Kelvin-sensing current through a sense resistor on a PC board.

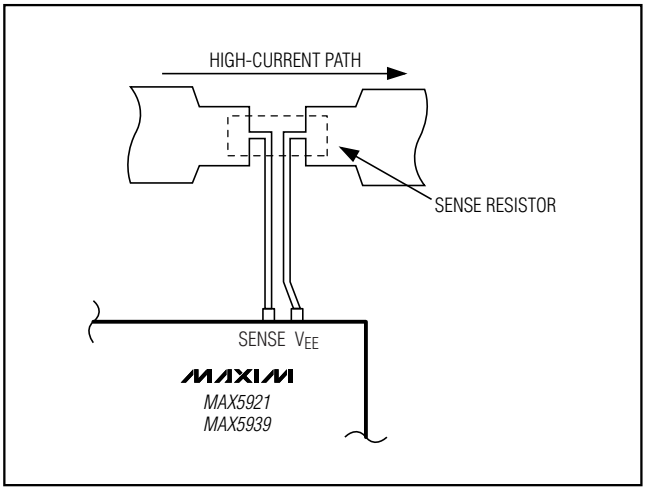


Figure 15. Recommended Layout for Kelvin-Sensing Current Through Sense Resistor

-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

Selector Guide

PART	DCEN POLARITY	FAULT MANAGEMENT	MAXIMUM CURRENT-LIMIT DURATION (ms)	MAXIMUM CURRENT-LIMIT DUTY CYCLE
MAX5921AESA	Active-Low $\overline{PWRGD}$	Autoretry	0.5	1/128
MAX5921BESA	Active-High PWRGD	Autoretry	0.5	1/128
MAX5921EESA	Active-Low $\overline{PWRGD}$	Autoretry	2	1/128
MAX5921FESA	Active-High PWRGD	Autoretry	2	1/128
MAX5939AESA	Active-Low $\overline{PWRGD}$	Latched	0.5	1/128
MAX5939BESA	Active-High PWRGD	Latched	0.5	1/128
MAX5939EESA	Active-Low $\overline{PWRGD}$	Latched	2	1/128
MAX5939FESA	Active-High PWRGD	Latched	2	1/128

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX5921EESA*	-40°C to +85°C	8 SO
MAX5921FESA*	-40°C to +85°C	8 SO
MAX5939AESA	-40°C to +85°C	8 SO
MAX5939BESA	-40°C to +85°C	8 SO
MAX5939EESA*	-40°C to +85°C	8 SO
MAX5939FESA*	-40°C to +85°C	8 SO

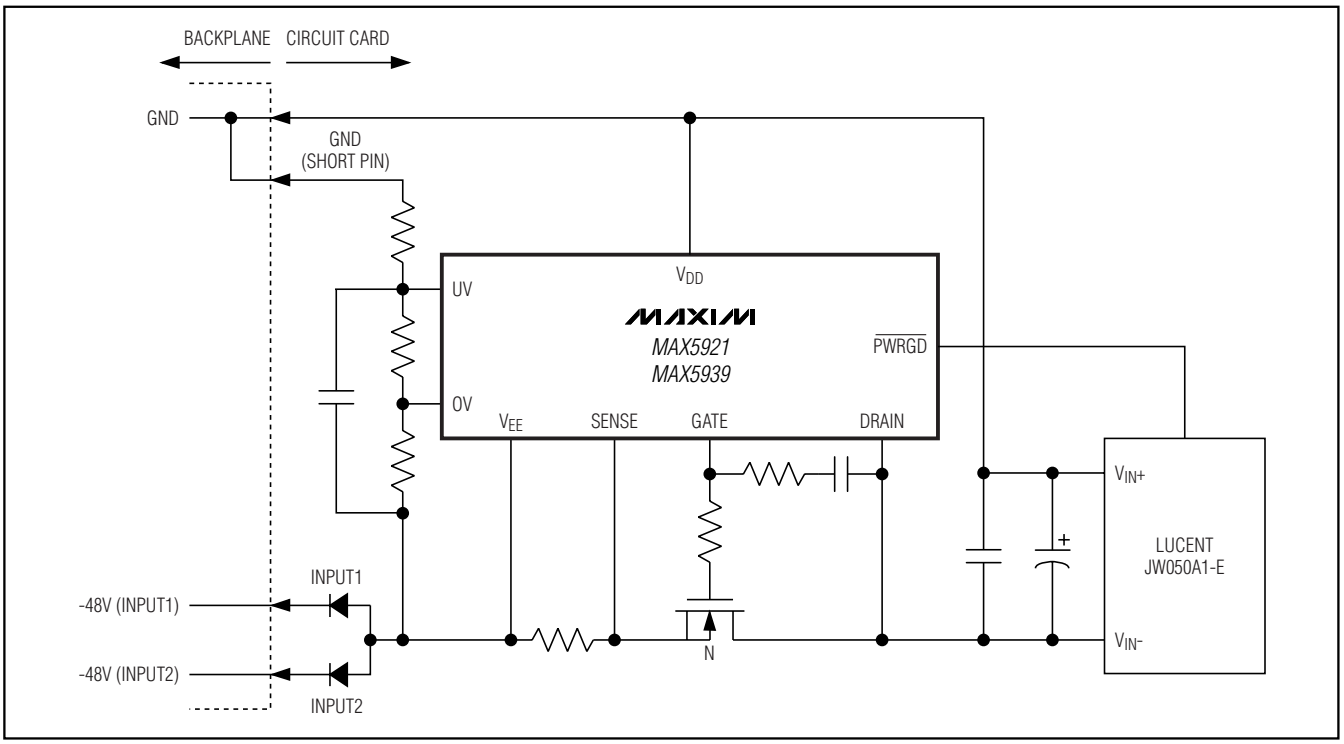
**Future product—contact factory for availability.*

Chip Information

TRANSISTOR COUNT: 2645

PROCESS: BiCMOS

Typical Operating Circuit

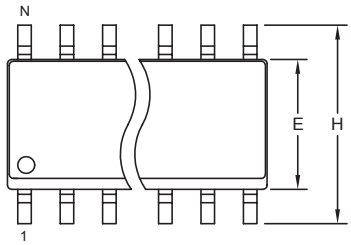


-48V Hot-Swap Controllers with External RSENSE and High Gate Pulldown Current

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOICN .EPS

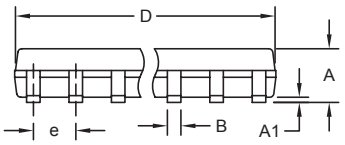


TOP VIEW

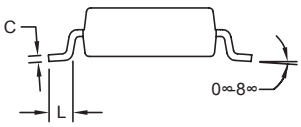
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050 BSC		1.27 BSC	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27

VARIATIONS:

	INCHES		MILLIMETERS			
DIM	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	AA
D	0.337	0.344	8.55	8.75	14	AB
D	0.386	0.394	9.80	10.00	16	AC



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. LEADS TO BE COPLANAR WITHIN 0.10mm (.004").
4. CONTROLLING DIMENSION: MILLIMETERS.
5. MEETS JEDEC MS012.
6. N = NUMBER OF PINS.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, .150" SOIC

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0041	B	1/1

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