ABSOLUTE MAXIMUM RATINGS

ENABLE to GND	0.3V to +70.0V 0.3V to +12.0V
UVLO to GND	0.3V to +12.0V 0.3V to (V _{IN} + 0.3V) 10mA
Continuous Power Dissipation 8-Pin SO (derate 5.9mW/°C	

Operating Temperature Range	40°C to +85°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	60°C to +150°C
Lead Temperature (soldering 10s	s)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{IN} = +42V, GND = 0, UVLO = open circuit, V_{ENABLE} = +3.3V, and T_A = -40^{\circ}C to +85^{\circ}C, unless otherwise noted. Typical values are at T_A = +25^{\circ}C.)$

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V _{IN}			10		65	V
Supply Current	I _{IN}	V _{IN} = 10V to 65V (Note 1)			1.2	2.5	mA
Output Current Limit	ILIM	V _{OUT} = V _{IN} - 5V, V _{IN} = 10V to 65V	MAX5910	250	280	310	mA
			MAX5917A	510	567	623	
			MAX5917B	370	420	470	
0		(Note 2)	MAX5910			240	mA
Continuous Operating Output Current	lout		MAX5917A			400	
Carrent			MAX5917B			350	
DMOS On-Resistance	R _{DS} (ON)	V _{IN} = 10V to 65V, MAX5910, I _{OUT} = 200mA MAX5917A, I _{OUT} = 400mA MAX5917B, I _{OUT} = 300mA			2.2	4	Ω
ENABLE Voltage Logic Low	V _{LOW}					0.8	V
ENABLE Voltage Logic High	VHIGH			2.4			V
ENABLE High Input Current	lін	VENABLE = +5V				1	μА
IFAULT Output Leakage Current	Іон	IFAULT = 10V, I _{OH} > (IF _{TH} + IF _{HYS})				1	μΑ
PGOOD Output Leakage Current	ILPGOOD	PGOOD = 10V, V _{OUT} > V _{PG}				1	μА
V _{IN} to V _{OUT} Leakage Current	IL _{IN/OUT}	ENABLE = 0, V _{IN} = +65V				1	μА
PGOOD/IFAULT Output Logic Low	V _{OL}	Sink current = 3mA				0.4	V
PGOOD Threshold	V _{PG}	Percentage of VIN, VOUT rising		71	78	85	%
PGOOD Hysteresis	PGHYS	Percentage of V _{IN}			10		%
Zero-Current Detection	IFTH	Decreasing output current	MAX5910	2	12	25	
Threshold			MAX5917A	2	6	10	mA
		MAX5917B		2	12	25	

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{IN} = +42V, GND = 0, UVLO = open circuit, V_{ENABLE} = +3.3V, and T_A = -40^{\circ}C to +85^{\circ}C, unless otherwise noted. Typical values are at T_A = +25^{\circ}C.)$

PARAMETER	SYMBOL	CONDITIONS		TYP	MAX	UNITS
Zero-Current Detection Threshold Hysteresis	IF _{HYS}	Percentage of IF _{TH}		10		%
IFAULT Output Delay	tIFD	(Figure 1)	7	12	17	ms
PGOOD Output Delay	tpgD	(Figure 2)		12	17	ms
Thermal Shutdown Temperature	TJ	Die temperature increasing		140		°C
Thermal Shutdown Hysteresis	TJHYS			3.5		°C
Default Undervoltage Lockout	V _{UVLO}	V _{IN} decreasing	24.5	26.5	28.5	V
Undervoltage Lockout Hysteresis	UVLO _{HYS}	Percentage of V _{UVLO}		11		%
Minimum Undervoltage Lockout Threshold	Vuvlo (MIN)	UVLO connected to V _{IN} , V _{IN} decreasing	7	7.5	8	V
Undervoltage Lockout Input Resistance	R _{UVLO}	Force I = 5μA into UVLO pin	260			kΩ

Note 1: Measured at GND pin at the end of the output voltage slew.

Note 2: Guaranteed by RDSON test. Limited by package power dissipation.

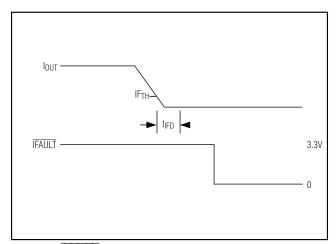


Figure 1. IFAULT Delay

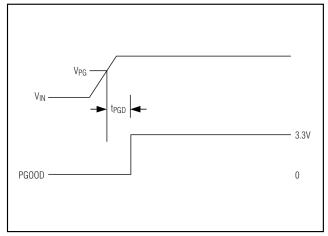
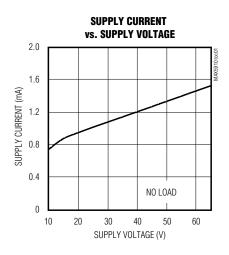
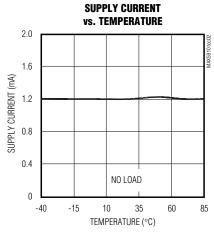


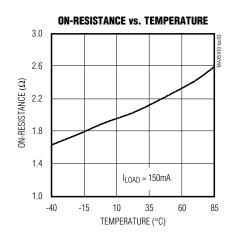
Figure 2. Power-Good Delay

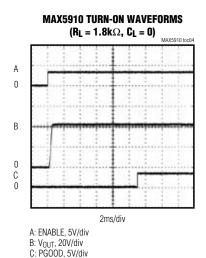
Typical Operating Characteristics

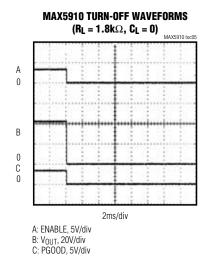
 $(V_{IN} = +42V, GND = 0, UVLO = open circuit, V_{ENABLE} = 3.3V, R_L = 1.8k\Omega, T_A = +25^{\circ}C, unless otherwise noted).$

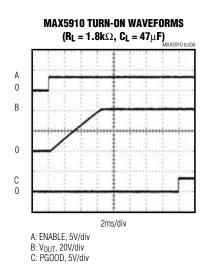








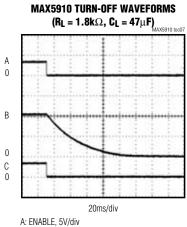


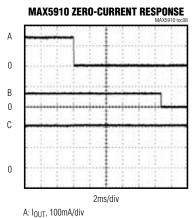


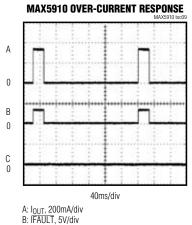
4 _______/V|/X|/V|

_Typical Operating Characteristics (continued)

 $(V_{IN} = +42V, GND = 0, UVLO = open circuit, V_{ENABLE} = 3.3V, R_{L} = 1.8k\Omega, T_{A} = +25^{\circ}C, unless otherwise noted).$





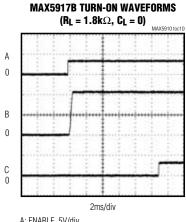


B: V_{OUT}, 20V/div C: PGOOD, 5V/div A: I_{OUT}, 100mA/div B: IFAULT, 5V/div C: V_{OUT}, 20V/div

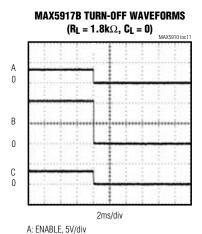
B: V_{OUT}, 20V/div

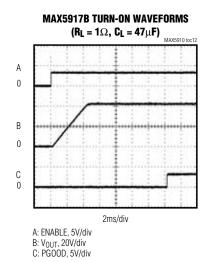
C: PGOOD, 5V/div

B: IFAULT, 5V/div C: V_{OUT}, 20V/div (SHORTED TO GND)



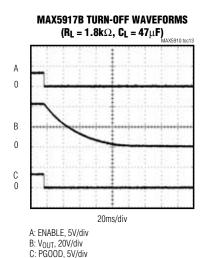


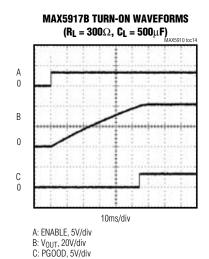


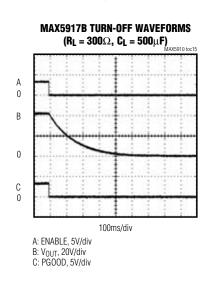


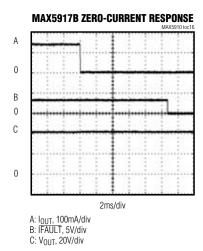
Typical Operating Characteristics (continued)

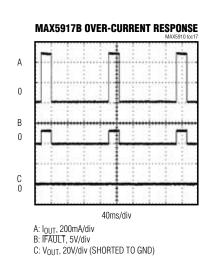
 $(V_{IN} = +42V, GND = 0, UVLO = open circuit, V_{ENABLE} = 3.3V, R_{L} = 1.8k\Omega, T_{A} = +25^{\circ}C, unless otherwise noted).$

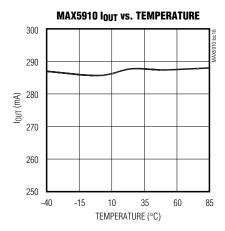








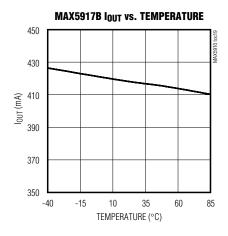


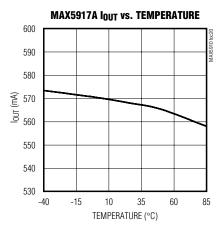


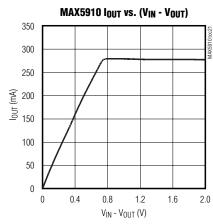
6 _________/V|/X|/V|

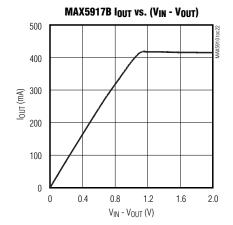
Typical Operating Characteristics (continued)

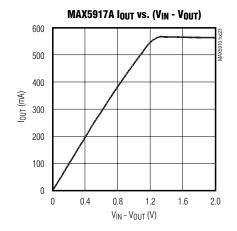
 $(V_{IN} = +42V, GND = 0, UVLO = open circuit, V_{ENABLE} = 3.3V, R_L = 1.8k\Omega, T_A = +25^{\circ}C, unless otherwise noted).$











Pin Description

PIN		NAME	FUNCTION
MAX5910	MAX5917A/B	NAME	FUNCTION
1	2	UVLO	Undervoltage Lockout Input. Leave UVLO open circuit for the default setting of 26.5V. Alternatively, UVLO can be connected to a resistive-divider to set a desired lockout voltage. See the <i>Changing the Undervoltage Lockout Setting</i> section.
2	3	VIN	Voltage Input Terminal. Bypass V_{IN} to GND with a 0.1 μF capacitor to improve noise immunity.
3	1, 6, 8, 9, 15, 16	N.C.	No Connection. Not internally connected.
4	7	ENABLE	3.3V Logic Input (TTL compatible), Active-High. Turns the internal FET on or off. Drive ENABLE high to enable V _{OUT} . Drive ENABLE low to disable V _{OUT} .
5	10	PGOOD	Open-Drain Logic Output, Active-High. PGOOD signals that the output is within specification. When the output is less than 70% of the input, the PGOOD signal is pulled low. Connect a $10\text{k}\Omega$ pullup resistor (R) to 3.3V .
6	11	ĪFAULT	Open-Drain Logic Output, Active-Low. $\overline{\text{IFAULT}}$ is asserted when the output current falls below the IF _{TH} nominal threshold or when the switch is off. Connect a $10k\Omega$ pullup resistor (R) to 3.3V.
7	4, 5, 12, 13	GND	Ground
8	14	Vout	Voltage Output Terminal

Detailed Description

The MAX5910/MAX5917 are fully integrated hot-swap switches for positive power-supply rails. The devices allow safe insertion and removal of circuit cards into live backplanes or ports without causing glitches on the backplane power-supply rail. During startup these devices act as current regulators using their on-board FET to limit the amount of current drawn by the load to 280mA for MAX5910, 567mA for MAX5917A, and 420mA for MAX5917B. If the required load current exceeds that current limit, the internal switch behaves like a constant current source.

The MAX5910/MAX5917 monitor the input voltage, the output voltage, the output current, and the die temperature. They assert IFAULT and PGOOD accordingly if they detect an error condition.

A zero-current load detection feature activates if the load current drops below IF_{TH} for over 12ms. The MAX5910/MAX5917 also include an ENABLE input allowing the host system to turn the FET on or off.

Normal Operation

Startup

When power is first applied with ENABLE high, or when ENABLE is asserted, the MAX5910/MAX5917A/MAX5917B limit the current to the load to 280mA/567mA/420mA. PGOOD is asserted high 12ms after the output voltage exceeds the power-good threshold. PGOOD is pulled low if VOUT is less than 70% VIN.

Zero-Current Load Fault

A zero-current load detection feature activates if the load current drops below IF_{TH} for more than 12ms. The MAX5910/MAX5917 flag the zero-current condition but do not disconnect the load. IFAULT is deasserted whenever the load current exceeds the IF_{TH} + IF_{HYS} zero-current detection threshold.

Undervoltage Lockout Fault

If $V_{IN} \leq UVLO$, where UVLO is the desired voltage at which the UVLO fault occurs, the internal FET is turned off and \overline{IFAULT} and PGOOD are pulled low. The default UVLO voltage is 26.5V, but it can be adjusted using an external resistive-divider (see the *Changing the Undervoltage Lockout Setting* section).

Thermal Shutdown Fault

The MAX5910/MAX5917 monitor their internal die temperature. If the temperature of the <u>die exceeds +140°C</u>, the internal FET is turned off and <u>IFAULT</u> and PGOOD are pulled low. The output is enabled again only when the die temperature is below the thermal shutdown temperature by 3.5°C typically.

Power-Good (PGOOD)

Power-good (PGOOD) logic output signals when the output has exceeded the PGOOD threshold. When the output voltage is below 70% of the input voltage, PGOOD is pulled low. When the output voltage is larger than 80% of the input voltage for more than 12ms, PGOOD is asserted.

Applications Information

Choosing a Device

The MAX5910 can output 280mA, the MAX5917B can output 420mA, and the MAX5917A can output up to 567mA. In applications where high power is expected, use the MAX5917 for its superior heat dissipation properties, and always solder all of its GND pins to a large section of circuit board copper.

Logic Control

The enable input (ENABLE) responds to 3.3V logic signals and will force the internal FET off if ENABLE is pulled low. This feature allows the host to disconnect the load from the power bus if required. Drive ENABLE high to enable Vout.

Changing the Undervoltage Lockout Setting

The undervoltage lockout (UVLO) value defaults to 26.5V if the UVLO pin is left open circuit (Figure 3). Connect UVLO to V_{IN} to set the undervoltage lockout to a minimum of 7.5V (Figure 4). This lockout voltage can also be changed with a resistive-divider from V_{IN} to GND. The center node of the divider is connected to the UVLO pin (Figure 5). The values of R1 and R2 must satisfy the condition R1//R2 << $260 k\Omega$ and R2 << $1.65 M\Omega$. R2 can be calculated as follows:

$$R2 = R1 \times [(V_{UVLO} / 7.5V) - 1]$$

where V_{IN (UVLO)} is the desired lockout voltage.

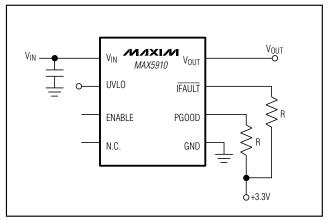


Figure 3. UVLO is Set Internally to its +26.5V Default Value

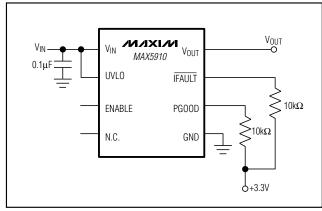


Figure 4. Minimum +7.5V UVLO Configuration

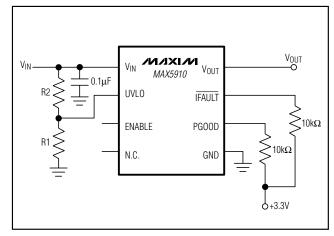
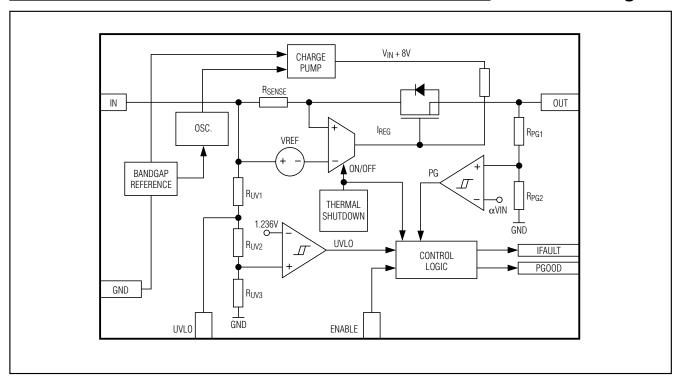
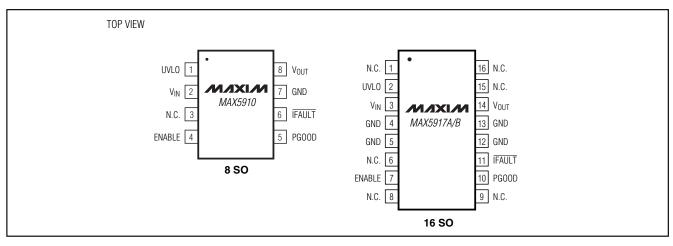


Figure 5. Adjusting UVLO with an External Resistive-Divider

Functional Diagram



Pin Configurations



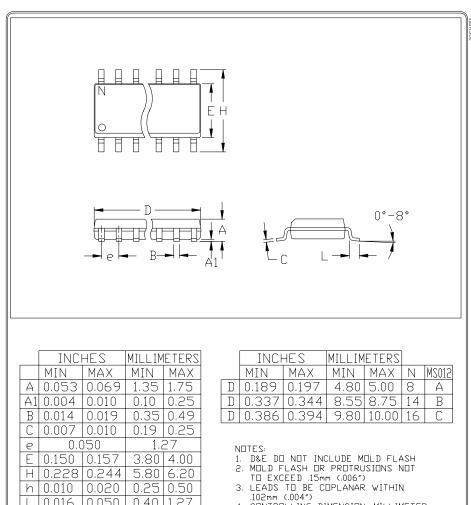
10 ______/VIXI/VI

Chip Information

TRANSISTOR COUNT: 1003

PROCESS: SG3ISO

Package Information



CONTROLLING DIMENSION: MILLIMETER
MEETS JEDEC MS012-XX AS SHOWN
IN ABOVE TABLE

N = NUMBER OF PINS

0.016 0.050

PACKAGE FAMILY DUTLINE: SDIC .150"



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