Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SOT23

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .... -0.3V to +6V
All Other Pins to GND (Note 1).................. -0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 8.7mW/°C above +70°C)...........696mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: The outputs may be shorted to V_{DD} or GND if the package power dissipation is not exceeded. Typical short-circuit current to GND is 70mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, REF = V_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution	N		8			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic		±0.3	±1	LSB
Integral Nonlinearity	INL	(Note 2)		±0.3	±1	LSB
Total Unadjusted Error	TUE	(Note 2)		±1		LSB
Zero-Code Offset	V_{ZS}			10		mV
Zero-Code Temperature Coefficient	TCV_{ZS}			100		µV/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V, V_{REF} = 4.096V		0.15		mV/V
		2.7V ≤ V_{DD} ≤ 3.6V, V_{REF} = 2.4V		0.5		
REFERENCE INPUT						
Reference Input Voltage Range			GND		V_{DD}	V
Reference Input Capacitance				25		pF
Reference Input Resistance	R_{REF}	(Note 3)	8	16		kΩ
Reference Input Resistance (Shutdown Mode)				2		MΩ
DAC OUTPUTS						
Output Voltage Range			0		REF	V
Capacitive Load at OUT_					100	pF
Output Resistance				50		Ω
DIGITAL INPUTS						
Input High Voltage	V_{IH}		0.7 x V_{DD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DD}	V
Input Current	I_{IN}	V_{IN} = 0 or V_{DD}		0.1	±10	µA
Input Capacitance	C_{IN}	(Note 4)			10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, REF = V_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate	SR	C_L = 100pF			1		V/µs
Voltage-Output Settling Time		To ±½LSB, C_L = 100pF			10		µs
Digital Feedthrough and Crosstalk		All 0s to all 1s			0.25		nV-s
POWER SUPPLY							
Supply Voltage Range	V_{DD}			2.7		5.5	V
Supply Current	I_{DD}	All inputs = 0	V_{DD} = 5.5V		0.55	1	mA
			V_{DD} = 3.6V		0.38	0.8	
Shutdown Supply Current		V_{DD} = 5.5V			0.1		µA

TIMING CHARACTERISTICS

(Figure 3, V_{DD} = +2.7V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL INTERFACE TIMING						
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		50			ns
SCLK Rise to $\overline{CS}$ Rise Setup Time	t_{CSH}		50			ns
DIN to SCLK Rise Setup Time	t_{DS}		20			ns
DIN to SCLK Rise Hold Time	t_{DH}		20			ns
SCLK Pulse Width High	t_{CH}		20			ns
SCLK Pulse Width Low	t_{CL}		20			ns
$\overline{CS}$ Pulse Width High	t_{CSPWH}		50			ns

Note 2: Reduced digital code range (code 24 through code 232) is due to swing limitations of the output amplifiers. See *Typical Operating Characteristics*.

Note 3: Reference input resistance is code dependent. The lowest input resistance occurs at code 55hex. See the *Reference Input* section.

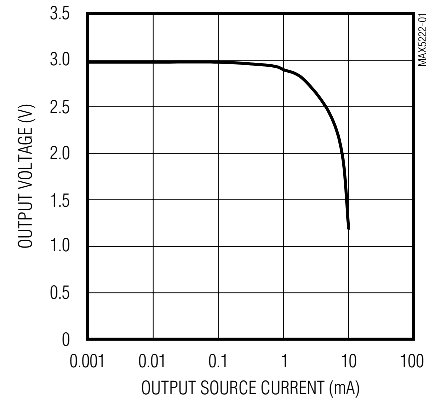
Note 4: Guaranteed by design. Not production tested.

Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SOT23

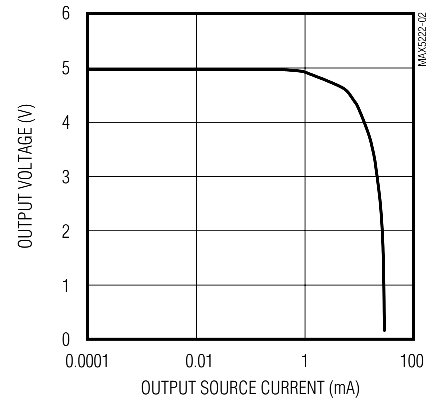
Typical Operating Characteristics

(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

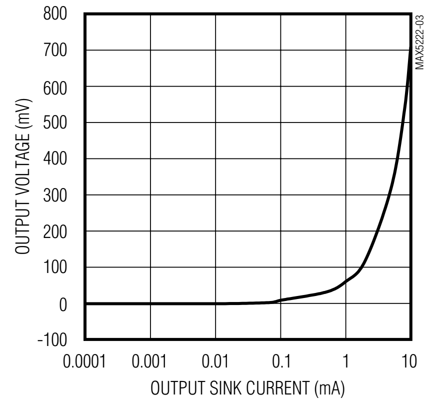
OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT (V_{DD} = 3V)



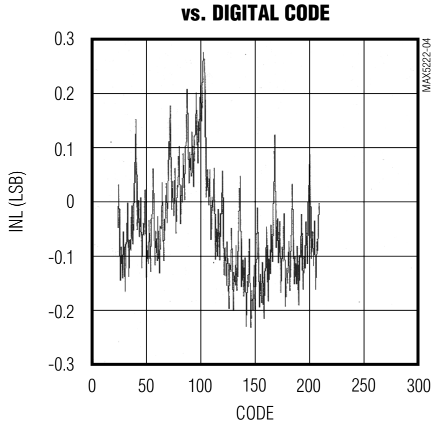
OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT (V_{DD} = 5V)



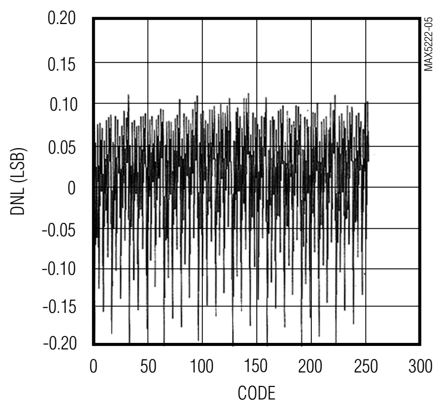
OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



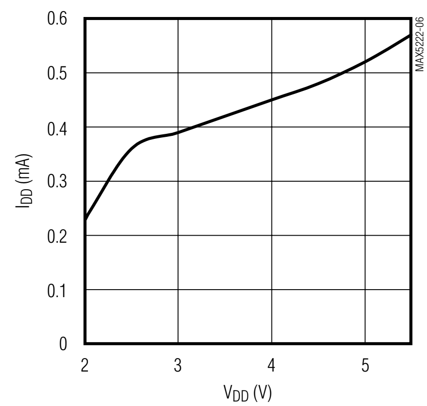
INTEGRAL NONLINEARITY vs. DIGITAL CODE



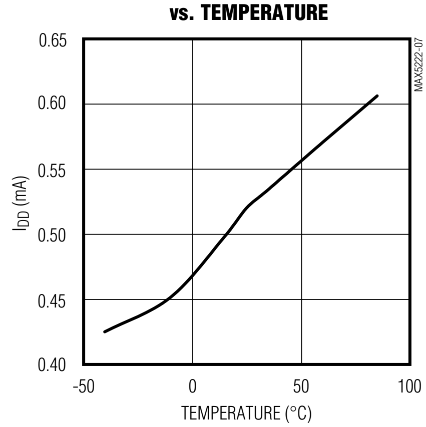
DIFFERENTIAL NONLINEARITY vs. DIGITAL CODE



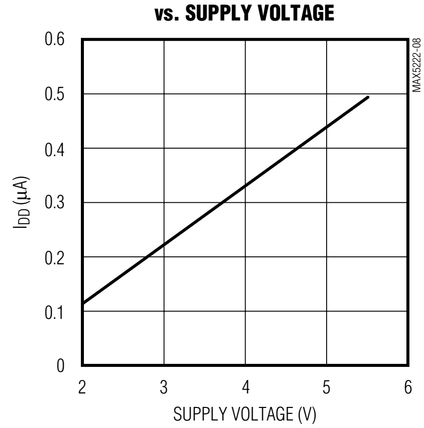
POSITIVE SUPPLY CURRENT vs. SUPPLY VOLTAGE



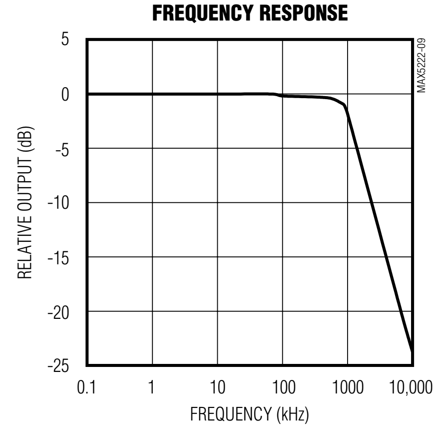
POSITIVE SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



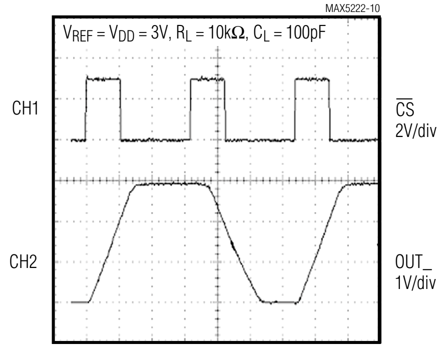
REFERENCE SMALL-SIGNAL FREQUENCY RESPONSE



Typical Operating Characteristics (continued)

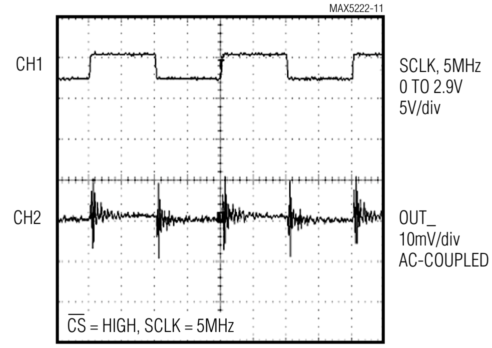
(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)

LARGE-SIGNAL OUTPUT STEP RESPONSE



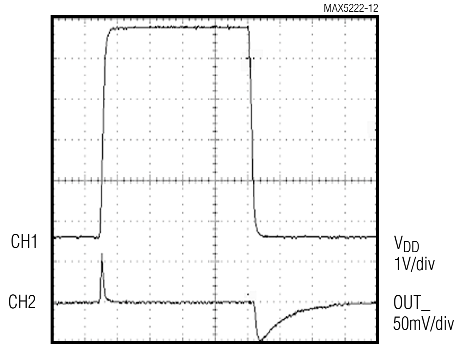
2µs/div

CLOCK FEEDTHROUGH



50ns/div

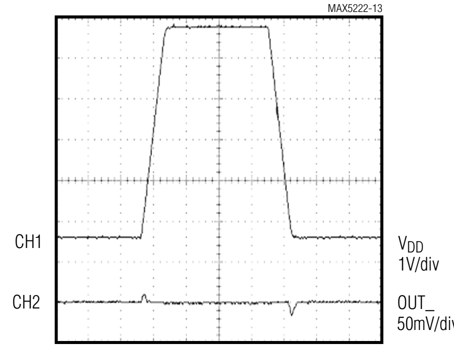
POWER-UP OUTPUT GLITCH



100µs/div

V_{DD} = CHANGES BETWEEN 0 AND 5V
RAMP TIME IS 10µs

POWER-UP OUTPUT GLITCH



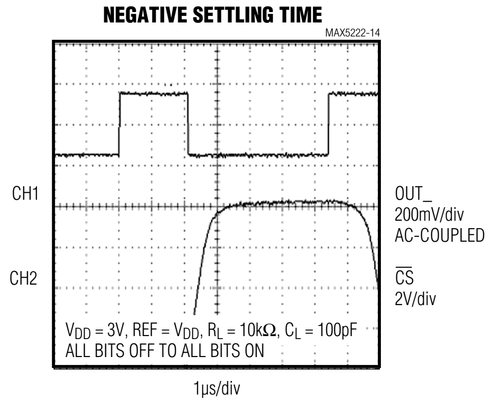
2ms/div

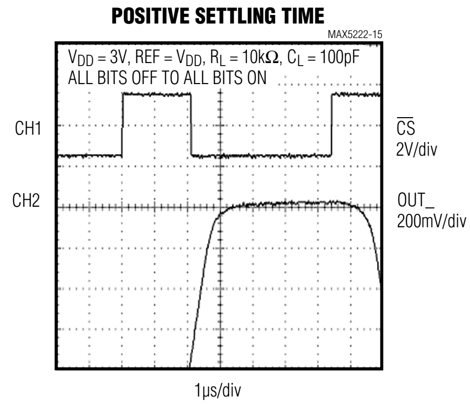
V_{DD} = CHANGES BETWEEN 0 AND 5V
RAMP TIME IS 1ms

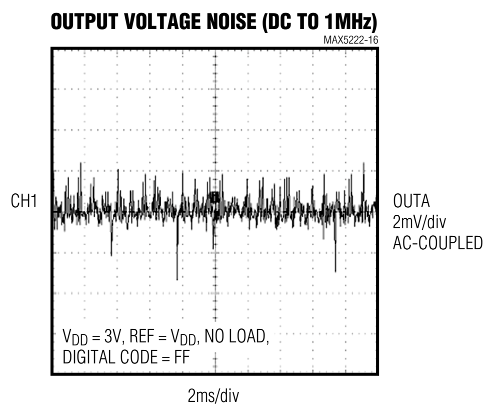
Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SOT23

Typical Operating Characteristics (continued)

(V_{DD} = +3V, T_A = +25°C, unless otherwise noted.)







Pin Description

PIN	NAME	FUNCTION
1	$\overline{CS}$	Chip Select, Active Low. Enables data to be shifted into the 16-bit shift register. Programming commands are executed at the rising edge of $\overline{CS}$.
2	GND	Ground
3	V_{DD}	Positive Power Supply (+2.7V to +5.5V). Bypass with 0.22µF to GND.
4	SCLK	Serial Clock Input. Data is clocked in on the rising edge of SCLK.
5	OUTA	DAC A Output Voltage (Buffered)
6	OUTB	DAC B Output Voltage (Buffered)
7	REF	Reference Input for DAC A and DAC B
8	DIN	Serial Data Input of the 16-bit Shift Register. Data is clocked into the register on the rising edge of SCLK.

Detailed Description

Analog Section

The MAX5222 contains two 8-bit, voltage-output DACs. The DACs are “inverted” R-2R ladder networks using complementary switches that convert 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage.

The MAX5222 has one reference input that is shared by DAC A and DAC B. The device includes output buffer amplifiers for both DACs and input logic for simple microprocessor (µP) and CMOS interfaces. The power-supply range is from +5.5V down to +2.7V.

Reference Input and DAC Output Range

The voltage at REF sets the full-scale output of the DACs. The input impedance of the REF input is code dependent. The lowest value, approximately 8kΩ, occurs when the input code is 01010101 (55hex). The maximum value of infinity occurs when the input code is zero.

In shutdown mode, the selected DAC output is set to zero, while the value stored in the DAC register remains unchanged. This removes the load from the reference input to save power. Bringing the MAX5222 out of shutdown mode restores the DAC output voltage. Because the input resistance at REF is code dependent, the DAC’s reference source should have an output impedance of no more than 5Ω. The input capacitance at the REF pin is also code dependent and typically does not exceed 25pF.

The reference voltage on REF can range anywhere from GND to V_{DD}. See the *Output Buffer Amplifier* section for more information.

Figure 1 is the DAC simplified circuit diagram.

Output Buffer Amplifiers

DAC A and DAC B voltage outputs are internally buffered. The buffer amplifiers have a Rail-to-Rail® (GND to V_{DD}) output voltage range.

Both DAC output amplifiers can source and sink up to 1mA of current. See the INL vs. Digital Code graph in the *Typical Operating Characteristics*. The amplifiers are unity-gain stable with a capacitive load of 100pF or smaller. The slew rate is typically 1V/µs.

Shutdown Mode

When programmed to shutdown mode, the outputs of DAC A and DAC B are passively pulled to GND with a series 5kΩ resistor. In shutdown mode, the REF input is high impedance (2MΩ typical) to conserve current drain from the system reference; therefore, the system reference does not have to be powered down.

Coming out of shutdown, the DAC outputs return to the values kept in the registers. The recovery time is equivalent to the DAC settling time.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SOT23

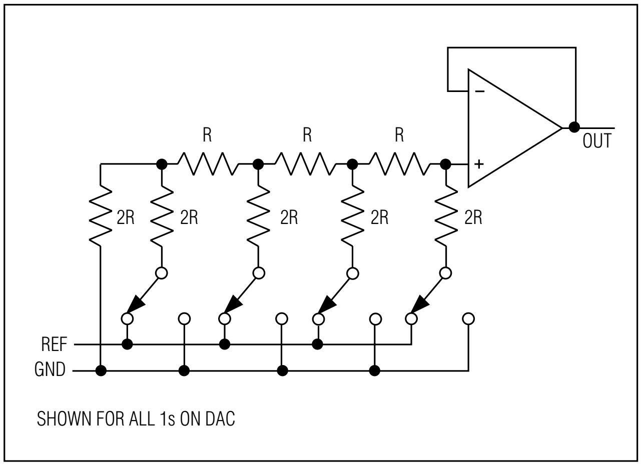


Figure 1. DAC Simplified Circuit Diagram

Serial Interface

An active-low chip select ($\overline{CS}$) enables the shift register to receive data from the serial data input. Data is clocked into the shift register on every rising edge of the serial clock signal (SCLK). The clock frequency can be as high as 25MHz.

Data is sent most significant bit (MSB) first and can be transmitted in one 16-bit word. The write cycle can be segmented when $\overline{CS}$ is kept active (low) to allow, for example, two 8-bit-wide transfers. After clocking all 16 bits into the input shift register, the rising edge of $\overline{CS}$ updates the DAC outputs and the shutdown status. Because of their single buffered structure, DACs cannot be simultaneously updated to different digital values.

Table 1. Input Shift Register

DATA BITS	B0*	DAC Data Bit 0 (LSB)
	B1	DAC Data Bit 1
	B2	DAC Data Bit 2
	B3	DAC Data Bit 3
	B4	DAC Data Bit 4
	B5	DAC Data Bit 5
	B6	DAC Data Bit 6
	B7	DAC Data Bit 7 (MSB)
CONTROL BITS	LA	Load Reg DAC A, Active High
	LB	Load Reg DAC B, Active High
	UB4	Uncommitted Bit 4
	SA	Shut Down, Active High
	SB	Shut Down, Active High
	UB3	Uncommitted Bit 3
	UB2	Uncommitted Bit 2
	UB1**	Uncommitted Bit 1

**Clocked in last.*
***Clocked in first.*

Serial-Input Data Format and Control Codes

Table 2 lists the serial-input data format. The 16-bit input word consists of an 8-bit control byte and an 8-bit data byte. The 8-bit control byte is not decoded internally. Every control bit performs one function. Data is clocked in starting with UB1 (uncommitted bit), followed by the remaining control bits and the data byte. The least significant bit (LSB) of the data byte (B0) is the last bit clocked into the shift register (Figure 2).

Table 3 is an example of a 16-bit input word. It performs the following functions:

- 80 hex (128 decimal) loaded into DAC registers A and B.
- DAC A and DAC B are active.

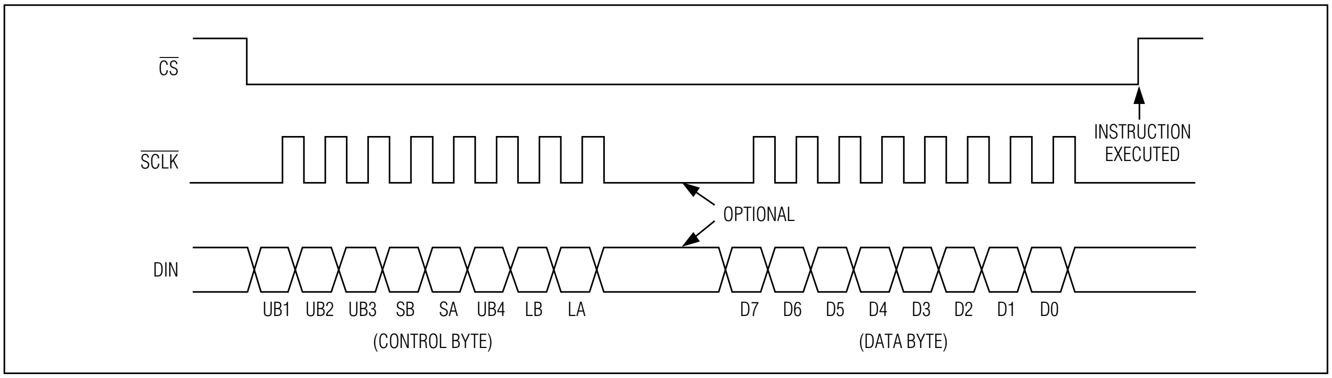


Figure 2. 3-Wire Serial-Interface Timing Diagram

Table 2. Serial-Interface Programming Commands

CONTROL								DATA								FUNCTION
UB1	**UB2**	**UB3**	**SB**	**SA**	**UB4**	**LB**	**LA**	**B7 MSB**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0 LSB**	
X	X	1	*	*	0	0	0	X	X	X	X	X	X	X	X	No Operation to DAC Registers
X	X	1	*	*	0	0	0									Unassigned Command
X	X	1	*	*	0	1	0	8-Bit DAC Data								Load Register to DAC B
X	X	1	*	*	0	0	1	8-Bit DAC Data								Load Register to DAC A
X	X	1	*	*	0	1	1	8-Bit DAC Data								Load Both DAC Registers
X	X	1	0	0	0	*	*	X	X	X	X	X	X	X	X	All DACs Active
X	X	1	0	0	0	*	*	X	X	X	X	X	X	X	X	Unassigned Command
X	X	1	1	0	0	*	*	X	X	X	X	X	X	X	X	Shut Down
X	X	1	0	1	0	*	*	X	X	X	X	X	X	X	X	Shut Down
X	X	1	1	1	0	*	*	X	X	X	X	X	X	X	X	Shut Down

X = Don't care.
** = Not shown, for the sake of clarity. The functions of loading and shutting down the DACs and programming the logic can be combined in a single command.*

Table 3. Example of a 16-Bit Input Word

LOADED IN FIRST															**LOADED IN LAST**
UB1	**UB2**	**UB3**	**SB**	**SA**	**UB4**	**LB**	**LA**	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
X	X	1	0	0	0	1	1	1	0	0	0	0	0	0	0

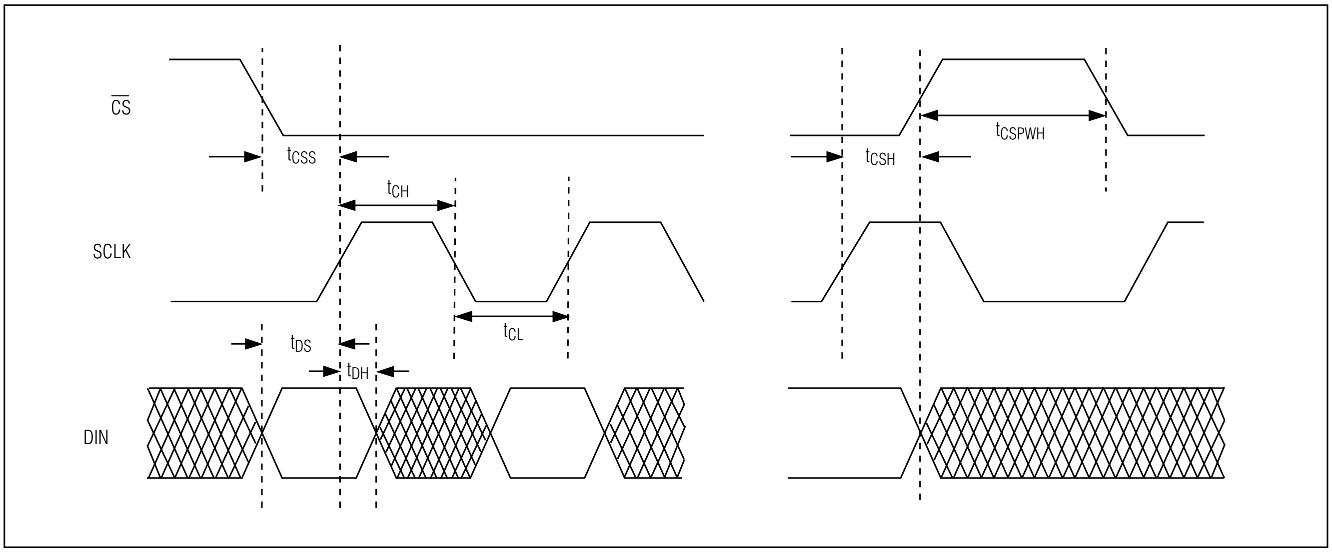


Figure 3. Detailed Serial-Interface Timing Diagram

Digital Inputs

The digital inputs are compatible with CMOS logic. Supply current increases slightly when toggling the logic inputs through the transition zone between $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.

Microprocessor Interfacing

The MAX5222 serial interface is compatible with MICROWIRE, SPI, and QSPI. For SPI, clear the CPOL and CPHA bits (CPOL = 0 and CPHA = 0). CPOL = 0 sets the inactive clock state to zero, and CPHA = 0 changes data at the falling edge of SCLK. This setting allows SPI to run at full clock speeds. If a serial port is not available on your µP, 3 bits of a parallel port can be used to emulate a serial port by bit manipulation. Minimize digital feedthrough at the voltage outputs by operating the serial clock only when necessary.

Table 4. Code Table

DAC CONTENTS								ANALOG OUTPUT
B7	B6	B5	B4	B3	B2	B1	B0	
1	1	1	1	1	1	1	1	$+REF \times \left(\frac{255}{256}\right)$
1	0	0	0	0	0	0	1	$+REF \times \left(\frac{129}{256}\right)$
1	0	0	0	0	0	0	0	$+REF \times \left(\frac{128}{256}\right) = +\frac{REF}{2}$
0	1	1	1	1	1	1	1	$+REF \times \left(\frac{127}{256}\right)$
0	0	0	0	0	0	0	1	$+REF \times \left(\frac{1}{256}\right)$
0	0	0	0	0	0	0	0	0V

Note:

$$1LSB = REF \times 2^{-8} = REF \times \left(\frac{1}{256}\right)$$

$$ANALOG\ OUTPUT = REF \times \left(\frac{D}{256}\right)$$ where D = decimal value of digital input

Applications Information

The MAX5222 is specified for single-supply operation with V_{DD} ranging from 2.7V to 5.5V, covering all commonly used supply voltages in 3V and 5V systems.

Initialization

An internal power-on reset circuit forces the outputs to zero scale and initializes all external registers to zero. This is equivalent to being in the shutdown state. Therefore, at power-up, perform an initial write operation to set the outputs to the desired voltage.

Power-Supply and Ground Management

GND should be connected to the highest quality ground available. Bypass V_{DD} with a 0.1µF to 0.22µF capacitor to GND. The reference input can be used without bypassing. For optimum line/load-transient response and noise performance, bypass the reference input with 0.1µF to 4.7µF to GND. Careful PC board layout minimizes crosstalk among DAC outputs, the reference, and digital inputs. Separate analog lines with ground traces between them. Make sure that high-frequency digital lines are not routed in parallel to analog lines.

Chip Information

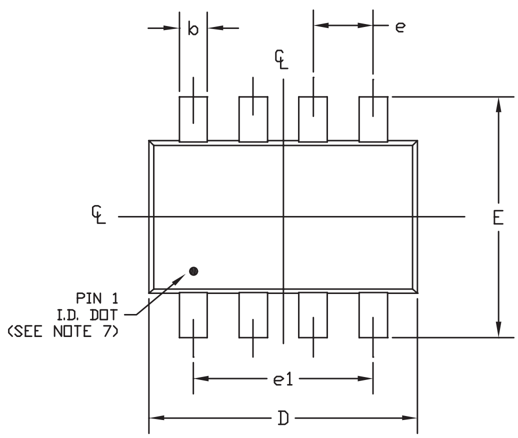
TRANSISTOR COUNT: 1480

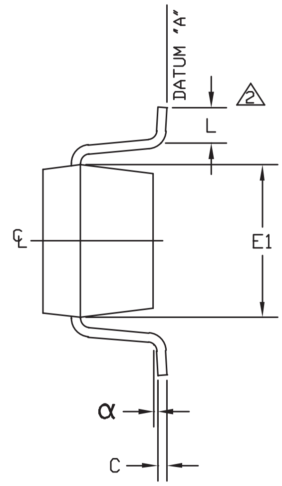
PROCESS TECHNOLOGY: BiCMOS

Dual, 8-Bit, Voltage-Output Serial DAC in 8-Pin SOT23

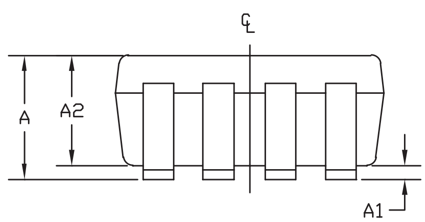
Package Information

SOT23, 8L.EPS





SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
α	0°	10°



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER" SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM ø MIN. LOCATED ABOVE PIN 1.

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, SOT 23, 8L
APPROVAL | DOCUMENT CONTROL NO. 21-0078 | REV B | 1/1

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