ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD} to GND	+20V
Time V_{IL} < $V_{IN\_}$ < V_{IH}	50ns
Input Voltage	V_{DD} + 0.3V to GND - 0.3V
Continuous Power Dissipation (T_A = +70°C)	
Plastic DIP (derate 9.09mW/°C above +70°C)	727mW
SO (derate 5.88mW/°C above +70°C)	471mW
CERDIP (derate 8.00mW/°C above +70°C)	640mW
Operating Temperature Ranges:	
MAX442_C_ _	0°C to +70°C
MAX442_E_ _	-40°C to +85°C
MAX442_MJA	-550°C to +125°C
Storage Temperature Range	-55°C to +160°C
Maximum Chip Temperature	+150°C
Lead Temperature (soldering, 10 sec)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

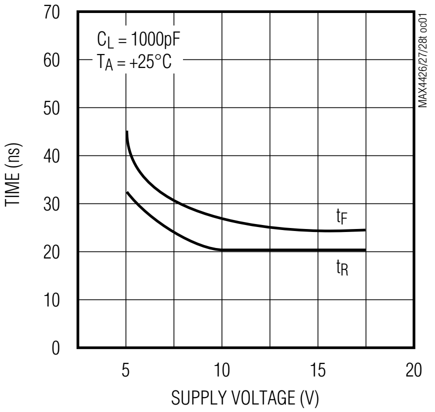
(V_{DD} = +4.5V to +18V, T_A = T_{MIN} to T_{MAX}, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Logic 1 Input Voltage	V_{IH}				2.4			V
Logic 0 Input Voltage	V_{IL}						0.8	V
Input Current	I_{IN}	V_{IN} = 0V to 18V			-1		1	µA
Output High Voltage	V_{OH}	No load			V_{DD} - 25			mV
Output Low Voltage	V_{OL}	No load					25	mV
Output Resistance	R_{OUT}	V_{DD} = 18V, I_{LOAD} = 10mA	V_{IN} = 0.8V for inverting stages, V_{IN} = 2.4V for noninverting stages	T_A = +25°C		4	10	Ω
				T_A = T_{MIN} to T_{MAX}		5	12	
			V_{IN} = 2.4V for inverting stages, V_{IN} = 0.8V for noninverting stages	T_A = +25°C		4	10	
				T_A = T_{MIN} to T_{MAX}		5	12	
Peak Output Current	I_{PK}	V_{DD} = 18V				1.5		A
Power-Supply Current	I_{SUPP}	V_{IN} = +3V for both inputs	T_A = +25°C			1.8	4.5	mA
			T_A = T_{MIN} to T_{MAX}			2.5	8.0	
		V_{IN} = 0V for both inputs	T_A = +25°C			0.2	0.4	
			T_A = T_{MIN} to T_{MAX}			0.3	0.6	
Rise Time (Note 1)	t_R	T_A = +25°C				20	30	ns
		T_A = T_{MIN} to T_{MAX}				25	40	
Fall Time (Note 1)	t_F	T_A = +25°C				20	30	ns
		T_A = T_{MIN} to T_{MAX}				25	40	
Delay Time (Note 1)	t_{D1}	T_A = +25°C				10	30	ns
		T_A = T_{MIN} to T_{MAX}				15	40	
	t_{D2}	T_A = +25°C				25	50	ns
		T_A = T_{MIN} to T_{MAX}				30	60	

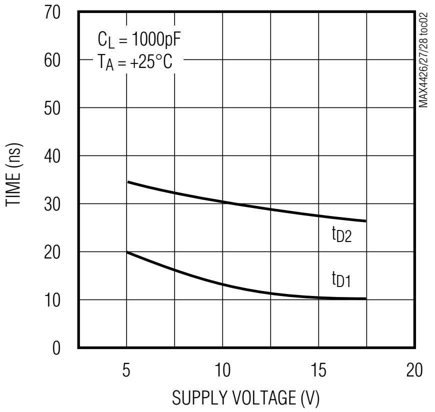
Note 1: Switching times guaranteed by design, not tested. See Figure 1 for timing measurement circuit.

Typical Operating Characteristics

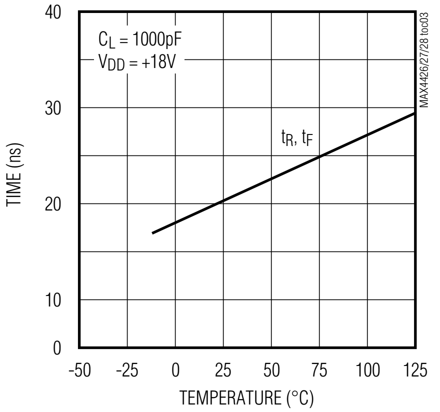
MAX4426 RISE AND FALL TIME vs. SUPPLY VOLTAGE



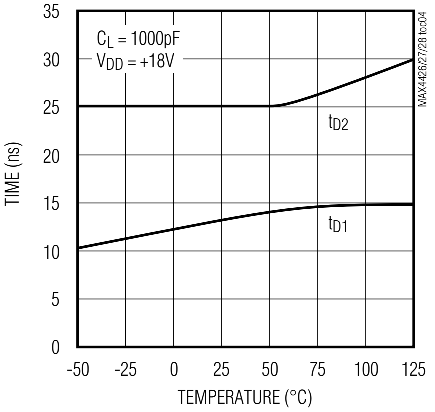
MAX4426 DELAY TIME vs. SUPPLY VOLTAGE



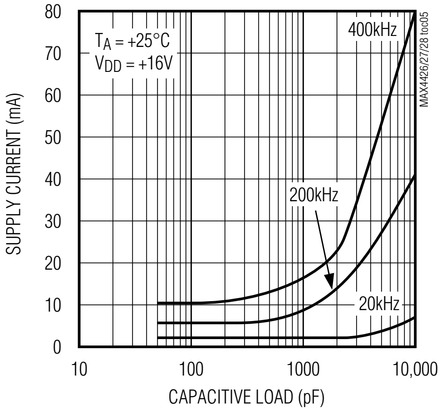
MAX4426 RISE AND FALL TIME vs. TEMPERATURE



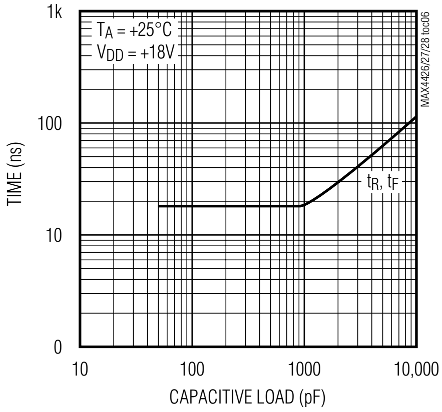
MAX4426 DELAY TIME vs. TEMPERATURE



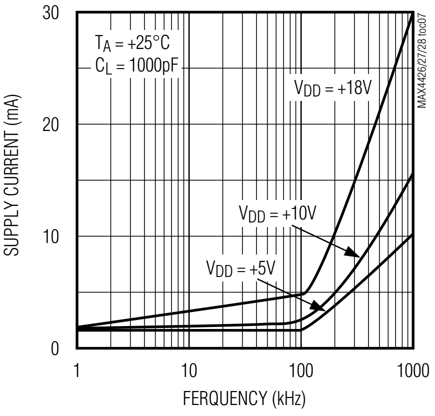
MAX4426 SUPPLY CURRENT vs. CAPACITIVE LOAD



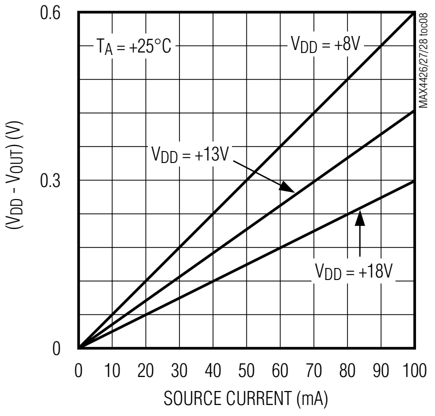
MAX4426 RISE AND FALL TIME vs. CAPACITIVE LOAD



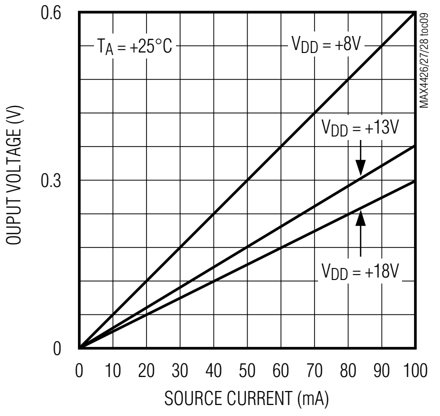
MAX4426 SUPPLY CURRENT vs. FREQUENCY



MAX4426 OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



MAX4426 OUTPUT LOW VOLTAGE vs. SOURCE CURRENT



Applications Information

The MAX4426/MAX4427/MAX4428 have easy-to-drive inputs. However, these inputs must never be allowed to stay between V_{IH} and V_{IL} for more than 50ns. Unused inputs should always be connected to ground to minimize supply current. Drivers can be paralleled on the MAX4426 or MAX4427 by tying both Inputs together and both outputs together.

Supply bypassing and grounding are extremely important with the MAX4426/MAX4427/MAX4428, as the peak supply current can be as high as 3A, which is twice the peak output current. Ground drops are a form of negative feedback with inverters, and hence will degrade the delay and transition time of the MAX4426/MAX4428.

Suggested bypass capacitors are a 4.7µF (low ESR) capacitor in parallel with a 0.1µF ceramic capacitor, mounted as close as possible to the MAX4426/MAX4427/MAX4428. Use a ground plane if possible or separate ground returns for inputs and outputs. Output voltage ringing can be minimized with a 5Ω to 20Ω resistor in series with the output, but this will degrade output transition time. Ringing may be undesirable due to the large current that flows through capacitive loads when the voltage across these loads transitions quickly.

Operation at the upper end of the supply voltage range (> 15V) requires that a capacitance of at least 50pF be present at the outputs. This prevents the supply voltage provided to the die (which can be different from that seen at the supply pin) from exceeding the 20V absolute maximum rating, due to overshoot. Since at least 50pF of gate capacitance is present in all higher power FETs, this requirement is easily met.

Power Dissipation

The MAX4426/MAX4427/MAX4428 power dissipation consists of input inverter losses, crowbar current through the output devices, and output current (either capacitive or resistive). The sum of these must be kept below the maximum power dissipation limit.

The DC input inverter supply current is 0.2mA when both inputs are low and 2mA when both inputs are high. The crowbar current through an output device making a transition is approximately 100mA for a few nanoseconds. This is a small portion of the total supply current, except for high switching frequencies or a small load capacitance (100pF).

The MAX4426/MAX4427/MAX4428 power dissipation when driving a ground-referenced resistive load is:

$$P = (D)\ (r_{ON(MAX)})\ (I_{LOAD}^2)$$

where D is the percentage of time the MAX4426/MAX4427/MAX4428 output pulls high, $r_{ON(MAX)}$ is the MAX4426/MAX4427/MAX4428 maximum on resistance, and I_{LOAD} is the MAX4426/MAX4427/MAX4428 load current.

For capacitive loads. the power dissipation is:

$$P = (C_{LOAD})\ (V_{DD}^2)\ (FREQ)$$

where C_{LOAD} is the capacitive load. V_{DD} is the MAX4426/MAX4427/MAX4428 supply voltage, and FREQ is the toggle frequency.

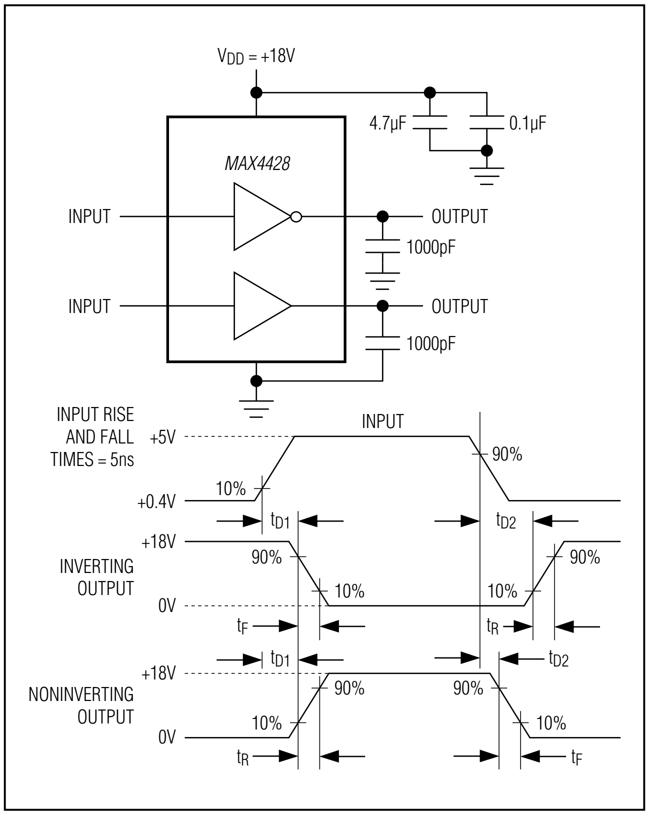


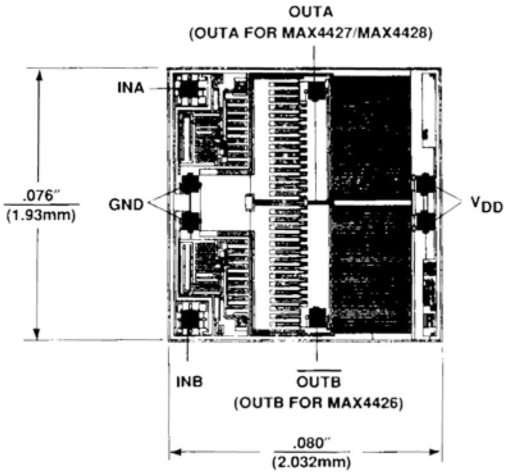
Figure 1. Inverting and Noninverting Test Circuit

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX4427CPA	0°C to +70°C	8 Plastic DIP
MAX4427CSA	0°C to +70°C	8 SO
MAX4427C/D	0°C to +70°C	Dice*
MAX4427EPA	-40°C to +85°C	8 Plastic DIP
MAX4427ESA	-40°C to +85°C	8 SO
MAX4427EJA	-40°C to +85°C	8 CERDIP
MAX4427MJA	-55°C to +125°C	8 CERDIP**
MAX4428CPA	0°C to +70°C	8 Plastic DIP
MAX4428CSA	0°C to +70°C	8 SO
MAX4428C/D	0°C to +70°C	Dice*
MAX4428EPA	-40°C to +85°C	8 Plastic DIP
MAX4428ESA	-40°C to +85°C	8 SO
MAX4428EJA	-40°C to +85°C	8 CERDIP
MAX4428MJA	-55°C to +125°C	8 CERDIP**

*Dice are tested at T_A = +25°C.
**Contact factory for availability and processing to MIL-STD-883.

Chip Topography

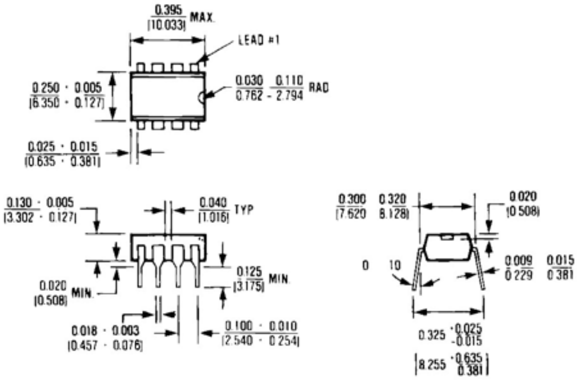


SUBSTRATE CONNECTED TO V_{DD};
TRANSISTOR COUNT: 26.

MAX4427/MAX4428

Package Information

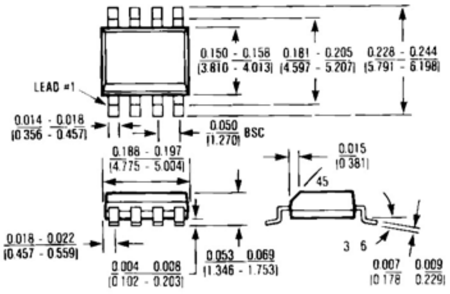
(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



8 Lead Plastic DIP

θ_{JA} = 120°C/W

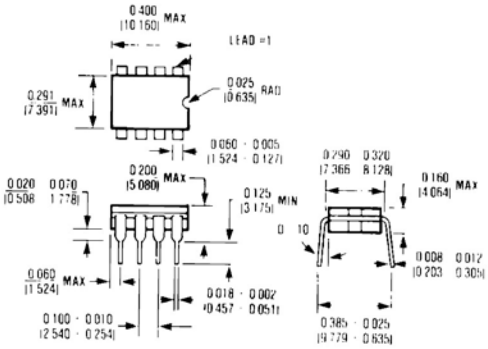
θ_{JC} = 70°C/W



8 Lead Small Outline

θ_{JA} = 170°C/W

θ_{JC} = 80°C/W



8 Lead CERDIP

θ_{JA} = 125°C/W

θ_{JC} = 55°C/W

Dual High-Speed 1.5A MOSFET Drivers

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
2	6/06	To clarify and illuminate an input logic level restriction	—