

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} - V_{EE}) 7.5V
 IN+, IN-, $\overline{SHDN}$ Voltage ($V_{CC} + 0.3V$) to ($V_{EE} - 0.3V$)
 Output Short-Circuit Duration (Note 1) Continuous
 (short to either supply)
 Continuous Power Dissipation ($T_A = +70^\circ C$)
 5-pin SOT23-5 (derate 7.1mW/ $^\circ C$ above $+70^\circ C$) 571mW
 8-pin SO (derate 5.88mW/ $^\circ C$ above $+70^\circ C$) 471mW
 8-pin μ MAX (derate 4.10mW/ $^\circ C$ above $+70^\circ C$) 330mW
 14-pin SO (derate 8.00mW/ $^\circ C$ above $+70^\circ C$) 640mW

Operating Temperature Range
 MAX412_E_ $-40^\circ C$ to $+85^\circ C$
 Maximum Junction Temperature $+150^\circ C$
 Storage Temperature Range $-65^\circ C$ to $+160^\circ C$
 Lead Temperature (soldering, 10sec) $+300^\circ C$

Note 1: Provided that the maximum package power-dissipation rating is met.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	$V_{CM} = V_{EE}$ to V_{CC}	MAX4123ESA/MAX4125ESA		± 0.20	± 0.60	mV
		MAX4122EUK/MAX4124EUK		± 0.35	± 1.50	
		MAX4123EUA/MAX4125EUA		± 0.35	± 1.20	
		MAX4126ESA/MAX4127ESD/MAX4128ESA		± 0.25	± 0.75	
		MAX4126EUA/MAX4128EUA		± 0.40	± 1.50	
		MAX4129ESD		± 0.35	± 1.50	
Input Bias Current	$V_{CM} = V_{EE}$ to V_{CC}			± 50	± 150	nA
Input Offset Current	$V_{CM} = V_{EE}$ to V_{CC}			± 1	± 12	nA
Differential Input Resistance	$-1.5V < V_{DIFF} < 1.5V$			500		k Ω
Common-Mode Input Voltage Range			$V_{EE} - 0.25$		$V_{CC} + 0.25$	V
Common-Mode Rejection Ratio	$(V_{EE} - 0.25) < V_{CM} < (V_{CC} + 0.25V)$	MAX4123ESA/MAX4125ESA	78	98		dB
		MAX4122EUK/MAX4124EUK	67	90		
		MAX4123EUA/MAX4125EUA	68	88		
		MAX4126ESA/MAX4127ESD/MAX4128ESA	74	94		
		MAX4126EUA/MAX4128EUA	66	86		
		MAX4129ESD	64	84		
Power-Supply Rejection Ratio	$V_{CC} = 2.7V$ to $6.5V$		78	100		dB
Output Resistance	$A_V = 1$			0.1		Ω
Off-Leakage Current	$\overline{SHDN} < 0.8V$, $V_{OUT} = 0V$ to V_{CC}			± 0.1	± 1	μA
Large-Signal Voltage Gain	$V_{CC} = 2.7V$	$V_{OUT} = 0.25V$ to $2.45V$, $R_L = 100k\Omega$	92	104		dB
		$V_{OUT} = 0.4V$ to $2.3V$, $R_L = 250\Omega$	72	80		
	$V_{CC} = 5V$	$V_{OUT} = 0.25V$ to $4.75V$, $R_L = 100k\Omega$	94	106		
		$V_{OUT} = 0.4V$ to $4.6V$, $R_L = 250\Omega$	75	84		

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage Swing	MAX4122/ MAX4123/ MAX4124/ MAX4125	R _L = 100kΩ	V _{CC} - V _{OH}	12	20	mV	
			V _{OL} - V _{EE}	20	35		
	R _L = 250Ω	V _{CC} - V _{OH}	240	290			
		V _{OL} - V _{EE}	125	170			
	MAX4126/ MAX4127/ MAX4128/ MAX4129	R _L = 100kΩ	V _{CC} - V _{OH}	15	30		
			V _{OL} - V _{EE}	25	40		
	R _L = 250Ω	V _{CC} - V _{OH}	280	330			
		V _{OL} - V _{EE}	180	230			
Output Short-Circuit Current				50		mA	
$\overline{\text{SHDN}}$ Logic Threshold	MAX4123/MAX4125/MAX4127		Low	0.8		V	
			High	2.0			
$\overline{\text{SHDN}}$ Input Current	MAX4123/MAX4125/MAX4127			±1	±3	μA	
Operating Supply-Voltage Range				2.7	6.5	V	
Supply Current per Amplifier	V _{CM} = V _{OUT} = V _{CC} /2		V _{CC} = 2.7V	650	750	μA	
			V _{CC} = 5V	725	825		
Shutdown Supply Current per Amplifier	$\overline{\text{SHDN}}$ > 0.8V, MAX4123/MAX4125/MAX4127		V _{CC} = 2.7V	25	40	μA	
			V _{CC} = 5V	40	60		

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V _{CM} = V _{EE} to V _{CC}	MAX4123ESA/MAX4125ESA			±0.75	mV
		MAX4122EUK/MAX4124EUK			±3.50	
		MAX4123EUA/MAX4125EUA			±4.40	
		MAX4126ESA/MAX4127ESD/MAX4128ESA			±0.95	
		MAX4126EUA/MAX4128EUA			±4.70	
		MAX4129ESD			±4.00	
Input Offset Voltage Tempco				±2		µV/°C
Input Bias Current	V _{CM} = V _{EE} to V _{CC}				±160	nA
Input Offset Current	V _{CM} = V _{EE} to V _{CC}				±18	nA
Common-Mode Input Voltage Range			V _{EE} - 0.20		V _{CC} + 0.20	V
Common-Mode Rejection Ratio	(V _{EE} - 0.2V) < V _{CM} < (V _{CC} + 0.2V)	MAX4123ESA/MAX4125ESA	76			dB
		MAX4122EUK/MAX4124EUK	62			
		MAX4123EUA/MAX4125EUA	60			
		MAX4126ESA/MAX4127ESD/MAX4128ESA	74			
		MAX4126EUA/MAX4128EUA	58			
		MAX4129ESD	60			

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DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $V_{CM} = 0V$, $V_{OUT} = V_{CC}/2$, R_L tied to $V_{CC}/2$, $\overline{SHDN} \geq 2V$ (or open), $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	V _{CC} = 2.7V to 6.5V			74			dB
Off-Leakage Current	SHDN $\overline{}$ < 0.8V, V _{OUT} = 0V to V _{CC}					±12	μA
Large-Signal Voltage Gain	V _{CC} = 2.7V	V _{OUT} = 0.25V to 2.45V, R _L = 100kΩ		84			dB
		V _{OUT} = 0.4V to 2.3V, R _L = 250Ω		66			
	V _{CC} = 5V	V _{OUT} = 0.25V to 4.75V, R _L = 100kΩ		86			
		V _{OUT} = 0.4V to 4.6V, R _L = 250Ω		68			
Output Voltage Swing	MAX4122/ MAX4123/ MAX4124/ MAX4125	R _L = 100kΩ	V _{CC} - V _{OH}			25	mV
			V _{OL} - V _{EE}			40	
		R _L = 250Ω	V _{CC} - V _{OH}			300	
			V _{OL} - V _{EE}			190	
	MAX4126/ MAX4127/ MAX4128/ MAX4129	R _L = 100kΩ	V _{CC} - V _{OH}			35	
			V _{OL} - V _{EE}			50	
		R _L = 250Ω	V _{CC} - V _{OH}			350	
			V _{OL} - V _{EE}			250	
SHDN Logic Threshold	MAX4123/MAX4125/MAX4127		Low			0.8	V
			High	2.0			
SHDN Input Current	MAX4123/MAX4125/MAX4127					±3	μA
Operating Supply-Voltage Range				2.7		6.5	V
Supply Current per Amplifier	V _{CM} = V _{OUT} = V _{CC} /2		V _{CC} = 2.7V			775	μA
			V _{CC} = 5V			850	
Shutdown Supply Current per Amplifier	SHDN $\overline{}$ < 0.8V, MAX4123/MAX4125/MAX4127		V _{CC} = 2.7V			50	μA
			V _{CC} = 5V			70	

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $\overline{SHDN} \geq 2V$ (or open), $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	MAX4122/23/26/27/29		5		MHz
	MAX4124/25/28 ($A_V \geq 10$)		25		
Phase Margin	MAX4122/23/26/27/29		64		degrees
	MAX4124/25/28 ($A_V \geq 10$)		60		
Gain Margin	MAX4122/23/26/27/29		12		dB
	MAX4124/25/28 ($A_V \geq 10$)		10		
Total Harmonic Distortion	$f = 10kHz$, $V_{OUT} = 2V_{p-p}$, MAX4122/23/26/27/29 ($A_V = 1$)		0.003		%
Slew Rate	MAX4122/23/26/27/29		2		V/ μs
	MAX4124/25/28 ($A_V \geq 10$)		10		
Settling Time to 0.01%	MAX4122/23/26/27/29 ($A_V = 1$), $V_{OUT} = 2V$ step		2.0		μs
	MAX4124/25/28 ($A_V \geq 10$), $V_{OUT} = 2V$ step		1.3		
Turn-On Time	$V_{CC} = 0V$ to $3V$ step, $V_{OUT} = V_{CC}/2$		1		μs

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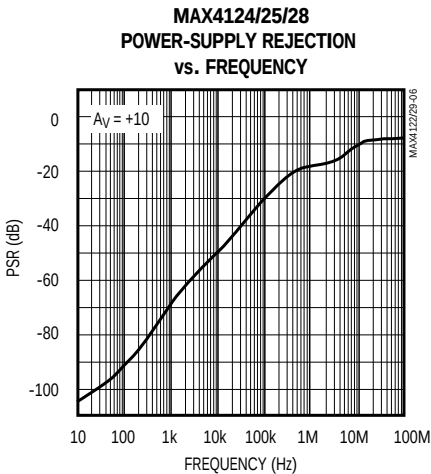
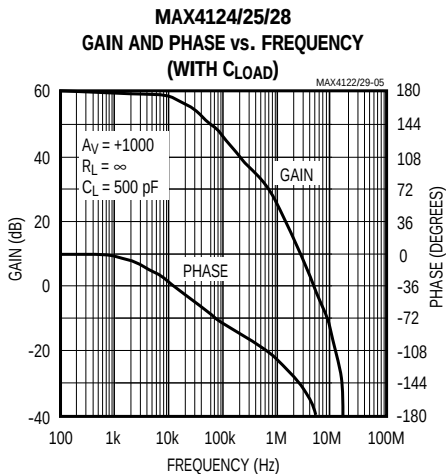
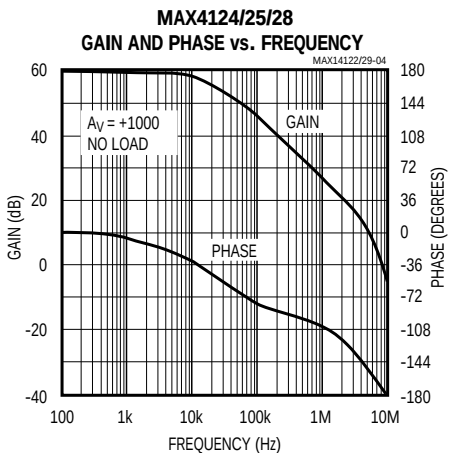
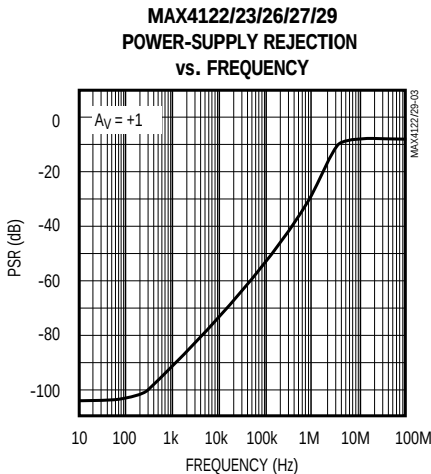
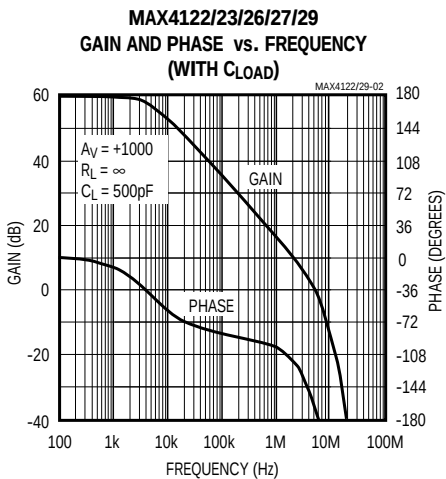
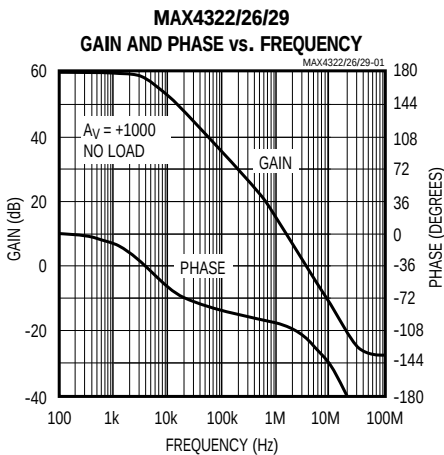
AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +2.7V$ to $+6.5V$, $V_{EE} = 0V$, $\overline{SHDN} \geq 2V$ (or open), $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Delay	$V_{CC} = 3V$, $V_{OUT} = V_{CC}/2$, MAX4123/25/27	Enable		1	μs
		Disable		0.2	
Input Capacitance			3		pF
Input Noise Voltage Density	$f = 1kHz$		22		$nV/\sqrt{Hz}$
Input Noise Current Density	$f = 1kHz$		0.4		$pA/\sqrt{Hz}$
Amp-Amp Isolation	MAX4126/27/28/29		135		dB
Capacitive Load Stability	MAX4122/23/26/27/29 ($A_V = 1$)		500		pF
	MAX4124/25/28 ($A_V \geq 10$)		500		

Typical Operating Characteristics

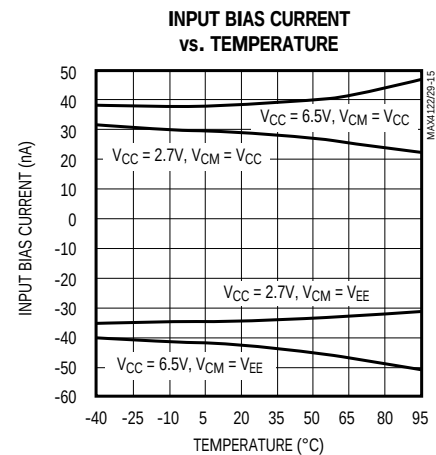
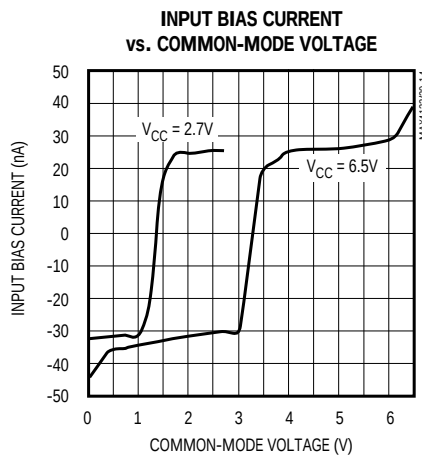
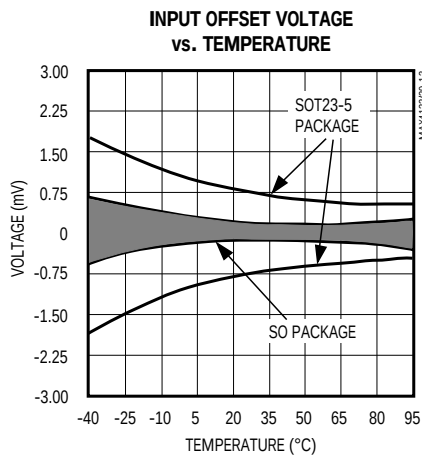
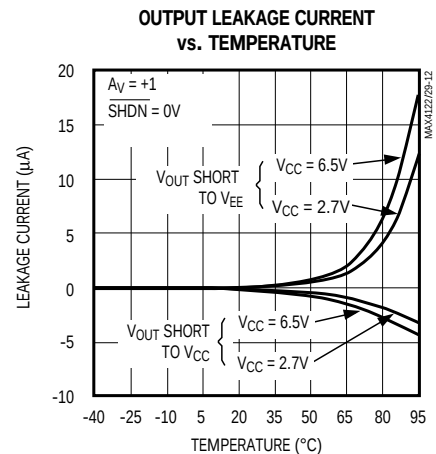
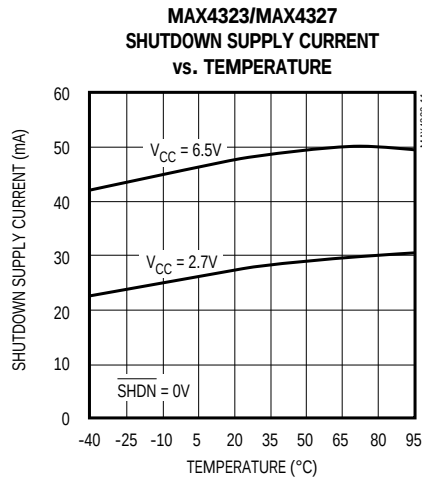
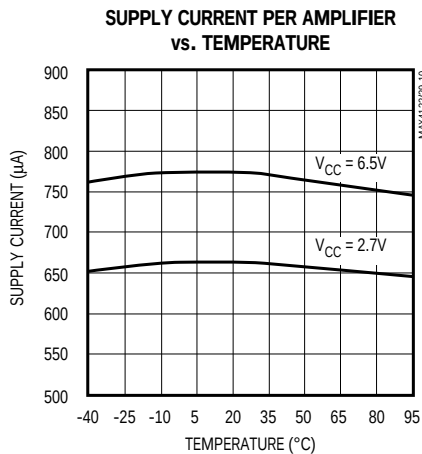
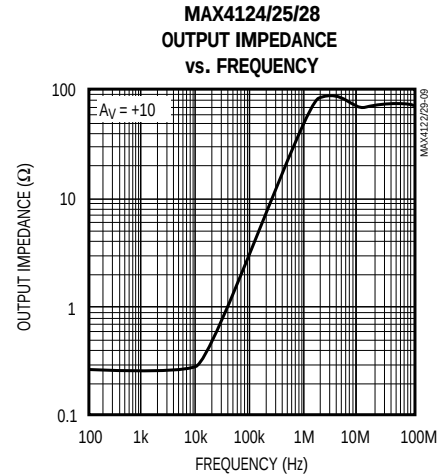
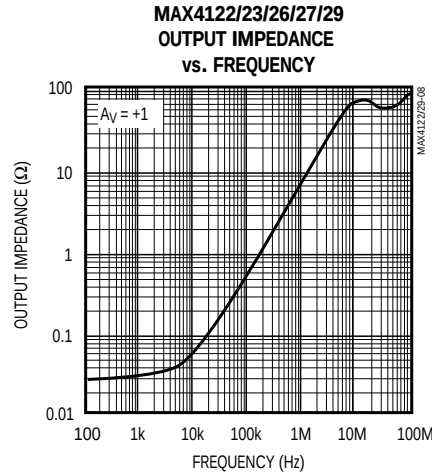
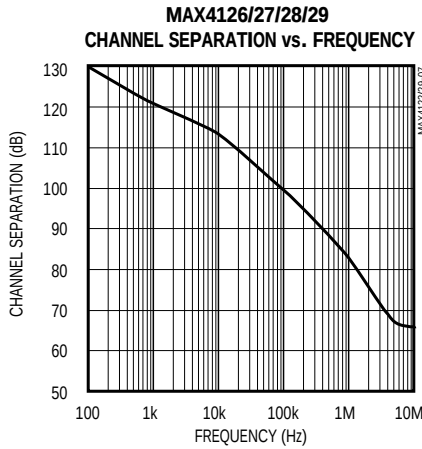
($V_{CC} = +5V$, $V_{EE} = 0V$, $V_{CM} = V_{CC}/2$, $T_A = +25^\circ C$, unless otherwise noted.)



Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

Typical Operating Characteristics (continued)

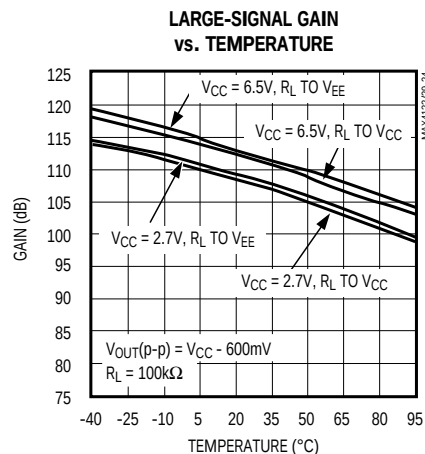
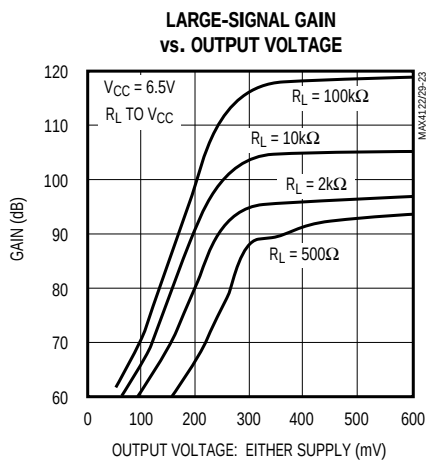
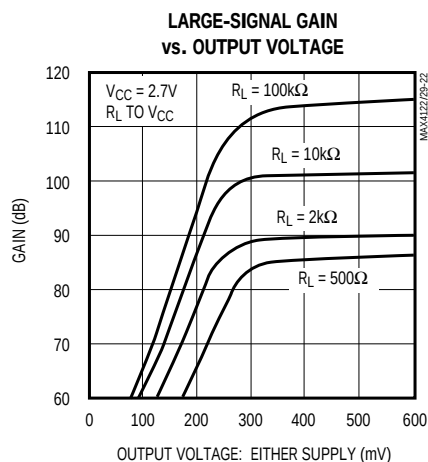
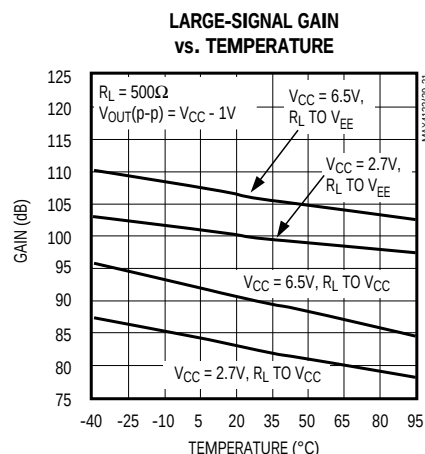
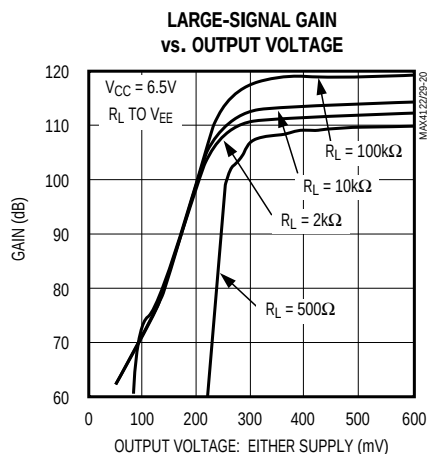
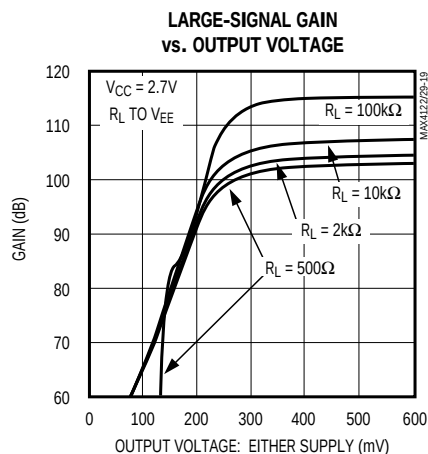
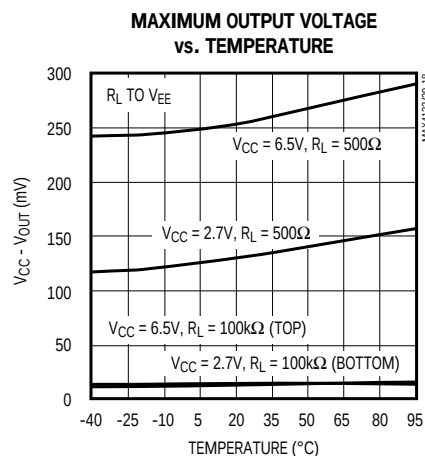
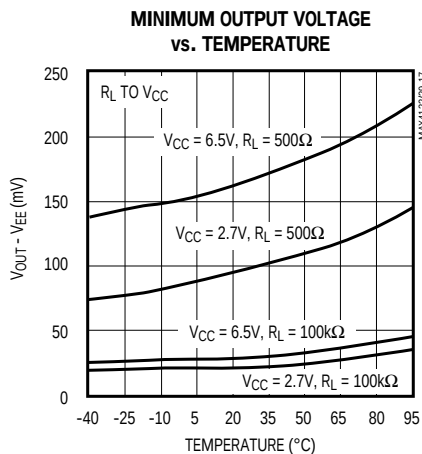
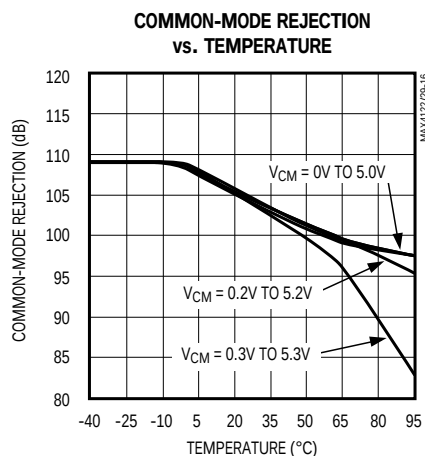
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Typical Operating Characteristics (continued)

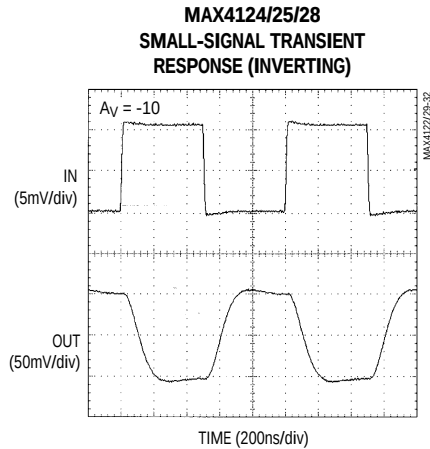
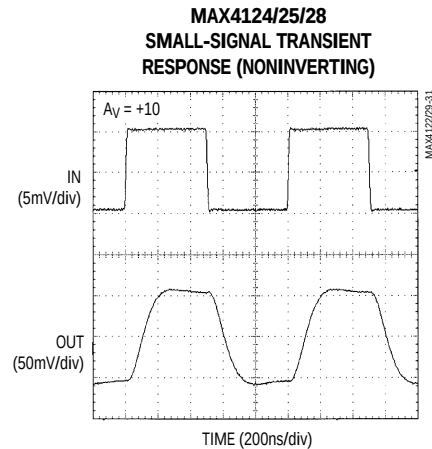
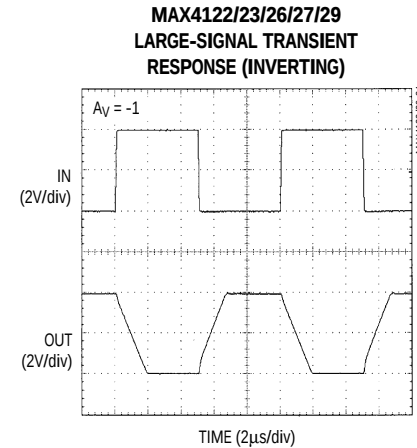
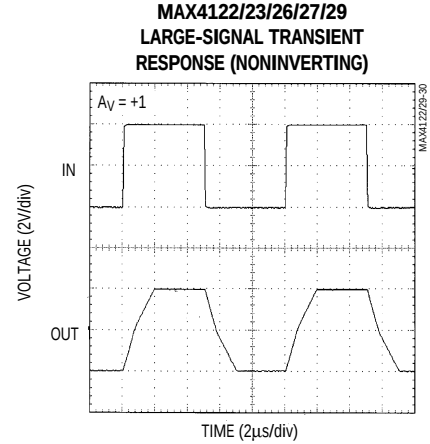
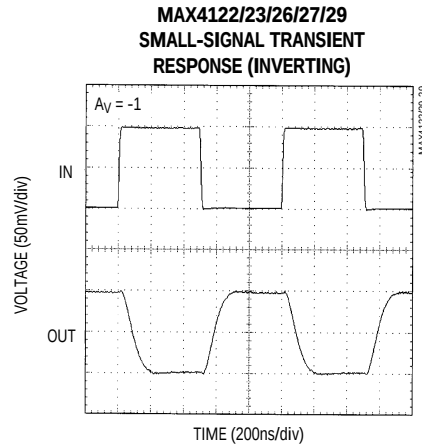
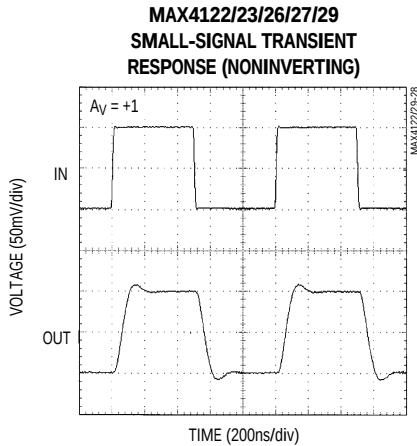
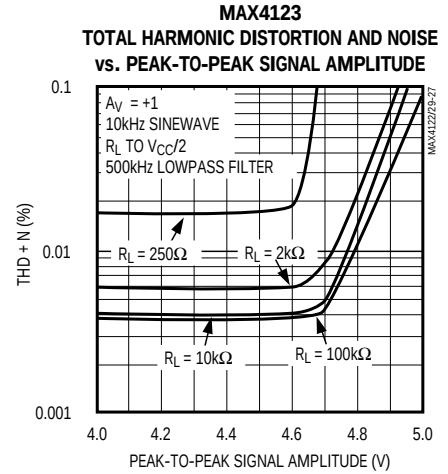
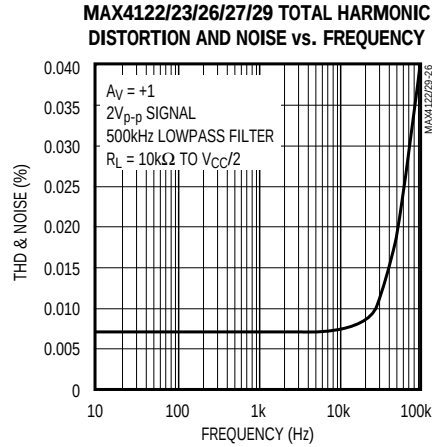
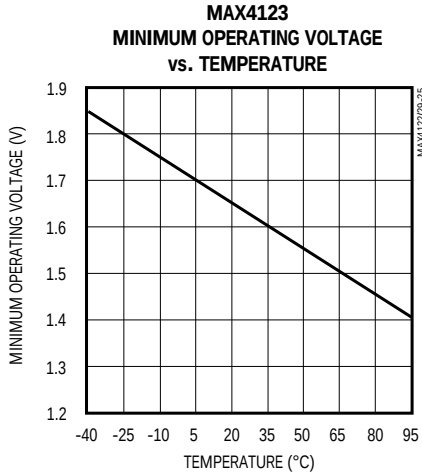
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Typical Operating Characteristics (continued)

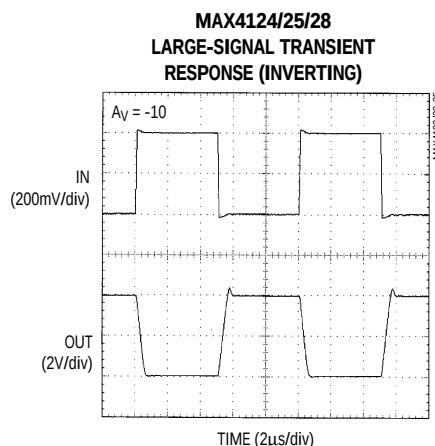
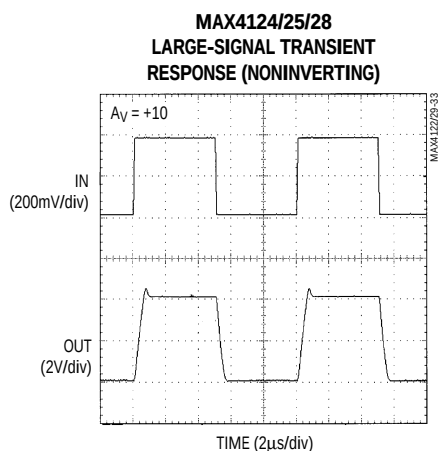
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Typical Operating Characteristics (continued)

($V_{CC} = +5V$, $V_{EE} = 0V$, $V_{CM} = V_{CC}/2$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN					NAME	FUNCTION
MAX4122 MAX4124	MAX4123 MAX4125	MAX4126 MAX4128	MAX4127	MAX4129		
1	6	—	—	—	OUT	Output
2	4	4	4	11	V_{EE}	Negative Supply. Ground for single-supply operation.
3	3	—	—	—	IN+	Noninverting Input
4	2	—	—	—	IN-	Inverting Input
5	7	8	14	4	V_{CC}	Positive Supply
—	1, 5	—	5, 7, 8, 10	—	N.C.	No Connect
—	8	—	—	—	$\overline{SHDN}$	Shutdown Control. Tie high or leave floating to enable amplifier.
—	—	1, 7	1, 13	1, 7	OUT1, OUT2	Outputs for Amps 1 and 2
—	—	2, 6	2, 12	2, 6	IN1-, IN2-	Inverting Inputs for Amps 1 and 2
—	—	3, 5	3, 11	3, 5	IN1+, IN2+	Noninverting Inputs for Amps 1 and 2
—	—	—	6, 9	—	$\overline{SHDN1}$, $\overline{SHDN2}$	Shutdown Control for Amps 1 and 2. Tie high or leave floating to enable amplifier.
—	—	—	—	8, 14	OUT3, OUT4	Outputs for Amps 3 and 4
—	—	—	—	9, 13	IN3-, IN4-	Inverting Inputs for Amps 3 and 4
—	—	—	—	10, 12	IN3+, IN4+	Noninverting Inputs for Amps 3 and 4

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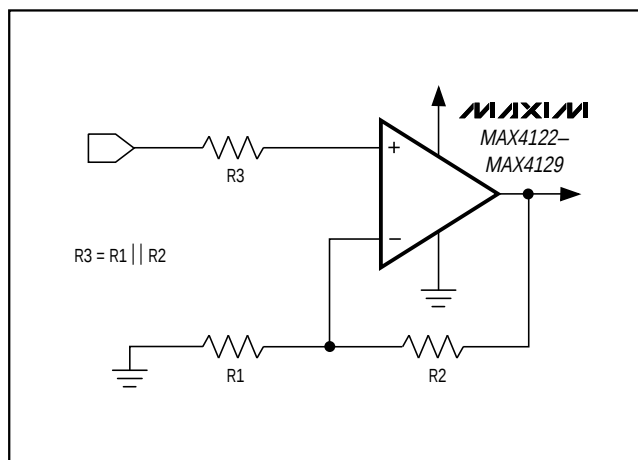


Figure 1a. Reducing Offset Error Due to Bias Current (Noninverting)

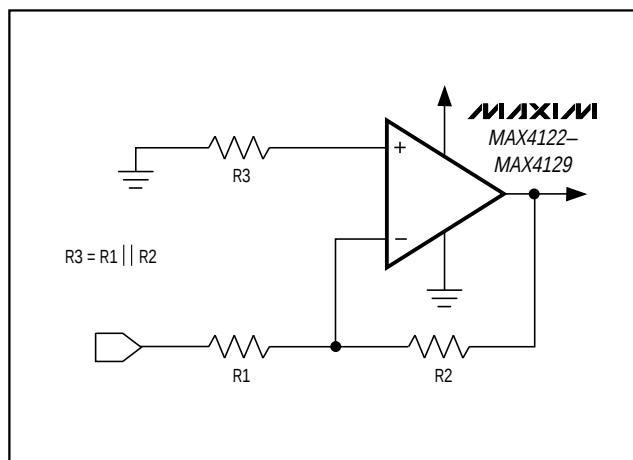


Figure 1b. Reducing Offset Error Due to Bias Current (Inverting)

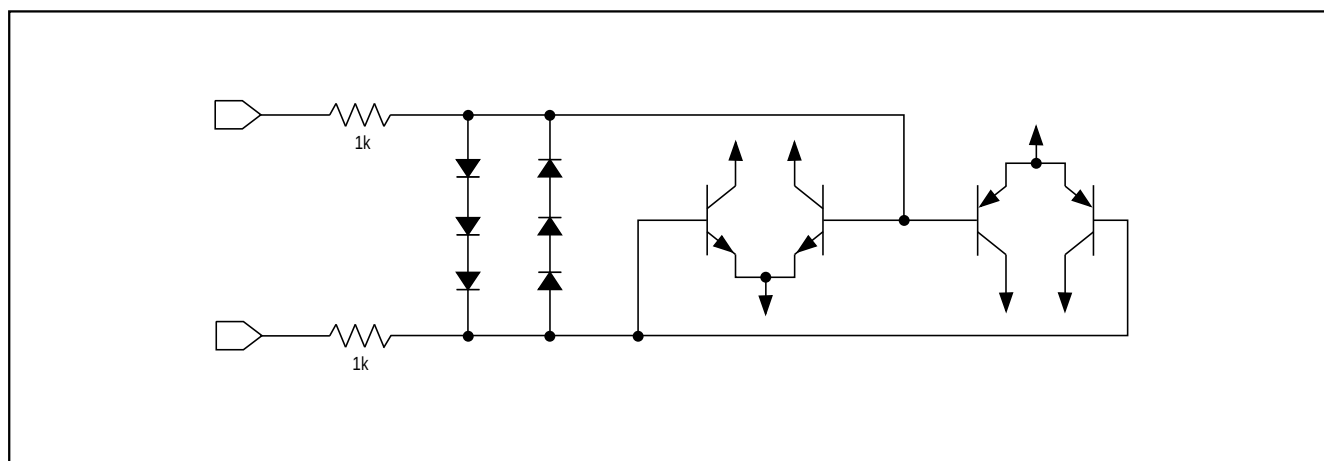


Figure 2. Input Protection Circuit

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

Applications Information

Rail-to-Rail Input Stage

Devices in the MAX4122–MAX4129 family of high-speed amplifiers have rail-to-rail input and output stages designed for low-voltage single-supply operation. The input stage consists of separate NPN and PNP differential stages, which combine to provide an input common-mode range extending 0.2V beyond the supply rails. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages near the positive rail. The input offset voltage is typically below 200μV. The switchover transition region, which occurs near $V_{CC}/2$, has been extended to minimize the slight degradation in CMRR caused by the mismatch of the input pairs. Their low offset voltage, high bandwidth, and rail-to-rail common-mode range make these op amps excellent choices for precision low-voltage data-acquisition systems.

Since the input stage switches between the NPN and PNP pairs, the input bias current changes polarity as the input voltage passes through the transition region. To reduce the offset error caused by input bias currents flowing through external source impedances, match the effective impedance seen by each input (Figures 1a, 1b). High source impedances, together with the input capacitance, can create a parasitic pole that produces an underdamped signal response. Reducing the input impedance or placing a small (2pF to 10pF) capacitor across the feedback resistor improves the response.

The MAX4122–MAX4129's inputs are protected from large differential input voltages by 1kΩ series resistors and back-to-back triple diodes across the inputs (Figure 2). For differential input voltages less than 1.8V the input resistance is typically 500kΩ. For differential input voltages greater than 1.8V the input resistance is approximately 2kΩ, and the input bias current is determined by the following equation:

$$I_{BIAS} = \frac{V_{DIFF} - 1.8V}{2k\Omega}$$

Rail-to-Rail Output Stage

The minimum output voltage will be within millivolts of ground for single-supply operation where the load is referenced to ground (V_{EE}). Figure 3 shows the input voltage range and output voltage swing of a MAX4123 connected as a voltage follower. With a +3V supply and the load tied to ground, the output swings from

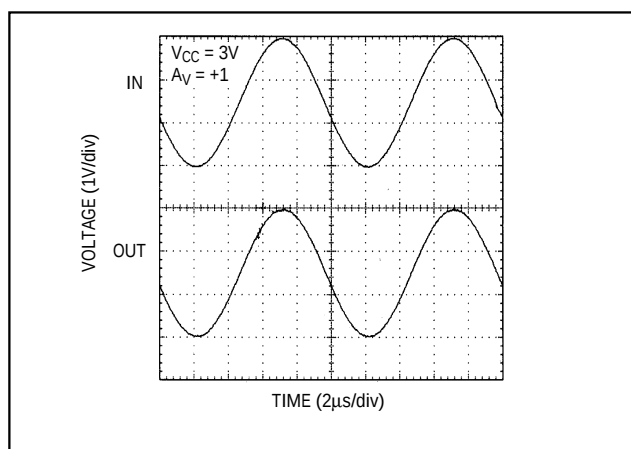


Figure 3. Rail-to-Rail Input /Output Voltage Range

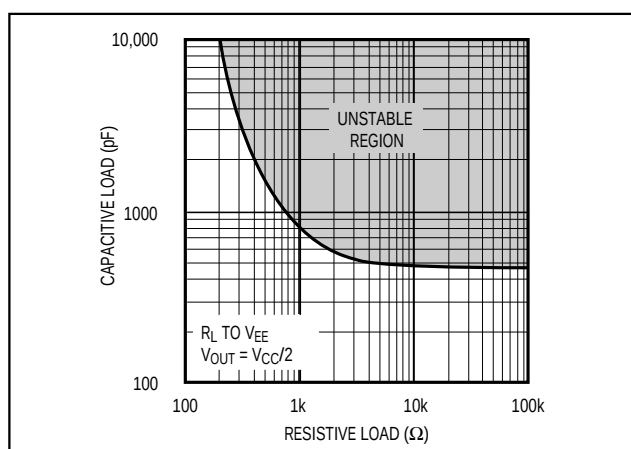


Figure 4. Capacitive-Load Stability

0.00V to 2.90V. The maximum output voltage swing depends on the load, but will be within 150mV of a +3V supply, even with the maximum load (500Ω to ground).

Driving a capacitive load can cause instability in most high-speed op amps, especially those with low quiescent current. The MAX4122–MAX4129 have a high tolerance for capacitive loads. They are stable with capacitive loads up to 500pF. Figure 4 gives the stable operating region for capacitive loads. Figures 5–8 show the response with capacitive loads, and the results of adding an isolation resistor in series with the output (Figure 9). The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

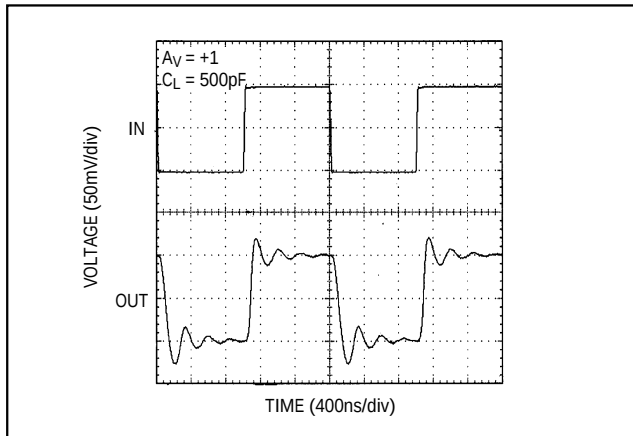


Figure 5. MAX4122/23/26/27/29 Small-Signal Transient Response with Capacitive Load

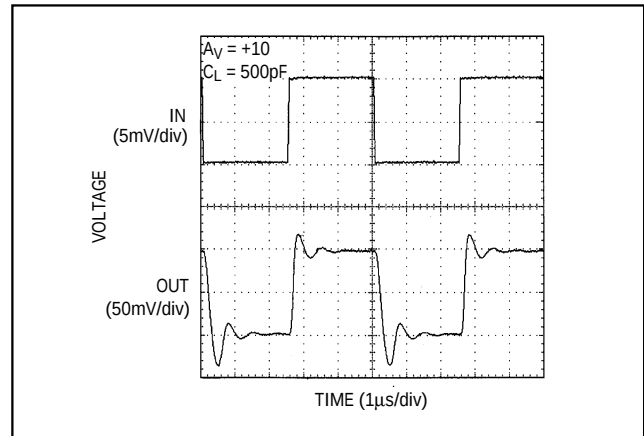


Figure 6. MAX4124/25/28 Small-Signal Transient Response with Capacitive Load

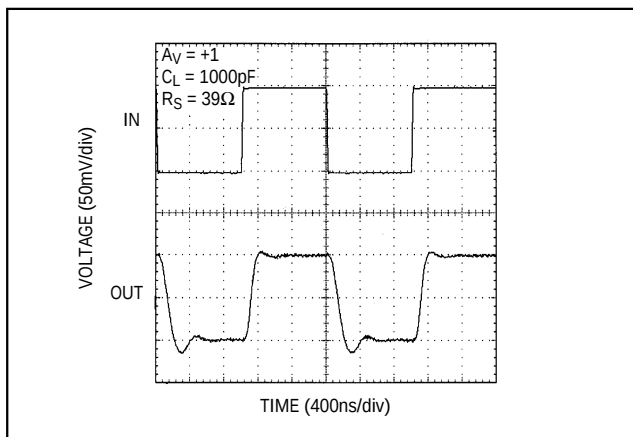


Figure 7. MAX4122/23/26/27/29 Transient Response to Capacitive Load with Isolation Resistor

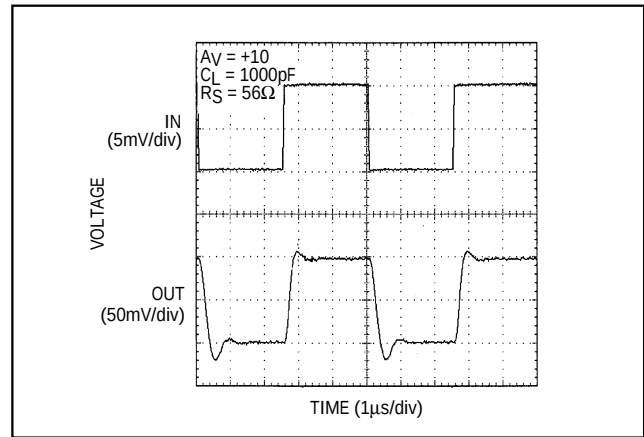


Figure 8. MAX4124/25/28 Transient Response to Capacitive Load with Isolation Resistor

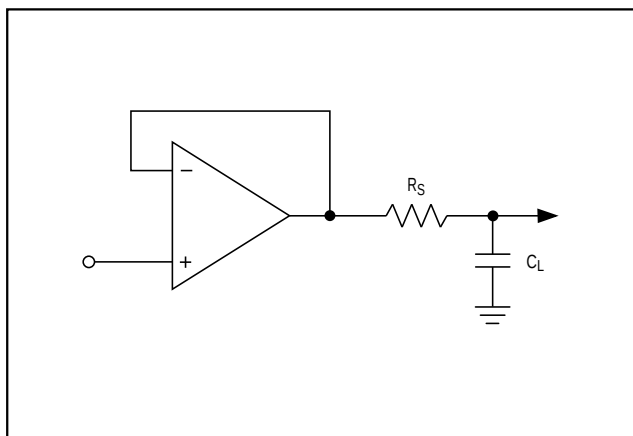


Figure 9. Capacitive-Load-Driving Circuit

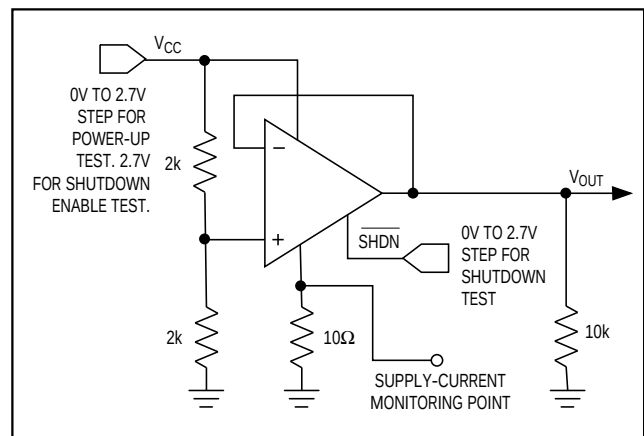


Figure 10. Power-Up/Shutdown Test Circuit

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

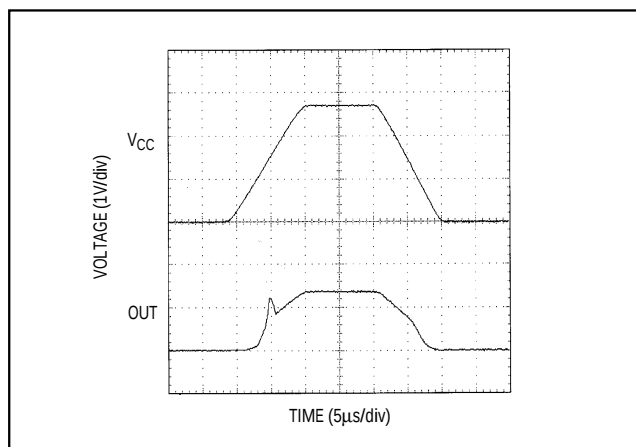


Figure 11. Power-Up Output Voltage

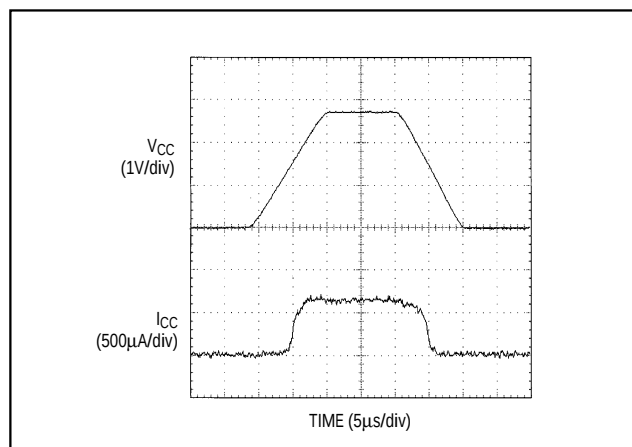


Figure 12. Power-Up Supply Current

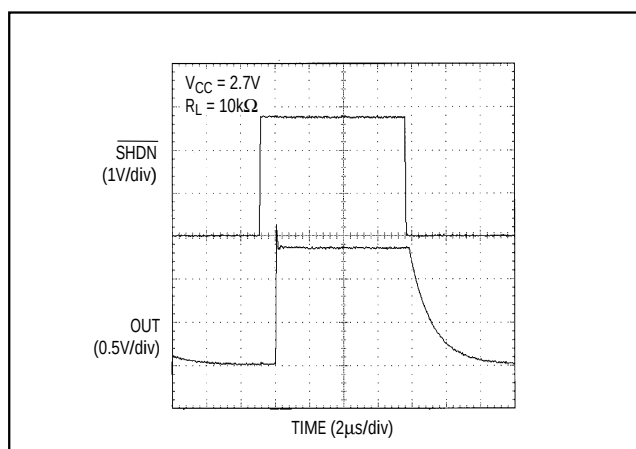


Figure 13. Shutdown Output Voltage

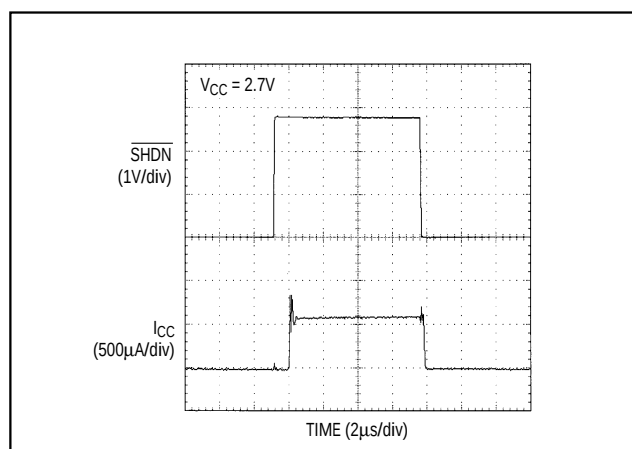


Figure 14. Shutdown Enable/Disable Supply Current

Power-Up and Shutdown Mode

The MAX4122-MAX4129 amplifiers typically settle within 1μs after power-up. Using the test circuit of Figure 10, Figures 11 and 12 show the output voltage and supply current on power-up.

The MAX4123, MAX4125, and MAX4127 have a shutdown option. When the shutdown pin ($\overline{\text{SHDN}}$) is pulled low, the supply current drops below 25μA per amplifier and the amplifiers are disabled with the outputs in a high-impedance state. Pulling $\overline{\text{SHDN}}$ high or leaving it floating enables the amplifier. In the dual-amplifier MAX4129, the shutdown functions operate independently. Figures 13 and 14 show the output voltage and supply current responses of the MAX4123 to a shutdown pulse.

Power Supplies and Layout

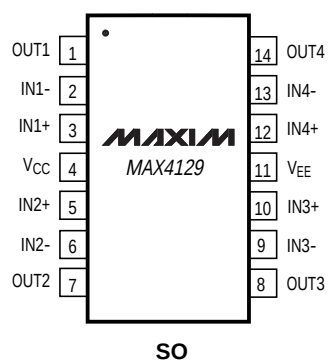
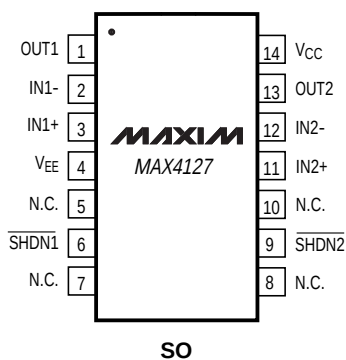
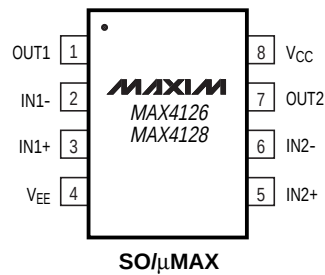
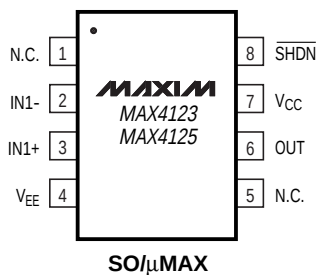
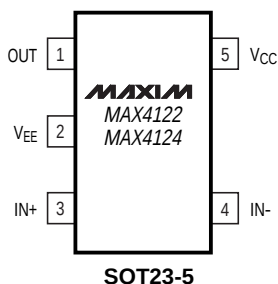
The MAX4122-MAX4129 operate from a single +2.7V to +6.5V power supply, or from dual supplies of ±1.35V to ±3.25V. For single-supply operation, bypass the power supply with a 0.1μF ceramic capacitor in parallel with at least 1μF. For dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths and resistor leads by placing external components close to the op amp's pins.

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

Pin Configurations

TOP VIEW



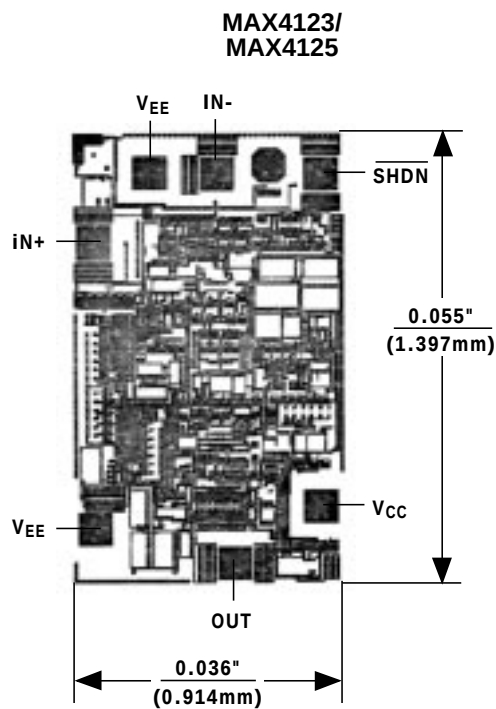
Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

Ordering Information (continued)

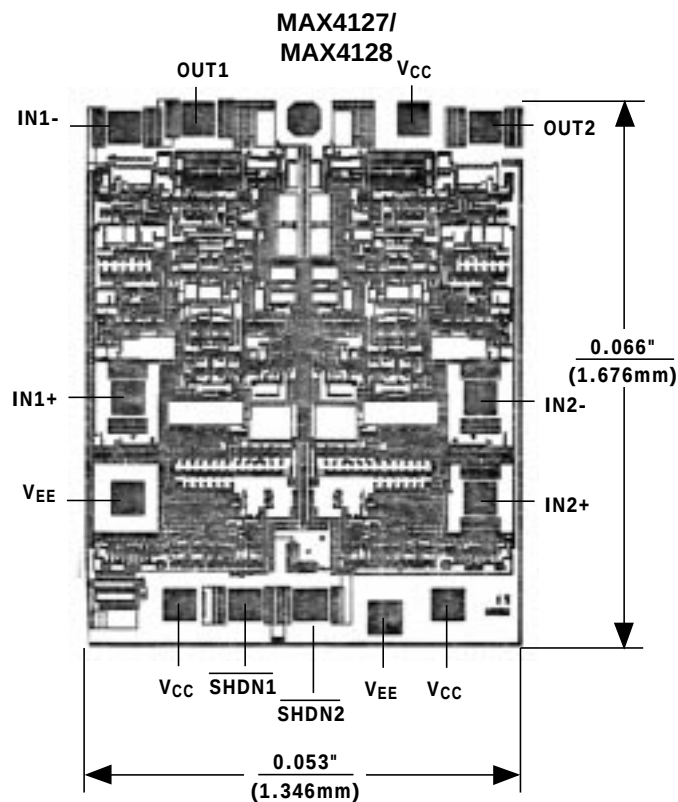
PART	TEMP. RANGE	PIN-PACKAGE	MARKING INFO.
MAX4124EUK	-40°C to +85°C	5 SOT23-5	AABA
MAX4125ESA	-40°C to +85°C	8 SO	—
MAX4125EUA	-40°C to +85°C	8 μ MAX	—
MAX4126ESA	-40°C to +85°C	8 SO	—
MAX4126EUA	-40°C to +85°C	8 μ MAX	—
MAX4127C/D	0°C to +70°C	Dice*	—
MAX4127ESD	-40°C to +85°C	14 SO	—
MAX4128ESA	-40°C to +85°C	8 SO	—
MAX4128EUA	-40°C to +85°C	8 μ MAX	—
MAX4129ESD	-40°C to +85°C	14 SO	—

*Dice are specified at $T_A = +25^\circ\text{C}$, DC parameters only.

Chip Topographies



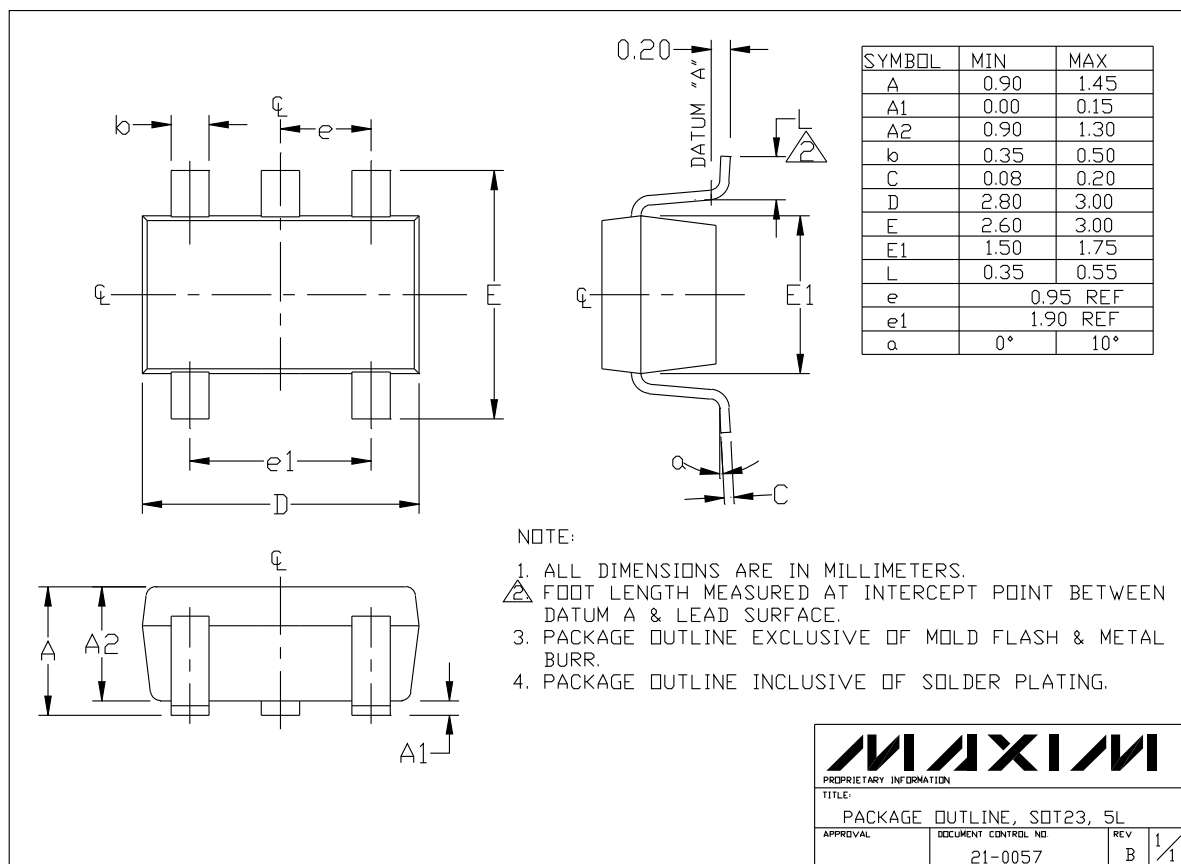
TRANSISTOR COUNT: 170
SUBSTRATE CONNECTED TO V_{EE}



TRANSISTOR COUNT: 340
SUBSTRATE CONNECTED TO V_{EE}

Single/Dual/Quad, Wide-Bandwidth, Low-Power, Single-Supply Rail-to-Rail I/O Op Amps

Package Information



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