Absolute Maximum Ratings

(All voltages referenced to GND, unless otherwise noted.)
Supply Voltage (V_{CC}) ..... +6V
DE, DI ..... -0.3V to +6V
Y, Z ..... -7V to +12.5V
Maximum Continuous Power Dissipation (T_A = +70°C)
SOT23 (derate 8.2mW/°C above +70°C) 654.1mW

Operating Temperature Ranges
MAX32_ _AUT ..... -40°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Junction Temperature ..... +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6 SOT23

Package Code	U6CN+2
Outline Number	**21-0058**
Land Pattern Number	**90-0175**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA}) (C/W)	122.3
Junction to Case (θ_{JC}) (C/W)	84
Thermal Resistance, Multilayer Board:	
Junction to Ambient (θ_{JA}) (C/W)	74.6
Junction to Case (θ_{JC}) (C/W)	6

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CC} = +3.3V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Supply Voltage	V_{CC}			3.135	3.300	3.465	V
Supply Current in Normal Operation	I_Q	No load, DI = V_{CC} or GND, DE = V_{CC}				5	mA
Supply Current in Shutdown Mode	I_{SHDN}	No load, DE = GND			1	10	µA
DRIVER							
Differential Driver Output	V_{OD}	Figure 1, DE = V_{CC}, DI = GND or V_{CC}	R = 50Ω (RS-422), T_A ≤ +85°C	2.0		V_{CC}	V
			R = 27Ω (RS-485), T_A ≤ +85°C	1.5		V_{CC}	
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	Figure 1, R = 27Ω or 50Ω, DE = V_{CC} (Note 3)				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	Figure 1, R = 27Ω or 50Ω, DE = V_{CC}, DI = V_{CC} or GND		-1		+3	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	Figure 1, R = 27Ω or 50Ω (Note 3)				0.2	V
DRIVER LOGIC							
Input High Voltage	V_{IH}	DE, DI		2.0			V
Input Low Voltage	V_{IL}	DE, DI				0.8	V
Input Current	I_{IN}	DE, DI		-2		+2	µA
Output Leakage	I_O	Y, Z DE = GND, V_{CC} = GND or +3.3V	V_{IN} = +12V	-20		+20	µA
			V_{IN} = -7V	-20		+20	
Driver Short-Circuit Foldback Output Current	I_{OSFD}	(VCC - 1V) ≤ V_{OUT} ≤ +12V, output high		+25			mA
		-7V ≤ V_{OUT} ≤ 1V, output high				-25	
Driver Short-Circuit Output Current	I_{OSD}	0 ≤ V_{OUT} ≤ +12V, output low		-250			mA
		-7V ≤ V_{OUT} ≤ V_{CC}, output high				+250	
Thermal-Shutdown Threshold	T_{TS}				160		°C
Thermal-Shutdown Hysteresis	T_{TSH}				40		°C
ESD Protection		Y, Z	Human Body Model		±9		kV

Switching Characteristics (MAX3293)

(V_{CC} = +3.3V ±5%, T_A = +25°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay	t_{PLH}	Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF	400		1300	ns
	t_{PHL}		400		1300	
Driver Differential Output Rise or Fall Time	t_R	Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF	400		1200	ns
	t_F		400		1200	
Driver-Output Skew	t_{SKEW}	Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF, t_{SKEW} = | t_{PLH} - t_{PHL} | (Note 5)	-400		+400	ns
Differential Driver-Output Skew	t_{DSKEW}	Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF	-100		+100	ns
Maximum Data Rate		Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF	250			kbps
Driver Enable to Output High	t_{ZH}	Figures 4, 5; S2 closed, R_L = 500Ω, C_L = 100pF			2000	ns
Driver Enable to Output Low	t_{ZL}	Figures 4, 5; S1 closed, R_L = 500Ω, C_L = 100pF			2000	ns
Driver Disable Time from Low	t_{LZ}	Figures 4, 5; S1 closed, R_L = 500Ω, C_L = 100pF			1000	ns
Driver Disable Time from High	t_{HZ}	Figures 4, 5; S2 closed, R_L = 500Ω, C_L = 100pF			1000	ns
Device-to-Device Propagation Delay Matching		Same power supply, maximum temperature difference between devices = +30°C (Note 5)			900	ns

Switching Characteristics (MAX3294)

(V_{CC} = +3.3V ±5%, T_A = +25°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Propagation Delay	t_{PLH}	Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF	24		70	ns
	t_{PHL}		24		70	
Driver Differential Output Rise or Fall Time	t_R	Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF	10		70	ns
	t_F		10		70	
Driver-Output Skew	t_{SKEW}	Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF, t_{SKEW} = | t_{PLH} - t_{PHL} | (Note 5)	-40		+40	ns
Differential Driver-Output Skew	t_{DSKEW}	Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF	-6		+6	ns
Maximum Data Rate		Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF	2.5			Mbps
Driver Enable to Output High	t_{ZH}	Figures 4, 5; S2 closed, R_L = 500Ω, C_L = 100pF			400	ns
Driver Enable to Output Low	t_{ZL}	Figures 4, 5; S1 closed, R_L = 500Ω, C_L = 100pF			400	ns
Driver Disable Time from Low	t_{LZ}	Figures 4, 5; S1 closed, R_L = 500Ω, C_L = 100pF			100	ns
Driver Disable Time from High	t_{HZ}	Figures 4, 5; S2 closed, R_L = 500Ω, C_L = 100pF			100	ns
Device-to-Device Propagation Delay Matching		Same power supply, maximum temperature difference between devices = +30°C (Note 5)			46	ns

Switching Characteristics (MAX3295)

(V_{CC} = +3.3V ±5%, T_A = +25°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Driver Propagation Delay	t_{PLH}	Figures 2, 3; R_{DIFF} = 54Ω, CL = 50_{pF}				25	ns
	t_{PHL}					25	
Driver Differential Output Rise or Fall Time	t_R	Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF	T_A = -40°C to +125°C			18.5	ns
			T_A < +85°C			15	
	t_F		T_A = -40°C to +125°C			18.5	
			T_A < +85°C			15	
Driver-Output Skew	t_{SKEW}	Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF, t_{SKEW} = | t_{PLH} - t_{PHL} |			5		ns
Differential Driver-Output Skew	t_{DSKEW}	Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF			5		ns
Maximum Data Rate		Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF, T_A ≤ +85°C		20			Mbps
		Figures 2, 3; R_{DIFF} = 54Ω, C_L = 50pF		16			
Driver Enable to Output High	t_{ZH}	Figures 4, 5; S2 closed, R_L = 500Ω, C_L = 100pF				400	ns
Driver Enable to Output Low	t_{ZL}	Figures 4, 5; S1 closed, R_L = 500Ω, C_L = 100pF				400	ns
Driver Disable Time from Low	t_{LZ}	Figures 4, 5; S1 closed, R_L = 500Ω, C_L = 100pF				100	ns
Driver Disable Time from High	t_{HZ}	Figures 4, 5; S2 closed, R_L = 500Ω, C_L = 100pF				100	ns
Device-to-Device Propagation Delay Matching		Same power supply, maximum temperature difference between devices = +30°C (Note 5)				25	ns

Note 1: Devices production tested at +25°C. Limits over the operating temperature range are guaranteed by design.
Note 2: All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to device ground, unless otherwise noted.
Note 3: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.
Note 4: The maximum current applies to peak current just prior to foldback current limiting.
Note 5: Guaranteed by design; not production tested.

Test Circuits and Timing Diagrams

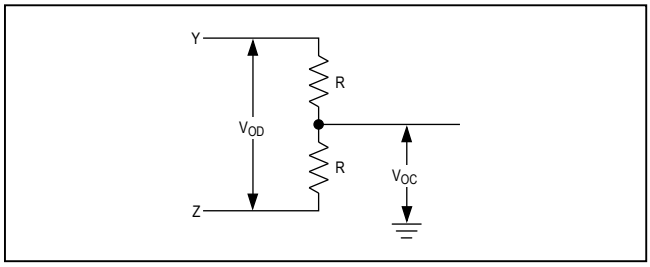


Figure 1. Driver DC Test Load

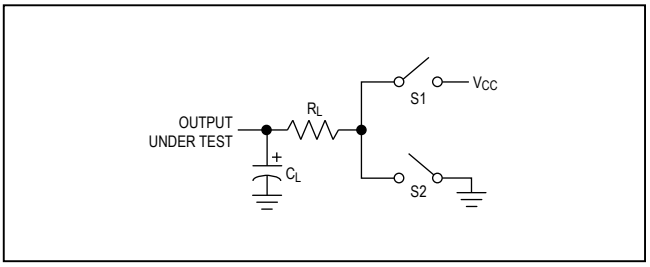


Figure 4. Enable/Disable Timing Test Load

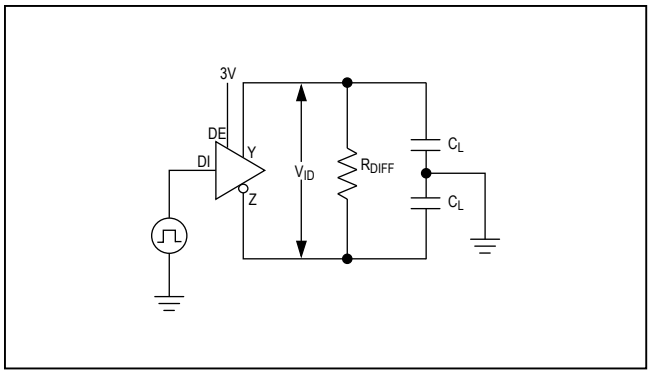


Figure 2. Driver Timing Test Circuit

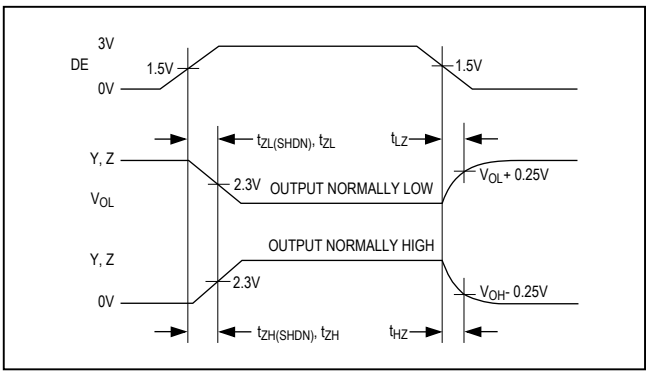


Figure 5. Driver Enable and Disable Times

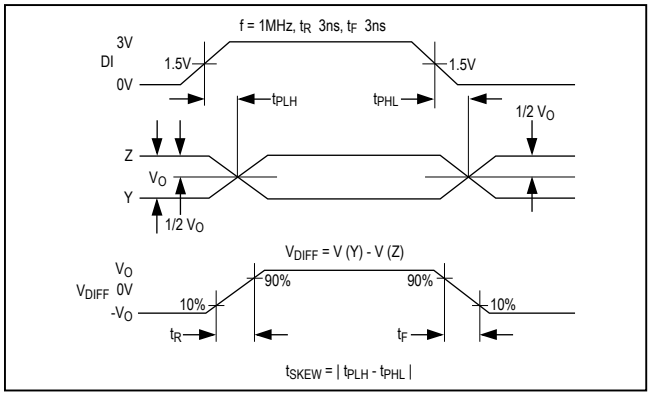
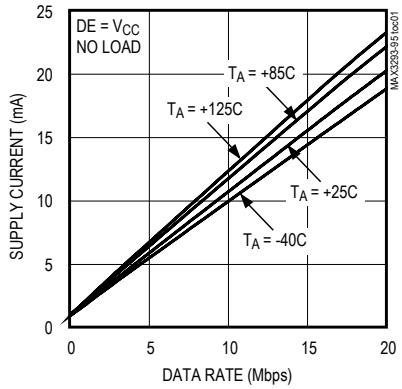


Figure 3. Driver Propagation Delays

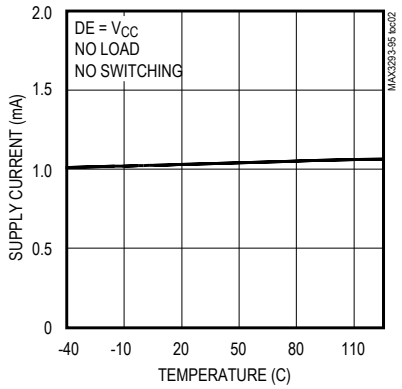
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

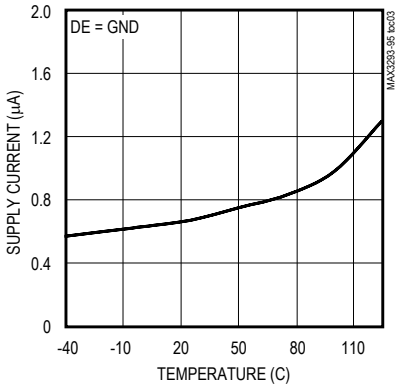
MAX3295
SUPPLY CURRENT vs. DATA RATE



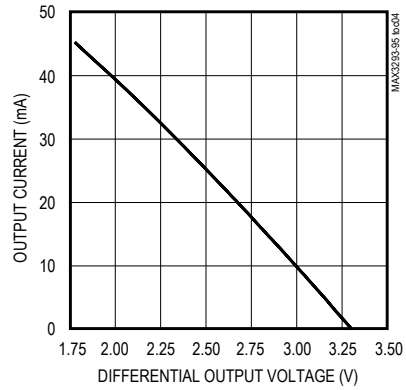
SUPPLY CURRENT vs. TEMPERATURE



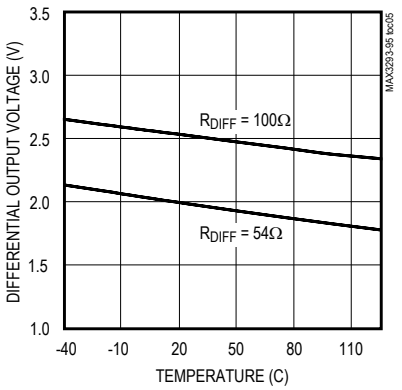
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



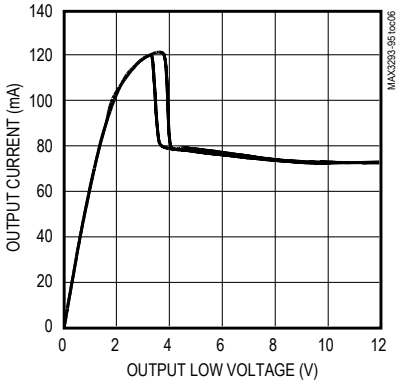
OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



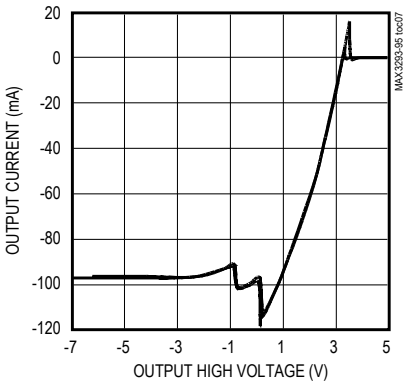
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



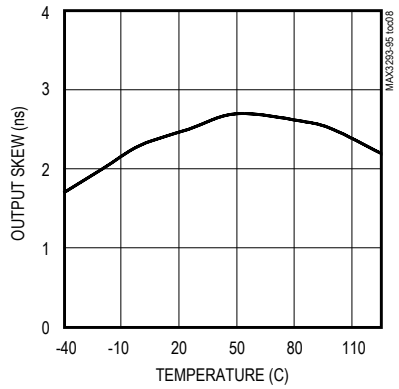
DRIVER-OUTPUT CURRENT vs. DRIVER-OUTPUT LOW VOLTAGE



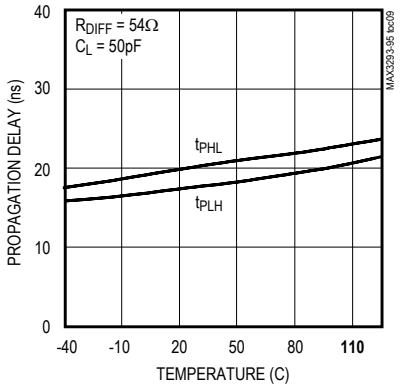
DRIVER-OUTPUT CURRENT vs. DRIVER-OUTPUT HIGH VOLTAGE



OUTPUT SKEW vs. TEMPERATURE



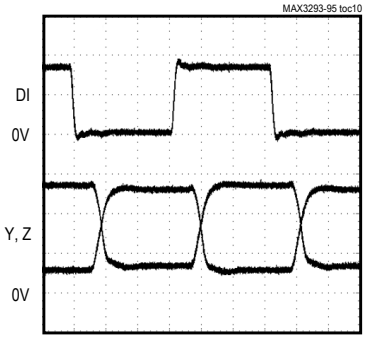
DRIVER PROPAGATION DELAY vs. TEMPERATURE



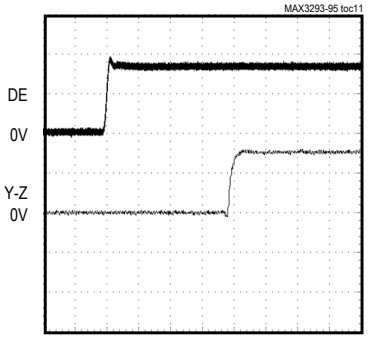
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

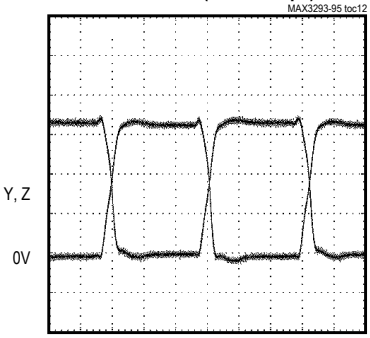
DRIVER PROPAGATION DELAY



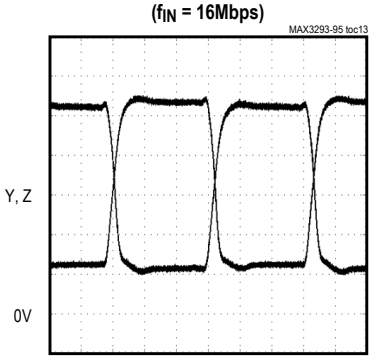
ENABLE RESPONSE TIME



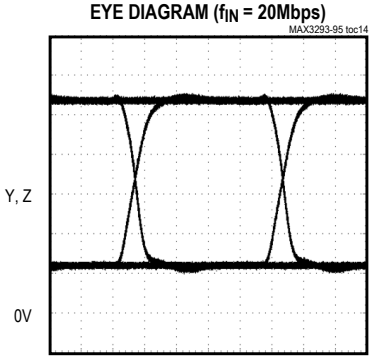
UNLOADED DRIVER-OUTPUT WAVEFORM (f_{IN} = 16Mbps)



LOADED DRIVER-OUTPUT WAVEFORM (f_{IN} = 16Mbps)



EYE DIAGRAM (f_{IN} = 20Mbps)



Pin Description

PIN	NAME	FUNCTION
1	DI	Driver Input. A logic low on DI forces the noninverting output (Y) low and the inverting output (Z) high. A logic high on DI forces the noninverting output (Y) high and the inverting output (Z) low.
2	V_{CC}	Positive Supply. V_{CC} = +3.3V ±5%. Bypass V_{CC} to GND with a 0.1µF capacitor.
3	DE	Driver Output Enable. Force DE high to enable driver. Pull DE low to disable the driver. Hot-swap input, see the *Hot-Swap Capability* section.
4	Z	Inverting RS-485/RS-422 Output
5	GND	Ground
6	Y	Noninverting RS-485/RS-422 Output

Detailed Description

The MAX3293/MAX3294/MAX3295 are low-power transmitters for RS-485/RS-422 communication. The MAX3295 operates at data rates up to 20Mbps, the MAX3294 up to 2.5Mbps (slew-rate limited), and the MAX3293 up to 250kbps (slew-rate limited). These devices are enabled using an active-high driver enable (DE) input. When disabled, outputs enter a high-impedance state, and the supply current reduces to 1µA.

The MAX3293/MAX3294/MAX3295 have a hot-swap input structure that prevents disturbance on the differential signal lines when a circuit board is plugged into a "hot" backplane (see the *Hot-Swap Capability* section). Drivers are also short-circuit current limited and are protected against excessive power dissipation by thermal-shutdown circuitry.

Driver

The driver accepts a single-ended, logic-level input (DI) and translates it to a differential RS-485/RS-422 level output (Y and Z). Driving DE high enables the driver, while pulling DE low places the driver outputs (Y and Z) into a high-impedance state (see Table 1).

Low-Power Shutdown

Force DE low to disable the MAX3293/MAX3294/MAX3295. In shutdown mode, the device consumes a maximum of 10µA of supply current.

Hot-Swap Capability

Hot-Swap Input

When circuit boards are inserted into a "hot" or powered backplane, disturbances to the enable can lead to data errors. Upon initial circuit board insertion, the processor undergoes its power-up sequence. During this period, the output drivers are high impedance and are unable to drive the DE input of the MAX3293/MAX3294/MAX3295 to a defined logic level. Leakage currents up to 10µA from the high-impedance output could cause DE to drift to an incorrect logic state. Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to DE. These factors could improperly enable the driver.

The MAX3293/MAX3294/MAX3295 eliminate all above issues with hot-swap circuitry. When V_{CC} rises, an internal pulldown circuit holds DE low for approximately 10µs. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap tolerable input.

Table 1. MAX3293/MAX3294/MAX3295 (RS-485/RS-422) Transmitting Function Table

INPUTS		OUTPUTS	
DE	DI	Y	Z
0	X	Shutdown	Shutdown
1	0	0	1
1	1	1	0

X = Don't care.

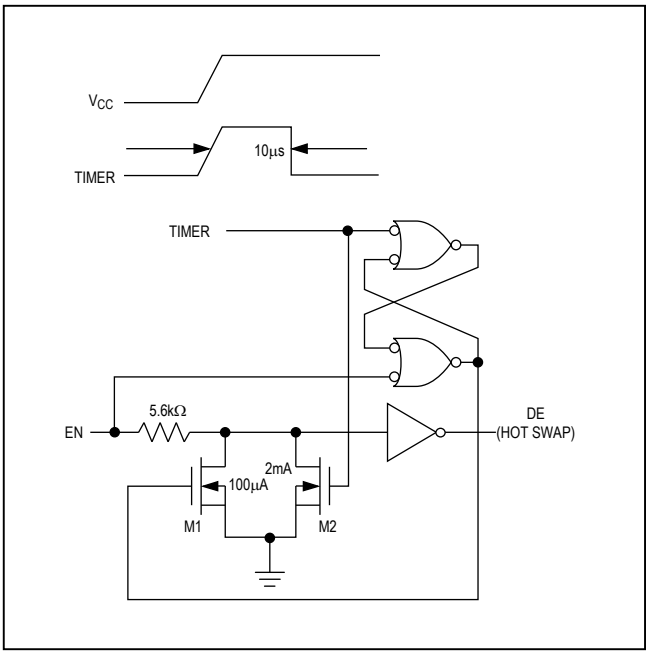


Figure 6. Simplified Structure of the Driver Enable Input (DE)

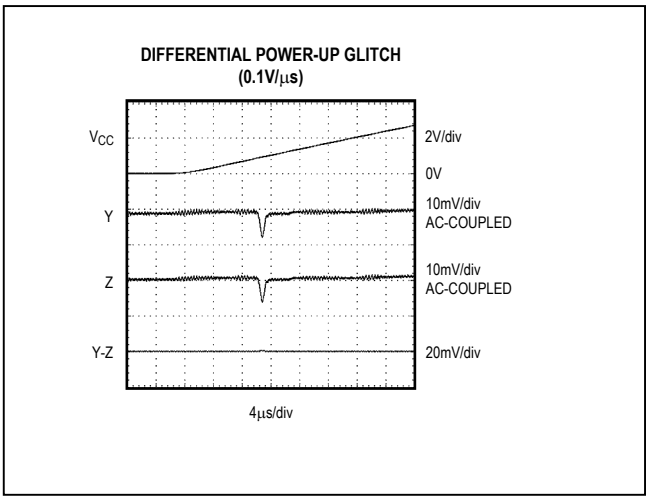


Figure 7. Differential Power-Up Glitch (0.1V/µs)

Hot-Swap Input Circuitry

The MAX3293/MAX3294/MAX3295 enable input features hot-swap capability. At the input, there are two NMOS devices, M1 and M2 (Figure 6). When V_{CC} ramps from zero, an internal 10µs timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 2mA current sink, and M1, a 100µA current sink, pull DE to GND through a 5.6kΩ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that may drive DE high. After 10µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

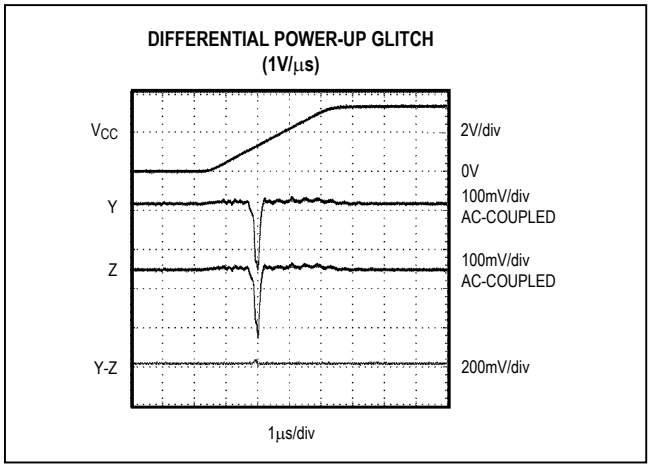


Figure 8. Differential Power-Up Glitch (1V/µs)

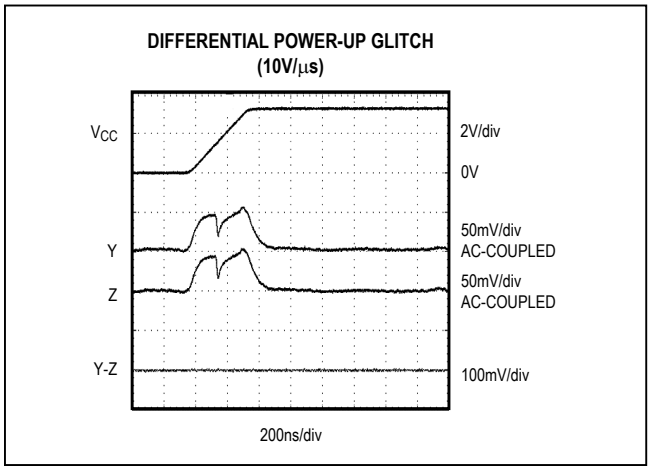


Figure 9. Differential Power-Up Glitch (10V/µs)

Hot-Swap Line Transient

During a hot-swap event when the driver is connected to the line and is powered up, the driver must not cause the differential signal to drop below 200mV. Figures 7, 8, and 9 show the results of the MAX3295 during power-up for three different V_{CC} ramp rates (0.1V/µs, 1V/µs, and 10V/µs). The photos show the V_{CC} ramp, the single-ended signal on each side of the 100Ω termination, as well as the differential signal across the termination.

ESD Protection

Human Body Model

Figure 10 shows the Human Body Model, and Figure 11 shows the current waveform it generates when discharged into low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

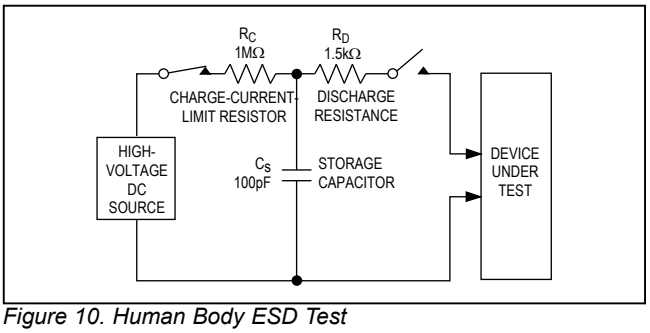


Figure 10. Human Body ESD Test

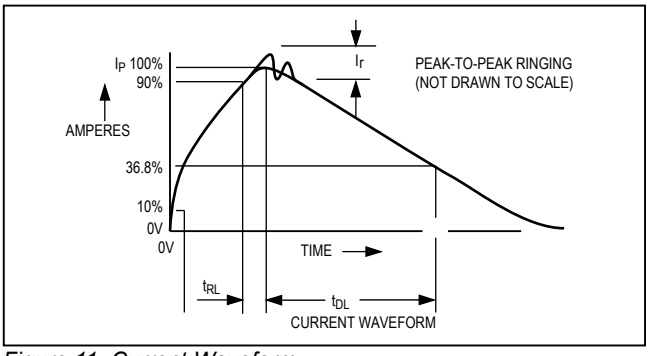


Figure 11. Current Waveform

Reduced EMI and Reflections (MAX3293/MAX3294)

The MAX3293/MAX3294 are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 12 shows Fourier analysis of the MAX3295 transmitting a 125kHz signal. High-frequency harmonics with large amplitudes are evident. Figure 13 shows the same information, but for the slew-rate-limited MAX3293, transmitting the same signal. The high-frequency harmonics have much lower amplitudes, and the potential for EMI is significantly reduced.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX3293 and MAX3294 are more tolerant of imperfect termination.

Driver-Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see the *Typical Operating Characteristics*). The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C.

Chip Information

PROCESS: BiCMOS

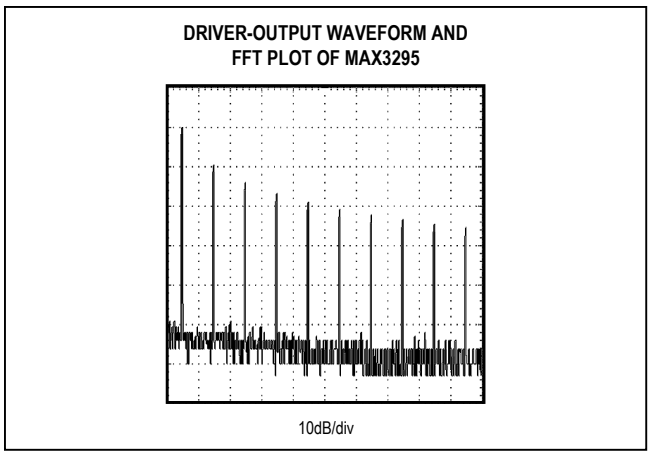


Figure 12. Driver-Output Waveform and FFT Plot of MAX3295 Transmitting a 125kHz Signal

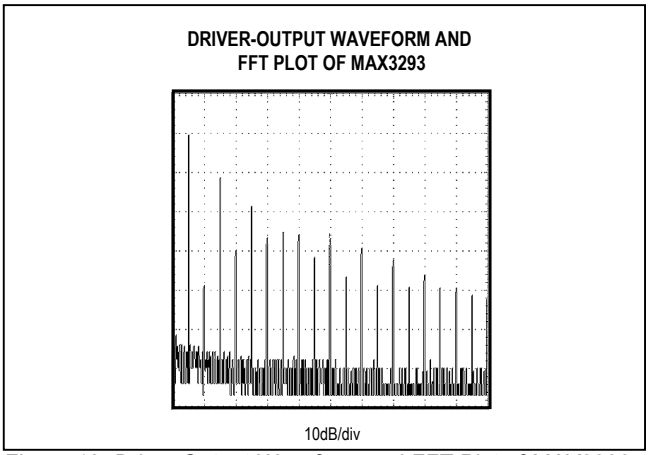
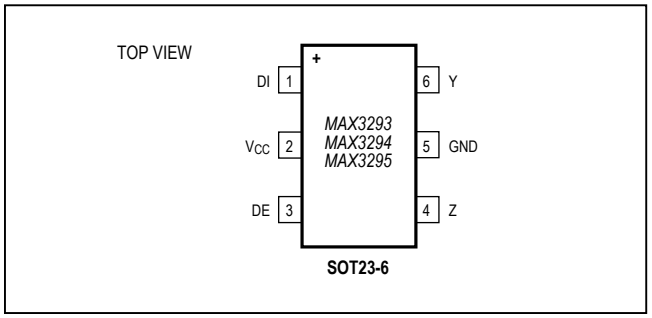


Figure 13. Driver-Output Waveform and FFT Plot of MAX3293 Transmitting a 125kHz Signal

Pin Configuration



Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
3	3/11	Added lead-free parts to the *Ordering Information* and *Selector Guide* tables	1
4	12/14	Added MAX3295AUT/V+T to *Ordering Information*	1
5	4/19	Added AEC-Q100 qualified MAX3295AUT/V+T in *Features*, move and added *Package Information* table with Thermal Characteristics information	1, 2