Absolute Maximum Ratings

V_{IN} to SGND .....-0.3V to +40V
V_{DRV} to SGND ..... -0.3V to +16V (MAX17595)
V_{DRV} to SGND ..... -0.3V to +6V (MAX17596 and MAX17597)
NDRV to SGND .....-0.3V to +(V_{DRV} + 0.3)V
EN/UVLO to SGND ..... -0.3V to +(V_{IN} + 0.3)V
OVI, RT, DITHER, COMP, SS, FB,
SLOPE to SGND .....-0.3V to +6V
CS to SGND .....-0.8V to +6V
PGND to SGND.....-0.3V to +0.3V

Maximum Input/Output Current (Continuous)
V_{IN}, V_{DRV}.....100mA
NDRV (pulsed, for less than 100ns) 1.5A/-0.9A
Continuous Power Dissipation TQFN (single-layer board)
(derate 20.8mW/°C above +70°C) 1666mW
Operating Temperature Range..... -40°C to +125°C
Storage Temperature Range..... -65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

Junction-to-Ambient Thermal Resistance (θ_{JA}) .....48°C/W

Junction-to-Case Thermal Resistance (θ_{JC}).....7°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 12V (for the MAX17595, bring V_{IN} up to 21V for startup), V_{CS} = V_{SLOPE} = V_{DITHER} = V_{FB} = V_{OVI} = V_{SGND} = V_{PGND} = 0V, $V_{EN/UVLO}$ = +2V; NDRV, SS, COMP are unconnected, R_{RT} = 25kΩ, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})							
V_{IN} Voltage Range	V_{IN}	MAX17595		8		29	V
		MAX17596/MAX17597		4.5		36	
V_{IN} Bootstrap UVLO Wakeup	V_{IN-UVR}	V_{IN} rising ↑	MAX17595	18.5	20	21.5	V
			MAX17596/MAX17597	3.8	4.1	4.4	
V_{IN} Bootstrap UVLO Shutdown Level	V_{IN-UVF}	V_{IN} falling ↓	MAX17595	6.5	7	7.5	V
			MAX17596/MAX17597	3.6	3.9	4.2	
V_{IN} Supply Startup Current (Under UVLO)	$I_{VIN-STARTUP}$	V_{IN} < UVLO			20	32	µA
V_{IN} Supply Shutdown Current	I_{IN-SH}	V_{EN} = 0V			20	32	µA
V_{IN} Supply Current	I_{IN-SW}	Switching, f_{SW} = 400kHz			2		mA
V_{IN} Clamp Voltage	V_{INC}	MAX17595, I_{VIN} = 2mA sinking, V_{EN} = 0V (Note 3)		30	33	36	V
ENABLE (EN)							
EN Undervoltage Threshold	V_{ENR}	V_{EN} rising ↑		1.16	1.21	1.26	V
	V_{ENF}	V_{EN} falling ↓		1.1	1.15	1.2	
EN Input Leakage Current	I_{EN}	V_{EN} = 1.5V, T_A = +25°C		-100		+100	nA

Electrical Characteristics (continued)

(V_{IN} = 12V (for the MAX17595, bring V_{IN} up to 21V for startup), V_{CS} = V_{SLOPE} = V_{DITHER} = V_{FB} = V_{OVI} = V_{SGND} = V_{PGND} = 0V, $V_{EN/UVLO}$ = +2V; NDRV, SS, COMP are unconnected, R_{RT} = 25kΩ, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTERNAL LDO (V_{DRV})							
V_{DRV} Output Voltage Range	V_{DRV}	8V < V_{IN} < 15V and 0mA < I_{VDRV} < 50mA (MAX17595)		7.1	7.4	7.7	V
		6V < V_{IN} < 15V and 0mA < I_{VDRV} < 50mA (MAX17596/MAX17597)		4.7	4.9	5.1	
V_{DRV} Current Limit	$I_{VDRV-MAX}$			70	100		mA
V_{DRV} Dropout	$V_{VDRV-DO}$	V_{IN} = 4.5V, I_{VDRV} = 20mA (MAX17596/MAX17597)		4.2			V
OVERVOLTAGE PROTECTION (OVI)							
OVI Overvoltage Threshold	V_{OVIR}	V_{OVI} rising ↑		1.16	1.21	1.26	V
	V_{OVIF}	V_{OVI} falling ↓		1.1	1.15	1.2	
OVI Masking Delay	t_{OVI-MD}				2		µs
OVI Input Leakage Current	I_{OVI}	V_{OVI} = 1V, T_A = +25°C		-100		+100	nA
OSCILLATOR (RT)							
NDRV Switching Frequency Range	f_{SW}			100		1000	kHz
NDRV Switching Frequency Accuracy				-8		+8	%
Maximum Duty Cycle	D_{MAX}	f_{SW} = 400kHz	(MAX17595/MAX17596)	46	48	50	%
			(MAX17597)	90	92.5	95	
SYNCHRONIZATION (DITHER/SYNC)							
Synchronization Logic-High Input	$V_{HI-SYNC}$			3			V
Synchronization Pulse Width					50		ns
Synchronization Frequency Range	f_{SYNC}	(MAX17595/MAX17596) (Note 4)		1.1 x f_{SW}		1.8 x f_{SW}	Hz
DITHERING RAMP GENERATOR (DITHER/SYNC)							
Charging Current				45	50	55	µA
Discharging Current				43	50	57	µA
Ramp-High Trip Point					2		V
Ramp-Low Trip Point					0.4		V

Electrical Characteristics (continued)

(V_{IN} = 12V (for the MAX17595, bring V_{IN} up to 21V for startup), V_{CS} = V_{SLOPE} = V_{DITHER} = V_{FB} = V_{OVI} = V_{SGND} = V_{PGND} = 0V, $V_{EN/UVLO}$ = +2V; NDRV, SS, COMP are unconnected, R_{RT} = 25kΩ, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SOFT-START (SS)						
Soft-Start Charging Current	I_{SSCH}		9	10	11	µA
SS Bias Voltage	V_{SS}		1.19	1.21	1.23	V
NDRV DRIVER (NDRV)						
Pulldown Impedance	R_{NDRV-N}	I_{NDRV} (sinking) = 100mA		1.37	3	Ω
Pullup Impedance	R_{NDRV-P}	I_{NDRV} (sourcing) = 50mA		4.26	8.5	Ω
Peak Sink Current		C_{NDRV} = 10nF		1.5		A
Peak Source Current		C_{NDRV} = 10nF		0.9		A
Fall Time	t_{NDRV-F}	C_{NDRV} = 1nF		10		ns
Rise Time	t_{NDRV-R}	C_{NDRV} = 1nF		20		ns
CURRENT-LIMIT COMPARATOR (CS)						
Cycle-by-Cycle Peak Current-Limit Threshold	$V_{CS-PEAK}$		290	305	320	mV
Cycle-by-Cycle Runaway Current-Limit Threshold	V_{CS-RUN}		340	360	380	mV
Current-Sense Leading-Edge Blanking Time	$t_{CS-BLANK}$	From NDRV rising ↑ edge		70		ns
Propagation Delay from Comparator Input to NDRV	t_{PDCS}	From CS rising (10mV overdrive) to NDRV falling (excluding leading edge blanking)		40		ns
Number of Consecutive Peak- Current-Limit Events to Hiccup	$N_{HICCUP-P}$			8		events
Number of Runaway-Current-Limit Events to Hiccup	$N_{HICCUP-R}$			1		event
Overcurrent Hiccup Timeout				32,768		cycle
Minimum On-Time	t_{ON-MIN}		90	130	170	ns
SLOPE COMPENSATION (SLOPE)						
Slope Bias Current	I_{SLOPE}		9	10	11	µA
Slope Resistor Range			25		200	kΩ

Electrical Characteristics (continued)

(V_{IN} = 12V (for the MAX17595, bring V_{IN} up to 21V for startup), V_{CS} = V_{SLOPE} = V_{DITHER} = V_{FB} = V_{OVI} = V_{SGND} = V_{PGND} = 0V, $V_{EN/UVLO}$ = +2V; NDRV, SS, COMP are unconnected, R_{RT} = 25kΩ, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = T_J = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slope Voltage Range for Default Slope Compensation			4			V
Slope Voltage Range for Programmable Slope Compensation			0.2		2	V
Slope Compensation Ramp		R_{SLOPE} = 100kΩ	140	165	190	mV/µs
Default Slope Compensation Ramp		4V < V_{SLOPE}		50		mV/µs
PWM COMPARATOR						
Comparator Offset Voltage	V_{PWM-OS}	V_{COMP}, when V_{CS} = 0	1.65	1.81	2	V
Current-Sense Gain	A_{CS-PWM}	$\Delta V_{COMP}/\Delta V_{CS}$	1.75	1.97	2.15	V/V
Comparator Propagation Delay	t_{PWM}	Change in V_{CS} = 10mV (including internal lead-edge blanking)		110		ns
ERROR AMPLIFIER						
FB Reference Voltage	V_{REF}	V_{FB}, when I_{COMP} = 0 and V_{COMP} = 1.8V	1.19	1.21	1.23	V
FB Input Bias Current	I_{FB}	V_{FB} = 1.5V, T_A = +25°C	-100		+100	nA
Voltage Gain	A_{EAMP}			90		dB
Transconductance	Gm		1.5	1.8	2.1	mS
Transconductance Bandwidth	BW	Open-loop (gain = 1), -3dB frequency		10		MHz
Source Current		V_{COMP} = 1.8V, V_{FB} = 1V	80	120	210	µA
Sink Current		V_{COMP} = 1.8V, V_{FB} = 1.75V	80	120	210	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		+160		°C
Thermal-Shutdown Hysteresis				20		°C

Note 2: All devices 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

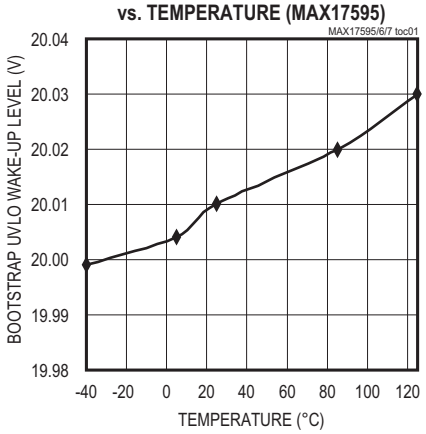
Note 3: The MAX17595 is intended for use in universal input power supplies. The internal clamp circuit at V_{IN} is used to prevent the bootstrap capacitor from charging to a voltage beyond the absolute maximum rating of the device when EN is low (shutdown mode). Externally limit the maximum current to V_{IN} (hence to clamp) to 2mA (max) when EN is low.

Note 4: Using an external clock for synchronization increases the maximum duty cycle by a factor equal to f_{SYNC} / f_{SW} for the MAX17595/MAX17596. External synchronization is not available for the MAX17597.

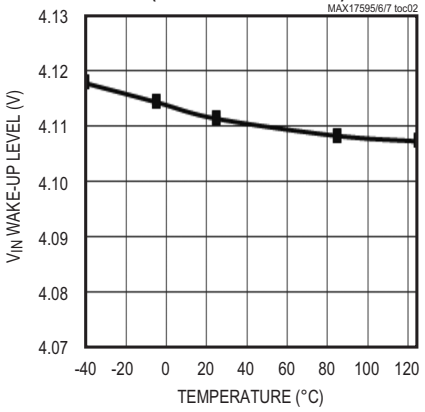
Typical Operating Characteristics

(V_{IN} = 15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

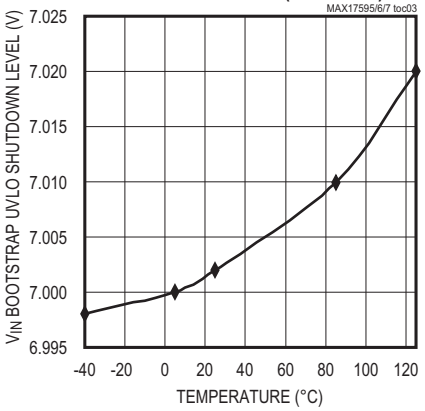
BOOTSTRAP UVLO WAKE-UP LEVEL vs. TEMPERATURE (MAX17595)



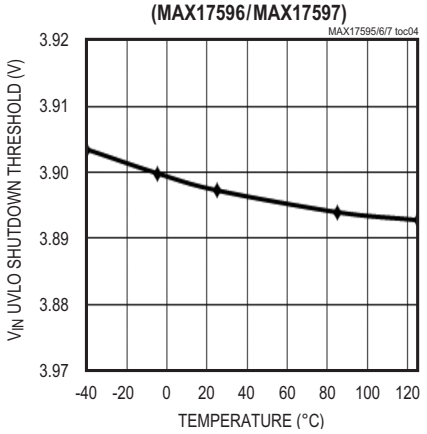
V_{IN} WAKE-UP LEVEL vs. TEMPERATURE (MAX17596/MAX17597)



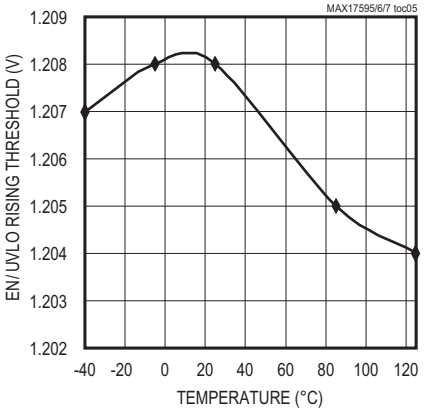
V_{IN} FALLING THRESHOLD vs. TEMPERATURE (MAX17595)



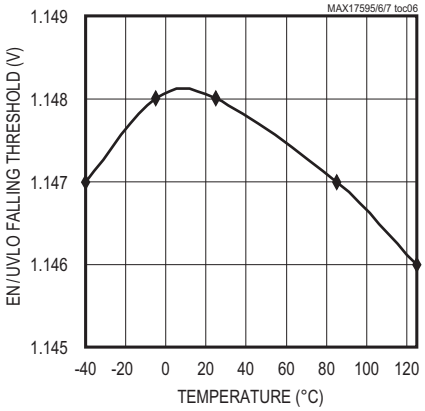
V_{IN} FALLING THRESHOLD vs. TEMPERATURE (MAX17596/MAX17597)



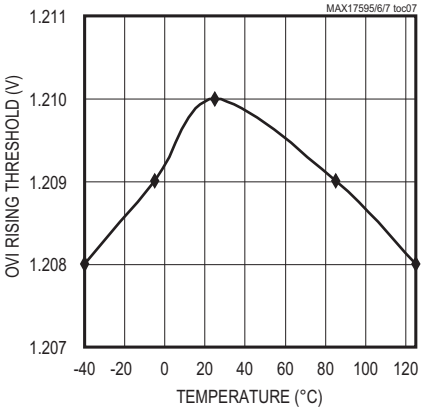
EN/UVLO RISING THRESHOLD vs. TEMPERATURE



EN/UVLO FALLING THRESHOLD vs. TEMPERATURE



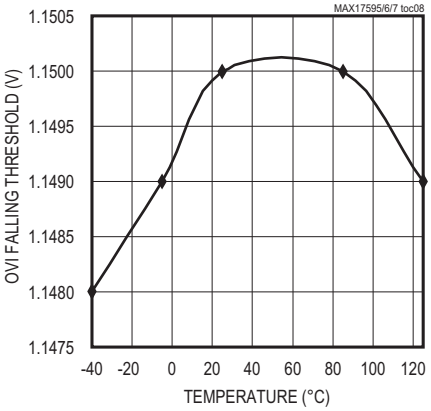
OVI RISING THRESHOLD vs. TEMPERATURE



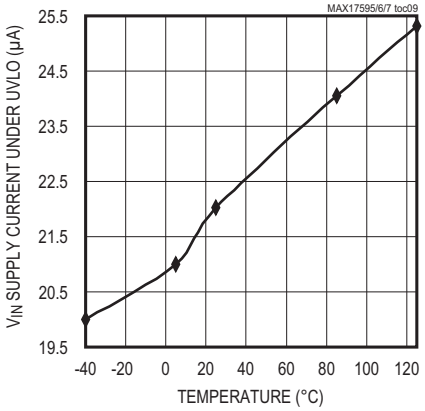
Typical Operating Characteristics (continued)

(V_{IN} = 15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

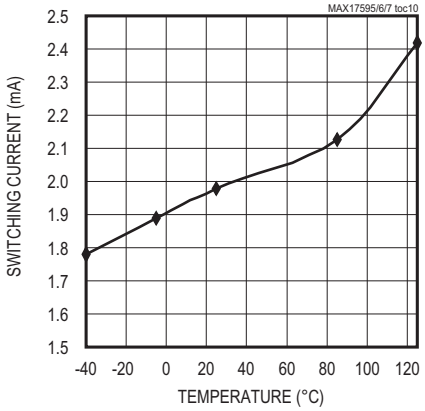
OVI FALLING THRESHOLD vs. TEMPERATURE



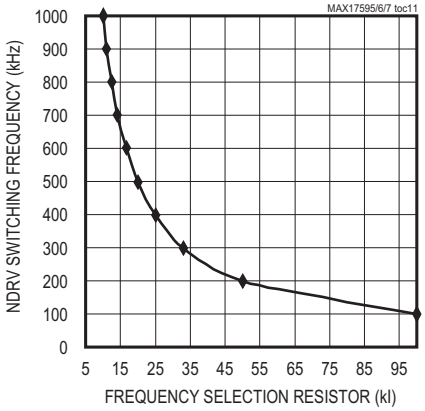
V_{IN} SUPPLY CURRENT UNDER UVLO vs. TEMPERATURE



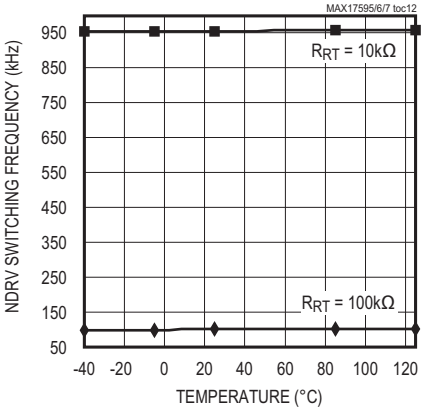
SWITCHING CURRENT vs. TEMPERATURE



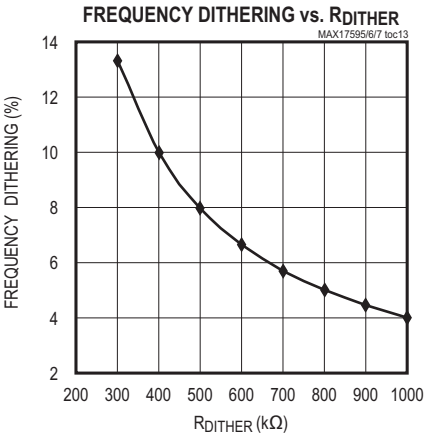
NDRV SWITCHING FREQUENCY vs. RESISTOR



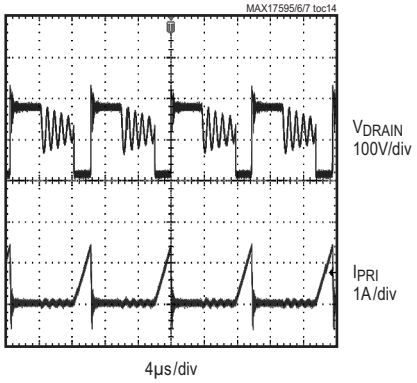
NDRV SWITCHING FREQUENCY vs. TEMPERATURE



FREQUENCY DITHERING vs. R_{DITHER}



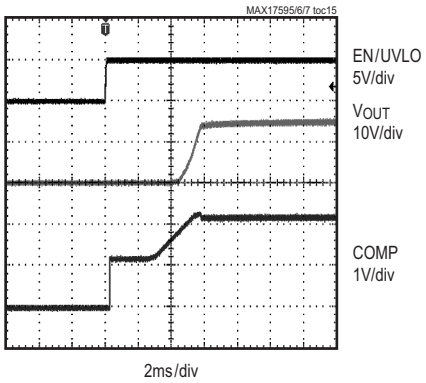
SWITCHING WAVEFORMS (MAX17595)



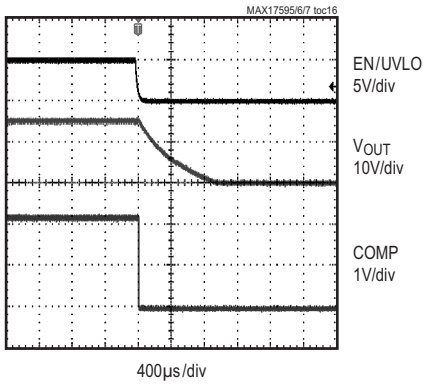
Typical Operating Characteristics (continued)

(V_{IN} = 15V, $V_{EN/UVLO}$ = +2V, COMP = open, C_{VIN} = 1µF, C_{VDRV} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted.)

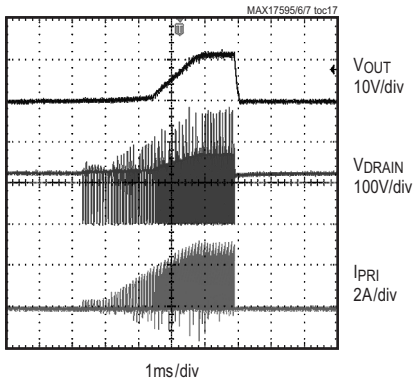
ENABLE STARTUP



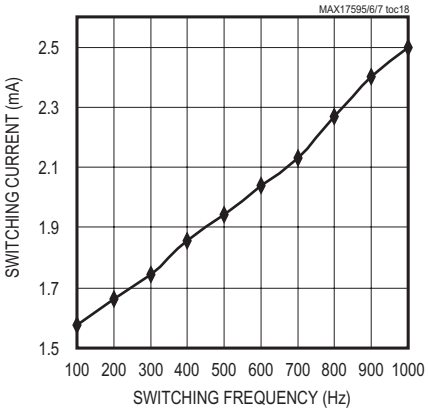
ENABLE SHUTDOWN



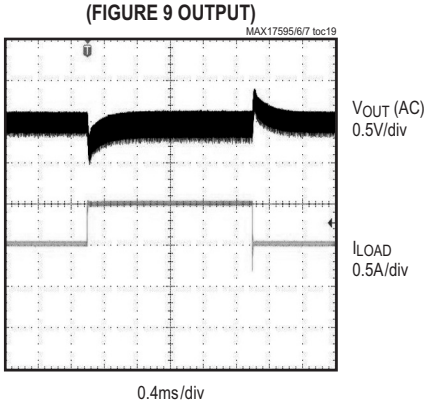
HICCUP OPERATION



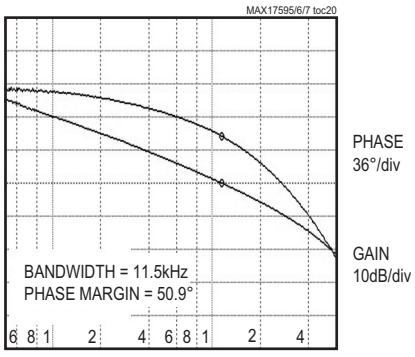
SWITCHING CURRENT vs. SWITCHING FREQUENCY



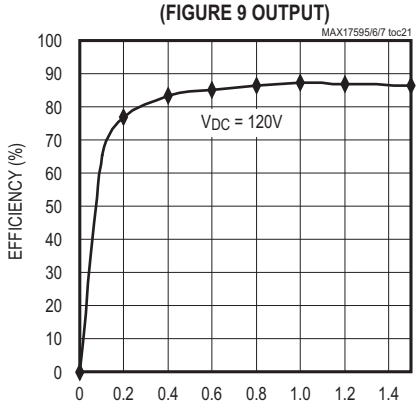
LOAD TRANSIENT RESPONSE (FIGURE 9 OUTPUT)



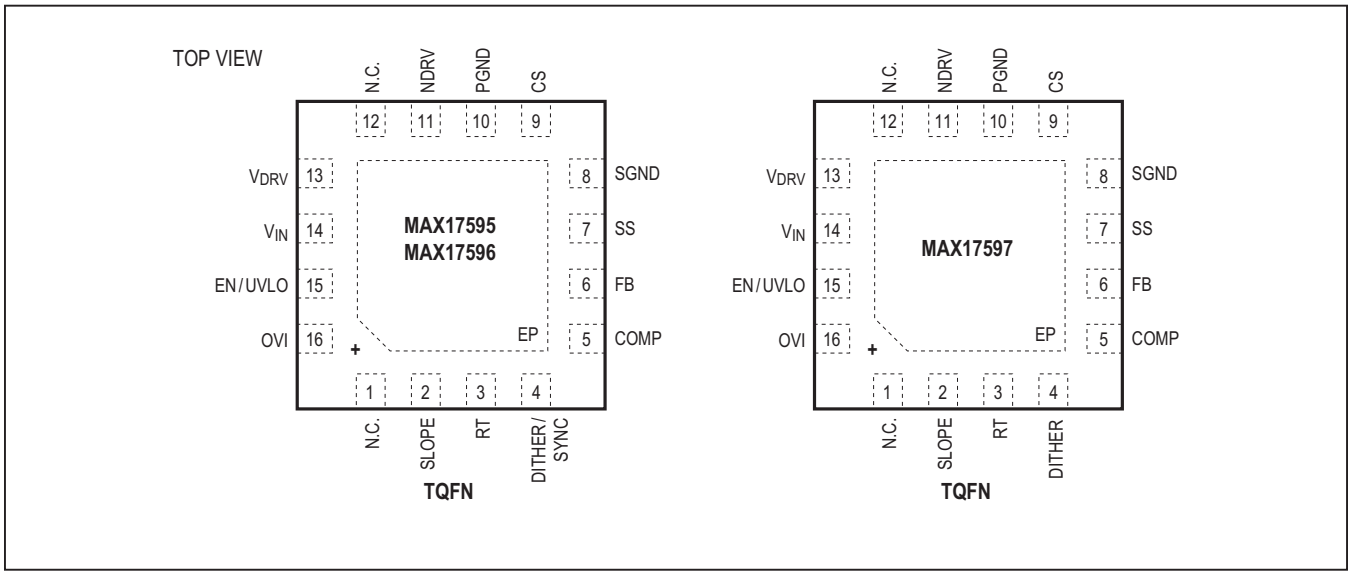
BODE PLOT (FIGURE 9 OUTPUT)



EFFICIENCY GRAPH (FIGURE 9 OUTPUT)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 12	N.C.	No Connection
2	SLOPE	Slope Compensation Input. A resistor, R_{SLOPE}, connected from SLOPE to SGND programs the amount of slope compensation with reference-voltage soft-start mode. Floating the SLOPE pin enables reference voltage soft-start with default slope compensation of 50mV/µs.
3	RT	Switching Frequency Programming Resistor Connection. Connect resistor R_{RT} from RT to SGND to set the PWM switching frequency.
4	DITHER/SYNC	Frequency Dithering Programming or Synchronization Connection. For spread-spectrum frequency operation, connect a capacitor from DITHER to SGND, and a resistor from DITHER to RT. To synchronize the internal oscillator to the externally applied frequency (MAX17595/MAX17596 only), connect DITHER/SYNC to the synchronization pulse.
5	COMP	Transconductance Amplifier Output. Connect the frequency compensation network between COMP and SGND.
6	FB	Transconductance Amplifier Inverting Input
7	SS	Soft-Start Capacitor Pin for Flyback Regulator. Connect a capacitor C_{SS} from SS to SGND to set the soft-start time interval.
8	SGND	Signal Ground. Connect SGND to the signal ground plane.
9	CS	Current-Sense Input. Peak-current-limit trip voltage is 300mV (typ).
10	PGND	Power Ground. Connect PGND to the power ground plane.
11	NDRV	External Switching nMOS Gate-Driver Output

Pin Description (continued)

PIN	NAME	FUNCTION
13	V_{DRV}	Linear Regulator Output and Driver Input. Connect a 1µF bypass capacitor from V_{DRV} to SGND as close as possible to the IC.
14	V_{IN}	Internal V_{DRV} Regulator Input. Connect V_{IN} to the input voltage source. Bypass V_{IN} to PGND with a 1µF minimum ceramic capacitor.
15	EN/UVLO	Enable/Undervoltage Lockout. To externally program the UVLO threshold of the input supply, connect a resistive divider between input supply, EN, and SGND.
16	OVI	Overvoltage Comparator Input. Connect a resistive divider between the input supply, OVI, and SGND to set the input overvoltage threshold.
—	EP	Exposed Pad. Connect to a large ground plane through multiple vias to maximize thermal dissipation.

Detailed Description

The MAX17595 offers a bootstrap UVLO wake-up level of 20V with a wide hysteresis, and is optimized for implementing isolated and nonisolated universal (85V to 265V AC) offline single-switch flyback converter or telecom (36V to 72V) power supplies. The MAX17596/MAX17597 offer a UVLO wake-up level of 4.4V and are well-suited for low-voltage DC-DC flyback/boost power supplies. An internal 1% reference (1.21V) can be used to regulate the output in nonisolated flyback and boost applications. Additional semiregulated outputs, if needed, can be generated by using additional secondary windings on the flyback converter transformer.

The MAX17595/MAX17596/MAX17597 family utilizes peak-current-mode control and external compensation for optimizing closed-loop performance. The devices include cycle-by-cycle peak current limit, and eight consecutive occurrences of current-limit-event trigger hiccup mode, which protects external components by halting switching for a period of 32,768 cycles. .

Input Voltage Range (V_{IN})

The MAX17595 has no limitation on maximum input voltage, as long as the external components are rated suitably and the maximum operating voltages of the MAX17595 are respected.

The MAX17595 implements a rising and falling UVLO threshold that allows it to be successfully used in universal input (85V to 265V AC) rectified bus applications, in rectified 3-phase DC bus applications, and in telecom (36V to 72V DC) applications.

The MAX17596/MAX17597 are intended to implement flyback (isolated and nonisolated) and boost converters. The V_{IN} pin of the MAX17596/MAX17597 has a maximum operating voltage of 36V. The MAX17596/MAX17597 implement rising and falling thresholds on the V_{IN} pin that assume power-supply startup schemes typical of low-voltage DC-DC applications, down to an input voltage of 4.5V DC. Therefore, flyback/boost converters with a 4.5V to 36V supply voltage range can be implemented with the MAX17596/MAX17597.

Internal Linear Regulator (V_{DRV})

The internal functions and driver circuits are designed to operate from 7.4V (MAX17595) or 5V (MAX17596/MAX17597) power-supply voltages. The MAX17595/MAX17596/MAX17597 family has an internal linear regulator that is powered from the V_{IN} pin. The output of the linear regulator is connected to the V_{DRV} pin, and should be decoupled with a 1µF capacitor to ground for stable operation. The V_{DRV} regulator output supplies all the operating current of the MAX17595/MAX17596/MAX17597. The maximum operating voltage on the V_{IN} pin is 29V for the MAX17595, and 36V for the MAX17596/MAX17597.

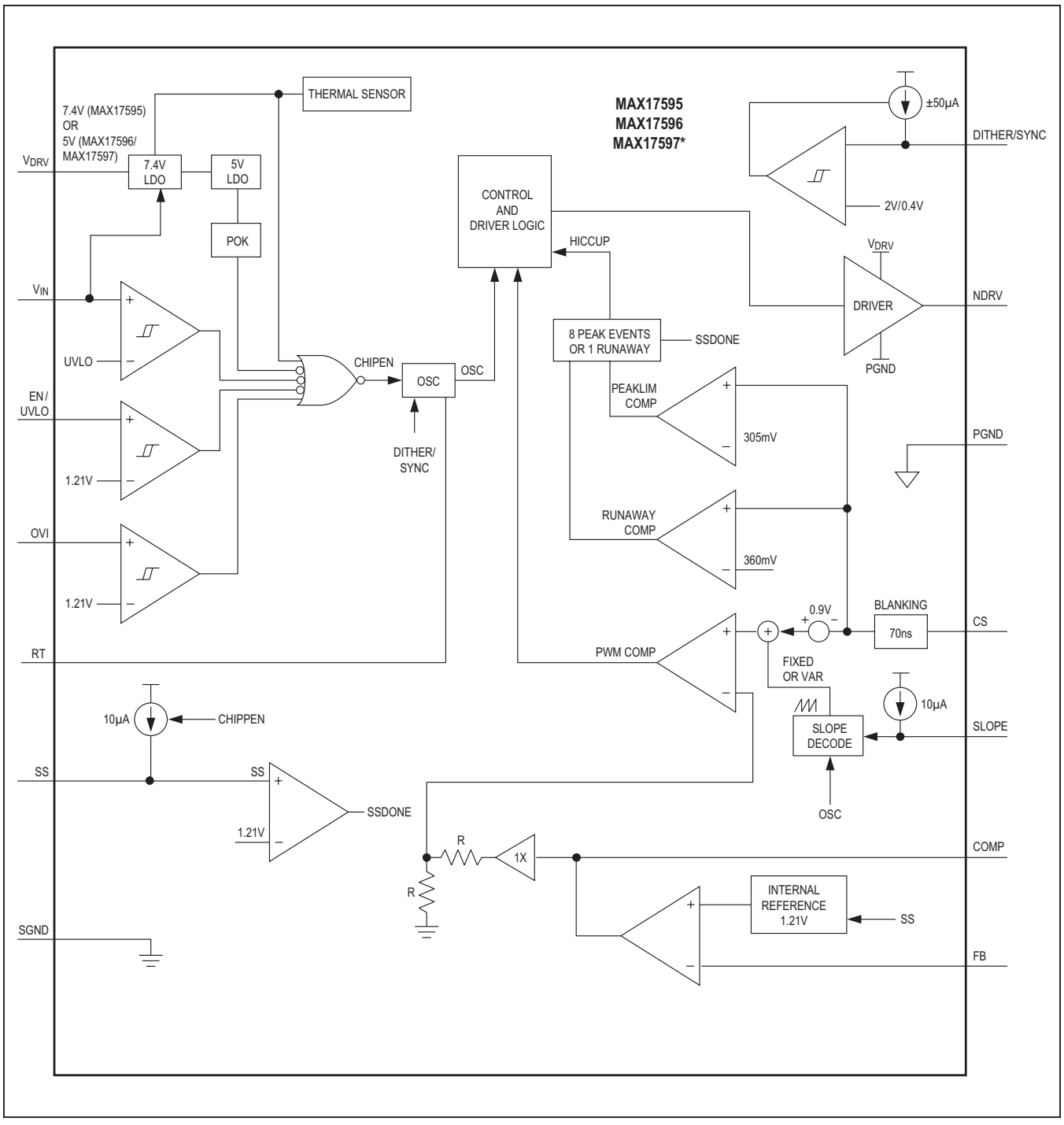


*Figure 1. MAX17595/MAX17596/MAX17597 Block Diagram (*See Note 4.)*

n-Channel MOSFET Gate Driver (NDRV)

The devices offer a built-in gate driver for driving an external n-channel MOSFET. The NDRV pin can source/sink peak currents in excess of 900mA/1500mA.

Maximum Duty Cycle

The MAX17595/MAX17596 operate at a maximum duty cycle of 49%. The MAX17597 offers a maximum duty cycle of 94% to implement flyback and boost converters involving large input-to-output voltage ratios in DC-DC applications. Slope compensation is necessary for stable operation of peak-current-mode controlled converters such as the MAX17595/MAX17596/MAX17597, in addition to the loop compensation required for small signal stability. The MAX17595/MAX17596/MAX17597 implement a SLOPE pin for this purpose. See the *Slope Compensation* section for more details.

Soft-Start (SS)

The devices implement soft-start operation for the flyback/boost regulators. A capacitor connected to the SS pin programs the soft-start period. The soft-start feature reduces input inrush current during startup. When the voltage on the SLOPE pin is more than 0.2V, the reference to the internal error amplifier is ramped up from 0V to 1.21V in a linear manner, as programmed by the soft-start capacitor. See the *Programming Soft-Start (SS)* section.

Switching Frequency Selection (RT)

The ICs' switching frequency is programmable between 100kHz and 1MHz with resistor R_{RT} connected between RT and SGND. Use the following formula to determine the appropriate value of R_{RT} needed to generate the desired output-switching frequency (f_{SW}):

$$R_{RT} = \frac{10^{10}}{f_{SW}}$$

where f_{SW} is the desired switching frequency.

Frequency Dithering for Spread-Spectrum Applications (Low EMI)

The switching frequency of the converter can be dithered in a range of ±10% by connecting a capacitor from DITHER/SYNC to SGND, and a resistor from DITHER to RT. Spread-spectrum modulation technique spreads the energy of switching frequency and its harmonics over a wider band while reducing their peaks, helping to meet stringent EMI goals.

Applications Information

Startup Voltage and Input Overvoltage Protection Setting (EN/UVLO, OVI)

The devices' EN/UVLO pin serves as an enable/disable input, as well as an accurate programmable input UVLO pin. The devices do not commence startup operation unless the EN/UVLO pin voltage exceeds 1.21V (typ). The devices turn off if the EN/UVLO pin voltage falls below 1.15V (typ). A resistor-divider from the input DC bus to ground can be used to divide down and apply a fraction of the input DC voltage (V_{DC}) to the EN/UVLO pin. The values of the resistor-divider can be selected so the EN/UVLO pin voltage exceeds the 1.23V (typ) turn-on threshold at the desired input DC bus voltage. The same resistor-divider can be modified with an additional resistor (R_{OVI}) to implement input overvoltage protection in addition to the EN/UVLO functionality as shown in Figure 2. When voltage at the OVI pin exceeds 1.21V (typ), the devices stop switching and resume switching operations only if voltage at the OVI pin falls below 1.15V (typ). For given values of startup DC input voltage (V_{START}) and input overvoltage-protection voltage (V_{OVI}), the resistor values for the divider can be calculated as follows, assuming a 24.9kΩ resistor for R_{OVI}:

$$R_{EN} = R_{OVI} \times \left[\frac{V_{OVI}}{V_{START}} - 1\right] k\Omega$$

where R_{OVI} is in kΩ, while V_{START} and V_{OVI} are in volts.

$$R_{SUM} = \left[R_{OVI} + R_{EN}\right] \times \left[\frac{V_{START}}{1.21} - 1\right] k\Omega$$

where R_{EN} and R_{OVI} are in kΩ, while V_{START} is in volts.

In universal AC input applications, R_{SUM} may need to be implemented as equal resistors in series (R_{DC1}, R_{DC2}, and R_{DC}) so that voltage across each resistor is limited to its maximum operation voltage.

$$R_{DC1} = R_{DC2} = R_{DC3} = \frac{R_{SUM}}{3} k\Omega$$

For low-voltage DC-DC applications based on the MAX17596/MAX17597, a single resistor can be used in the place of R_{SUM}, as the voltage across it is approximately 40V.

Startup Operation

The MAX17595 is optimized for implementing an offline single-switch flyback converter and has a 20V V_{IN} UVLO wake-up level with hysteresis of 15V (min). In offline applications, a simple cost-effective RC startup circuit is used. When the input DC voltage is applied, the startup resistor (R_{START}) charges the startup capacitor (C_{START}), causing the voltage at the V_{IN} pin to increase towards the wake-up V_{IN} UVLO threshold (20V typ). During this time, the MAX17595 draws a low startup current of 20µA (typ) through R_{START}. When the voltage at V_{IN} reaches the wake-up V_{IN} UVLO threshold, the MAX17595 commences switching and control operations. In this condition, the MAX17595 draws 2mA (typ) current from C_{START} for its internal operation. In addition, the gate-drive current is also drawn from C_{START}, which is a function of the gate charge of the external MOSFET used and switching frequency. Since this total current cannot be supported by the current through R_{START}, the voltage on C_{START} starts to drop. When suitably configured, as shown in Figure 3, the external MOSFET is switched by the NDRV pin and the flyback converter generates pulses on bias winding NB. The soft-start period of the converter should be programmed so the bias winding pulses sustain the voltage on C_{START} before it falls below 7V, thus allowing continued operation. The large hysteresis of the MAX17595 allows for a small startup capacitor (C_{START}). The low startup current (20µA typ) allows the use of a large startup resistor (R_{START}), thus reducing power dissipation at higher DC bus voltages. R_{START} might need to be implemented as equal, multiple resistors in series (R_{IN1}, R_{IN2}, and R_{IN3}) to share the applied high DC voltage in offline applications so that the voltage across each resistor is limited to its maximum continuous operating voltage rating. R_{START} and C_{START} can be calculated as:

$$C_{START} = 0.75 \left(\begin{matrix} C_{VDRV} + I_{IN} \times t_{SS} \times 0.1 \\ + 0.04 \times \frac{t_{SS} \times Q_G \times f_{SW}}{10^6} \end{matrix} \right) \mu F$$

where I_{IN} is the supply current drawn at the V_{IN} pin in mA, Q_G is the gate charge of the external MOSFET used in nC, f_{SW} is the switching frequency of the converter in Hz, and t_{SS} is the soft-start time programmed for the flyback converter in ms. C_{VDRV} is a cummulative capacitor used in V_{DRV} node in µF. See the *Programming Soft-Start of Flyback/Boost Converter (SS)* section.

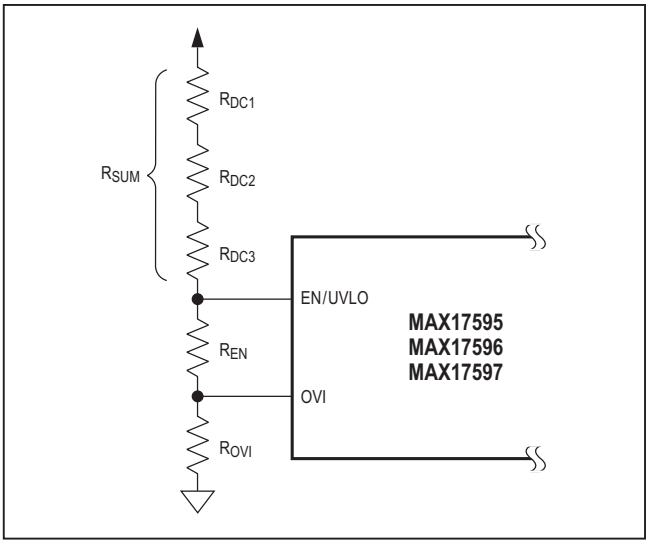


Figure 2. Programming EN/UVLO and OVI

$$R_{START} = \frac{(V_{START} - 10) \times 50}{[1 + C_{START}]} \ k\Omega$$

where C_{START} is the startup capacitor in µF.

For designs that cannot accept power dissipation in the startup resistors at high DC input voltages in offline applications, the startup circuit can be set up with a current source instead of a startup resistor as shown in Figure 4.

The startup capacitor (C_{START}) can be calculated using the above equation:

Resistors R_{SUM} and R_{ISRC} can be calculated as:

$$R_{SUM} = \frac{V_{START}}{10} \ M\Omega$$

$$R_{ISRC} = \frac{V_{BEQ1}}{70} \ M\Omega$$

The V_{IN} UVLO wake-up threshold of the MAX17596/MAX17597 is set to 4.1V (typ) with a 200mV hysteresis, optimized for low-voltage DC-DC applications down to 4.5V. For applications where the input DC voltage is low enough (e.g., 4.5V to 5.5V DC) that the power loss incurred to supply the operating current of the MAX17596/MAX17597 can be tolerated, the V_{IN} pin is directly connected to the DC input, as shown in Figure 5. In the case of higher DC input voltages (e.g., 16V to 32V DC), a startup circuit, such as that shown in Figure 6, can be used to minimize power dissipation. In this startup

scheme, the transistor (Q1) supplies the switching current until a bias winding NB comes up and turns off Q1. The resistor (R_Z) can be calculated as:

$$R_Z = 2 \times (V_{INMIN} - 6.3)\ k\Omega$$

Programming Soft-Start (SS)

The soft-start period for the devices can be programmed by selecting the value of the capacitor C_{SS} connected from the SS pin to SGND. Capacitor C_{SS} can be calculated as:

$$C_{SS} = 8.2645 \times t_{SS}\ nF$$

where t_{SS} is expressed in ms. This equation is directly applicable to the boost converter application circuit of Figure 11. For optoisolated converters, the soft-start period is approximately equal to 30% of t_{SS} when the

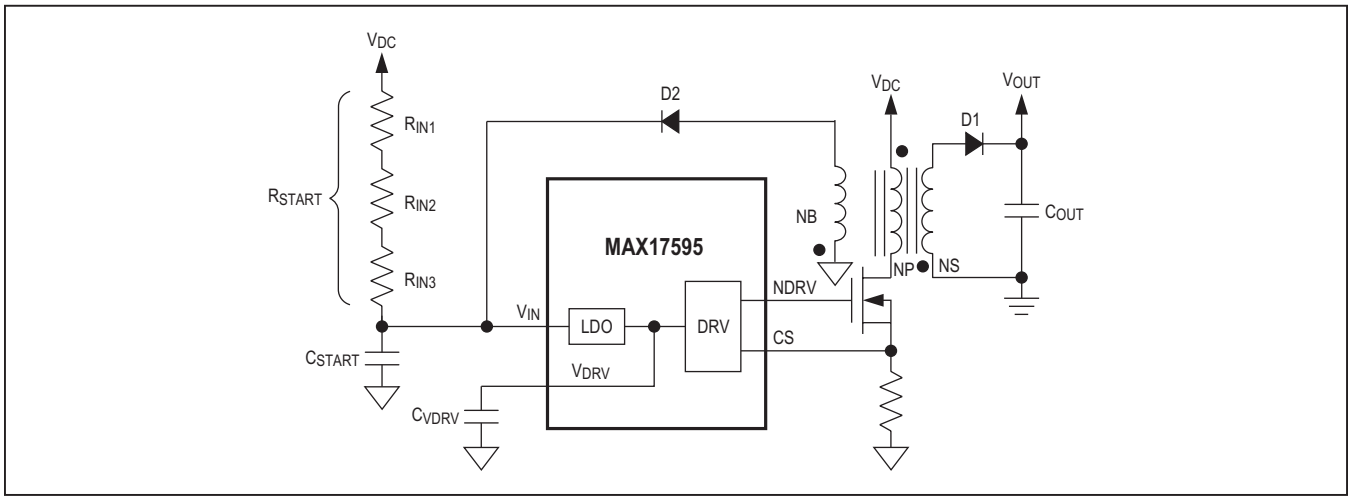


Figure 3. MAX17595 RC-Based Startup Circuit

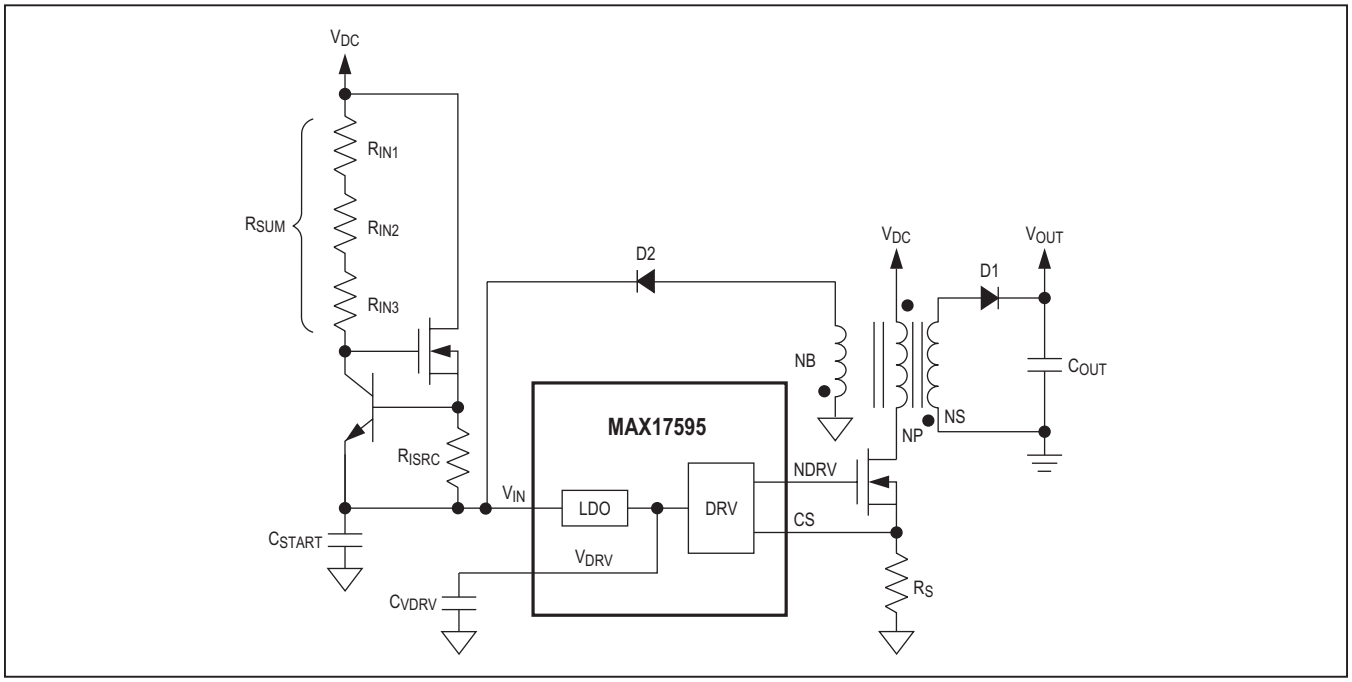


Figure 4. MAX17595 Current-Source-Based Startup Circuit

error amplifier is set up as a proportional gain amplifier as shown in Figure 9.

Programming Output Voltage

The devices incorporate an error amplifier with a 1% precision voltage reference that enables negative feedback control of the output voltage. The output voltage of the switching converter can be programmed by selecting the values for the resistor-divider connected from V_{OUT}, and the flyback/boost output to ground, with the midpoint of the divider connected to the FB pin (Figure 7). With R_B selected in the 20kΩ to 50kΩ range, R_U can be calculated as:

$$R_U = R_B \times \left[\frac{V_{OUT}}{1.21} - 1\right] k\Omega, \text{ where } R_B \text{ is in } k\Omega.$$

Peak-Current-Limit Setting (CS)

The devices include a robust overcurrent protection scheme that protects the device under overload and short-circuit conditions. A current-sense resistor, connected between the source of the MOSFET and PGND, sets the peak current limit. The current-limit comparator has a voltage

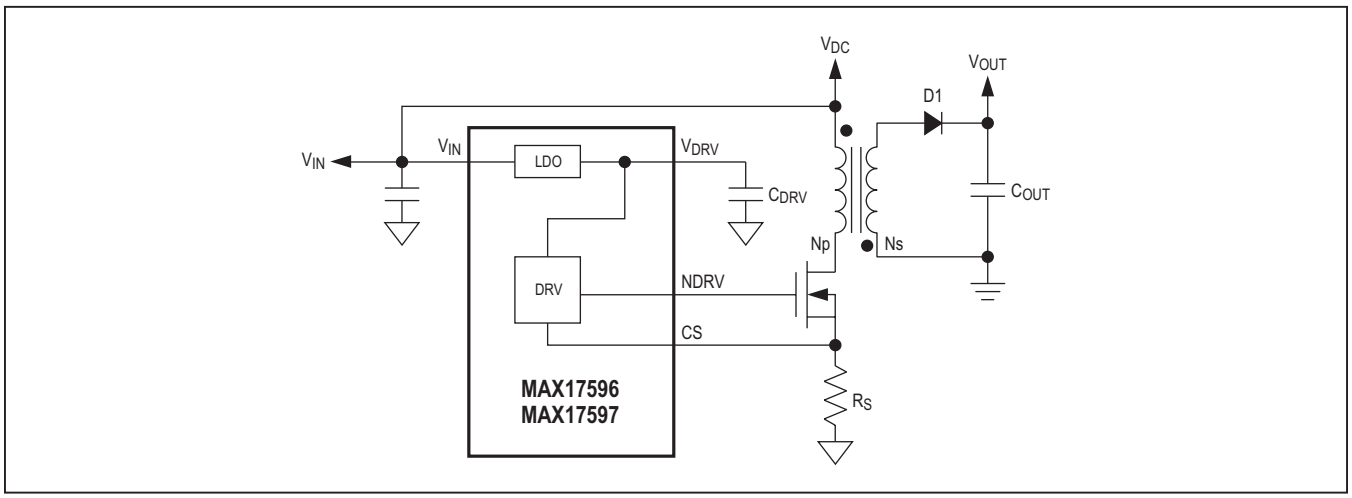


Figure 5. MAX17596/MAX17597 Typical Startup Circuit with V_{IN} Connected Directly to DC Input

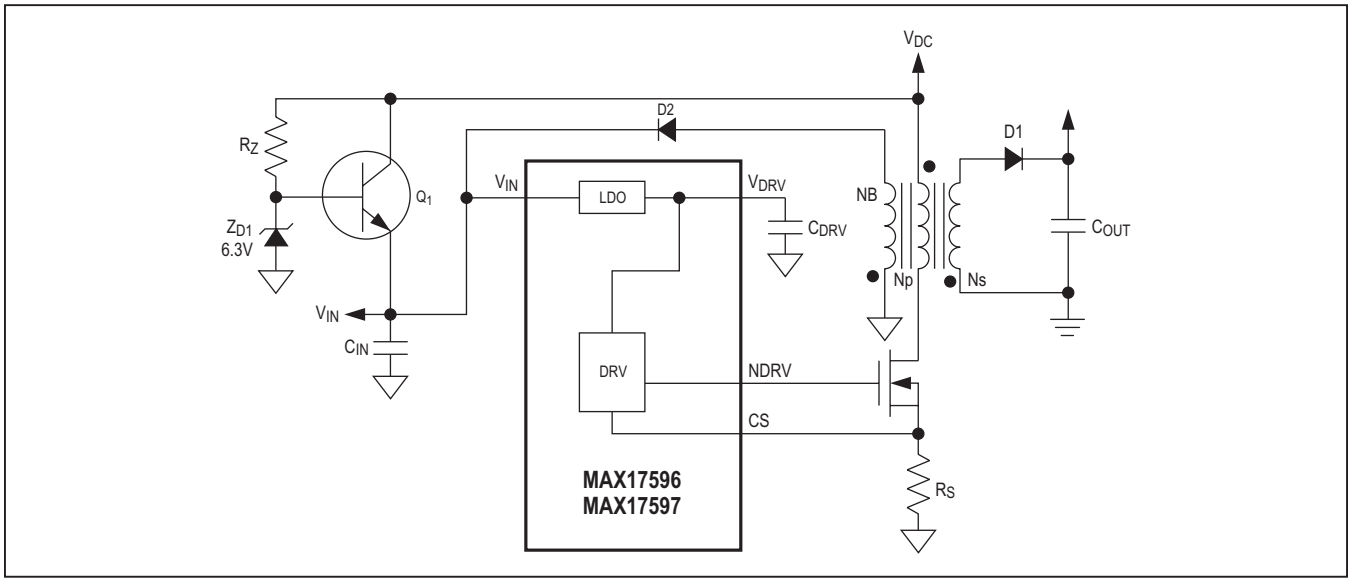


Figure 6. MAX17596/MAX17597 Typical Startup Circuit with Bias Winding to Turn Off Q1 and Reduce Power Dissipation

trip level ($V_{CS-PEAK}$) of 300mV. Use the following equation to calculate the value of R_{CS}:

$$R_{CS} = \frac{300mV}{I_{MOSFET}} \Omega$$

where I_{MOSFET} is the peak current flowing through the MOSFET.

The devices implement 65ns of leading-edge blanking to ignore leading-edge current spikes. Use a small RC network for additional filtering of the leading edge spike on the sense waveform when needed. Set the corner frequency between 10MHz and 20MHz. After the leading-edge blanking time, the device monitors V_{CS}. The switching cycle is terminated within 30ns from V_{CS} exceeding 300mV.

The devices offer a runaway current limit scheme that protects the devices under high-input-voltage short-circuit conditions when there is insufficient output voltage available to restore inductor current built up during the on period of the flyback/boost converter. Either eight consecutive occurrences of the peak-current-limit event or one occurrence of the runaway current limit trigger a hiccup mode that protects the converter by immediately suspending switching for a period of time (t_{RSTART}). This allows the overload current to decay due to power loss in the converter resistances, load, and the output diode of the flyback/boost converter before soft-start is attempted again. The runaway current limit is set at a $V_{CS-PEAK}$ of 360mV (typ). The peak-current-limit-triggered hiccup operation is disabled until the end of the soft-start period, while the runaway current-limit-triggered hiccup operation is always enabled.

Programming Slope Compensation (SLOPE)

The MAX17595/MAX17596 operate at a maximum duty cycle of 49%. In theory, they do not require slope compensation to prevent subharmonic instability that occurs naturally in continuous-conduction mode (CCM) peak-current-mode-controlled converters operating at duty cycles greater than 50%. In practice, the MAX17595/MAX17596 require a minimum amount of slope compensation to provide stable operation. The devices allow the user to program this default value of slope compensation simply by leaving the SLOPE pin unconnected. It is recommended that discontinuous-mode designs also use this minimum amount of slope compensation to provide better noise immunity and jitter-free operation.

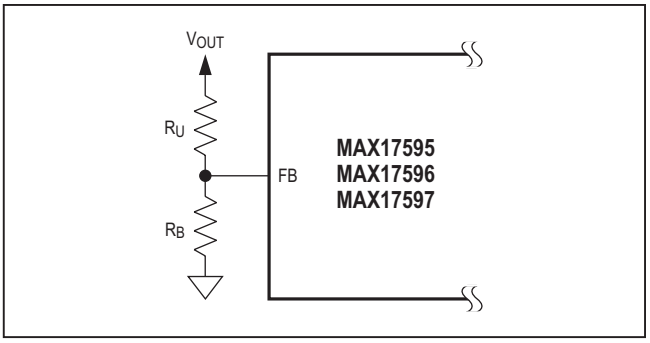


Figure 7. Programming Output Voltage

The MAX17597 flyback/boost converter can be designed to operate in either discontinuous-conduction mode (DCM) or to enter into continuous-conduction mode at a specific load condition for a given DC input voltage. In continuous-conduction mode, the flyback/boost converter needs slope compensation to avoid subharmonic instability that occurs naturally over all specified load and line conditions in peak-current-mode-controlled converters operating at duty cycles greater than 50%. A minimum amount of slope signal is added to the sensed current signal even for converters operating below 50% duty to provide stable, jitter-free operation. The SLOPE pin allows the user to program the necessary slope compensation by setting the value of the resistor (R_{SLOPE}) connected from the SLOPE pin to ground.

$$R_{SLOPE} = \frac{S_E - 8}{1.55} k\Omega$$

where the slope (S_E) is expressed in mV/µs.

Frequency Dithering for Spread-Spectrum Applications (Low EMI)

The switching frequency of the converter can be dithered in a range of ±10% by connecting a capacitor from DITHER/SYNC to SGND, and a resistor from DITHER to RT as shown in the *Typical Operating Circuits*. This results in lower EMI.

A current source at DITHER/SYNC charges capacitor C_{DITHER} to 2V at 50µA. Upon reaching this trip point, it discharges C_{DITHER} to 0.4V at 50µA. The charging and discharging of the capacitor generates a triangular waveform on DITHER/SYNC with peak levels at 0.4V and 2V and a frequency that is equal to:

$$f_{TRI} = \frac{50\mu A}{C_{DITHER} \times 3.2V}$$

typically, f_{TRI} should be set close to 1kHz. Resistor R_{DITHER} connected from DITHER/SYNC to RT determines the amount of dither as follows:

$$\%DITHER = \frac{R_{RT}}{R_{DITHER}}$$

where %DITHER is the amount of dither expressed as a percentage of the switching frequency. Setting R_{DITHER} to 10 x R_{RT} generates ±10% dither.

Synchronization (SYNC)

The internal oscillator can be synchronized to an external clock by applying the clock to the DITHER/SYNC pin directly. The external clock frequency can be set anywhere between 1.1x and 1.8x times the programmable switching frequency for the MAX17595/MAX17596. The synchronization feature is not available in the MAX17597. An external clock increases the maximum duty cycle by a factor of (f_{SYNC} / f_{SW}).

Error Amplifier and Loop Compensation

The MAX17595/MAX17596/MAX17597 include an internal transconductance error amplifier. The noninverting input of the error amplifier is internally connected to the internal reference and the inverting input is brought out at the FB pin to apply the feedback signal. The internal reference is linearly ramped up from 0V to 1.21V (typ) when the device is enabled at turn-on. After soft-start, the internal reference is connected to the bandgap.

In isolated applications, where an optocoupler is used to transmit the control signal from the secondary side, the emitter current of the optocoupler flows through a resistor to ground to set up the feedback voltage. A shunt regulator is usually employed as a secondary-side error amplifier to drive the optocoupler photodiode to couple the control signal to the primary. The loop compensation is applied in the secondary side as an R-C network on the shunt regulator. The MAX17595/MAX17596/MAX17597 error amp can be set up as a proportional gain amplifier, or used to implement additional poles or zeros. The *Typical Application Circuits* for the MAX17595/MAX17596 use the internal error amplifier as a proportional gain amplifier.

In nonisolated applications, the output voltage is divided down with a voltage-divider to ground and is applied to the FB pin. Loop compensation is applied at the COMP pin as an R-C network from COMP to GND that implements the required poles and zeros, as shown in Figure 8. The boost converter application circuit of Figure 11 for the MAX17597 uses this approach.

Layout, Grounding and Bypassing

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents in high-frequency-switching power converters. This implies that the loop areas for forward and return pulsed currents in various parts of the circuit should be minimized. Additionally, small current loop areas reduce radiated EMI. Similarly, the heatsink of the MOSFET presents a dV/dt source; therefore, the surface area of the MOSFET heatsink should be minimized as much as possible.

Ground planes must be kept as intact as possible. The ground plane for the power section of the converter should be kept separate from the analog ground plane, except for a connection at the least noisy section of the power ground plane, typically the return of the input filter capacitor. The negative terminal of the filter capacitor, the ground return of the power switch and current-sensing resistor, must be close together. PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the part for efficient heat dissipation. For a sample layout that ensures first-pass success, refer to the MAX17595 evaluation kit layout available at **www.maximintegrated.com**. For universal AC input designs, follow all applicable safety regulations. Offline power supplies can require UL, VDE, and other similar agency approvals.

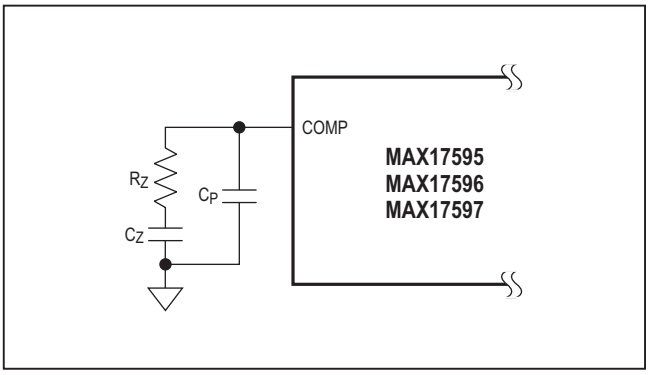


Figure 8. Error-Amplifier Compensation Network

Typical Operating Circuits

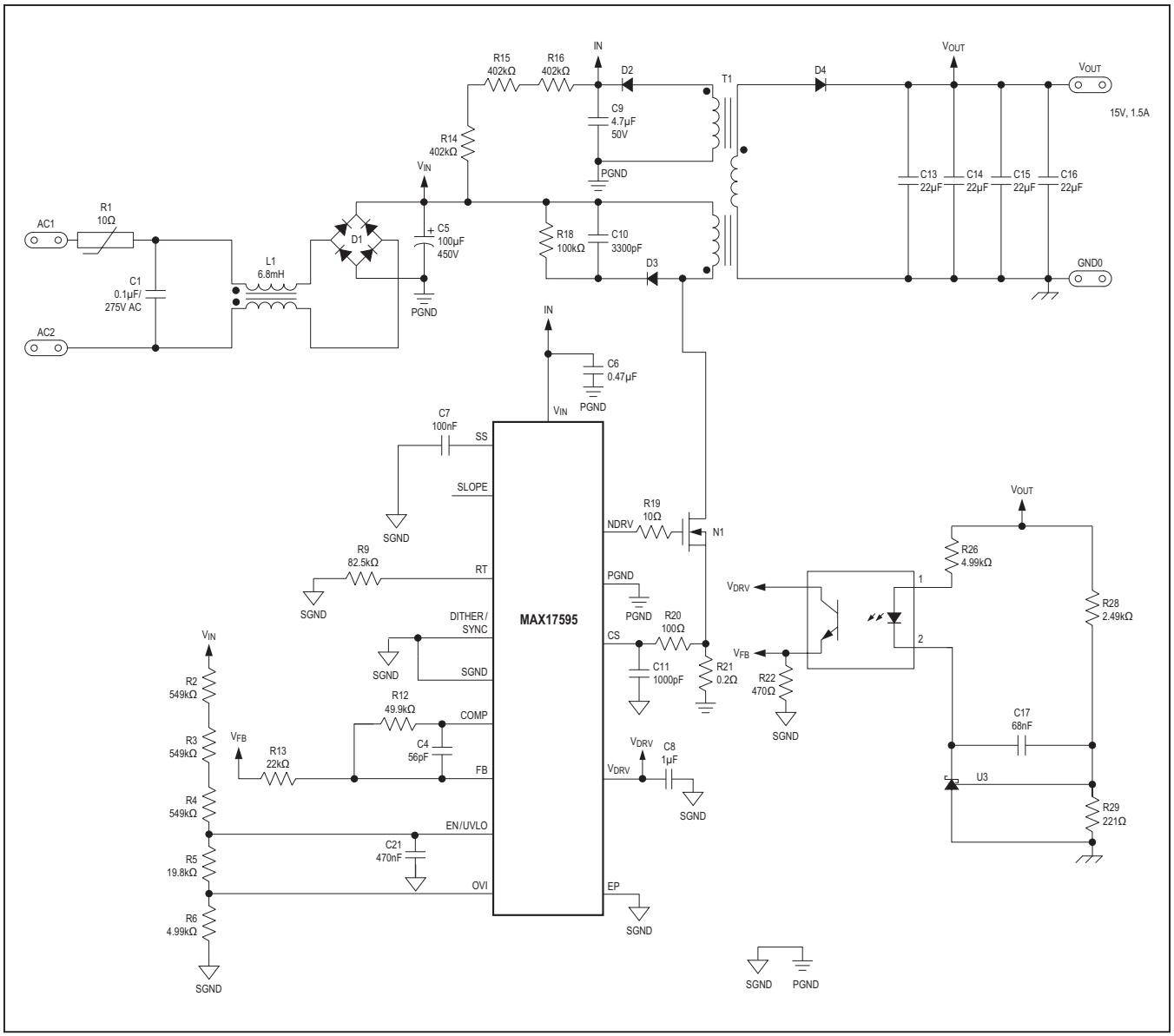


Figure 9. MAX17595 Typical Application Circuit (Universal Offline Isolated Power Supply)

Typical Operating Circuits (continued)

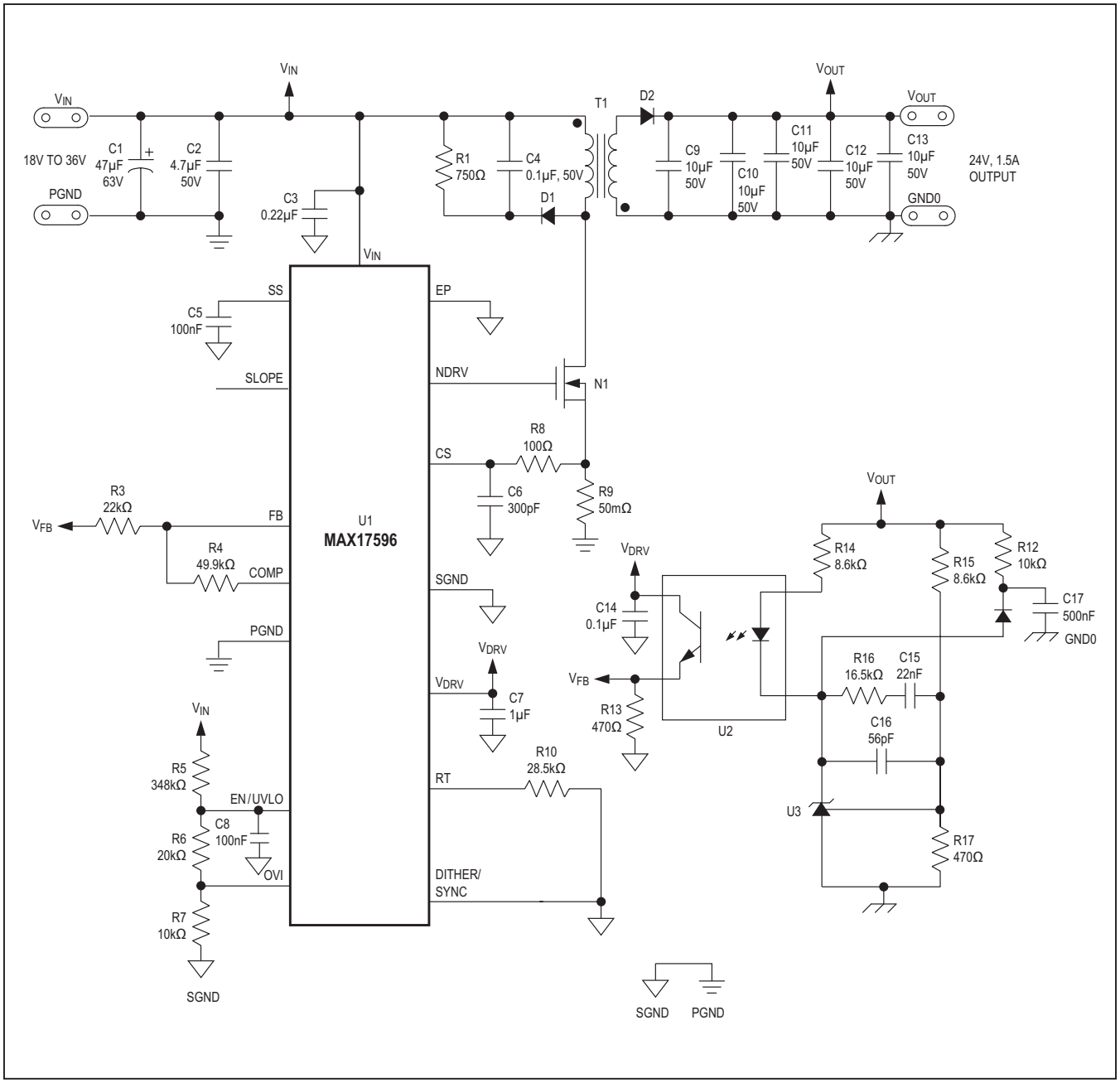


Figure 10. MAX17596 Typical Application Circuit (Power Supply for DC-DC Applications)

Typical Operating Circuits (continued)

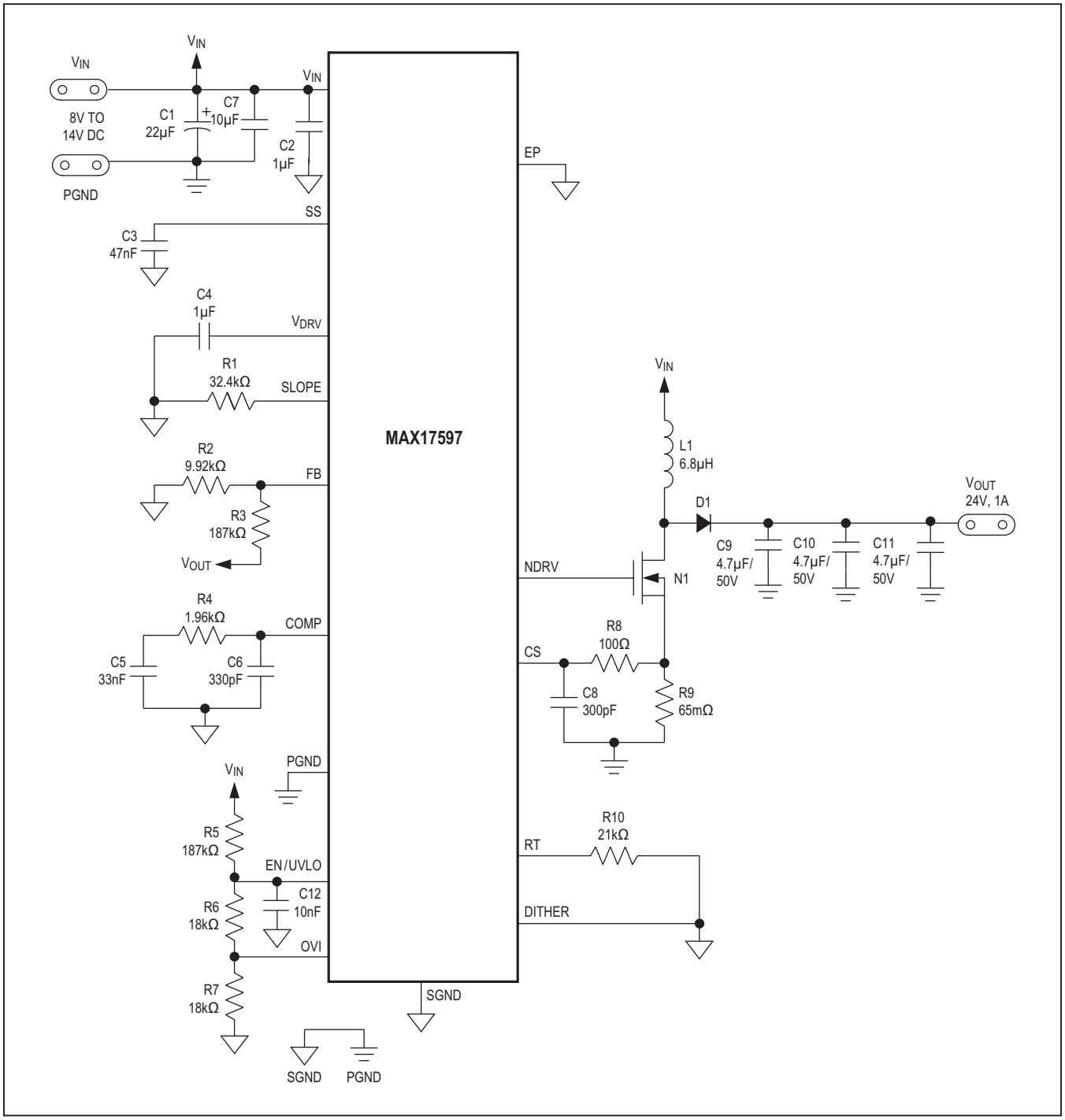


Figure 11. MAX17597 Typical Application Circuit (Nonsynchronous Boost Converter)

Ordering Information/Selector Guide

PART	TEMP RANGE	PIN PACKAGE	FUNCTIONALITY	UVLO, V_{IN} CLAMP	D_{MAX}
MAX17595ATE+	-40°C to +125°C	16 TQFN-EP*	Offline Flyback Controller	20V, Yes	46%
MAX17596ATE+	-40°C to +125°C	16 TQFN-EP*	Low-Voltage DC-DC Flyback Controller	4V, No	46%
MAX17597ATE+	-40°C to +125°C	16 TQFN-EP*	Boost Controller	4V, No	93%

+Denotes a lead(Pb)-free/RoHS-compliant package.
**Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN	T1633+4	**21-0136**	**90-0032**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/12	Initial release	—
1	2/13	Updated *General Description*, *Electrical Characteristics* tables, *Typical Operating Characteristics*; *Detailed Description*, *Figures 1, 3–6*; *Typical Operating Circuits*, deleted sections relating to soft-stop, flyback, and boost.	1–22
2	6/13	Updated *Pin Description* for EP and *Figure 10*	10, 19
3	11/14	Deleted automotive reference in *Applications* section	1
4	5/15	Updated *Benefits and Features* section	1
5	5/17	Added reference to App Note and modified pin description	1, 9,