1-Cell to 3-Cell, High-Power (1.5A), Low-Noise, Step-Up DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

OUT, $\overline{ON}$, AO, POK to GND .....-0.3V to +6V
PGND to GND.....±0.3V
LXP, LXN to PGND .....-0.3V to (V_{POUT} + 0.3V)
POUT, CLK/SEL, AIN, REF, FB,
POKIN to GND.....-0.3V to (V_{OUT} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Narrow SO (derate 8.70mW/°C above +70°C) 696mW

Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(CLK/SEL = AIN = $\overline{ON}$ = POKIN = FB = PGND = GND, OUT = POUT, LXP = LXN, V_{OUT} = 5.3V (Note 1), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC-DC CONVERTER						
Input Supply Range	(Note 2)			0.7	5.5	V
Minimum Start-Up Voltage	I_{LOAD} < 1mA, T_A = +25°C (Note 3)			0.9	1.1	V
Frequency in Start-Up Mode	V_{OUT} = 1.5V		40	140	300	kHz
Output Voltage (Note 4)	V_{FB} < 0.1V, CLK/SEL = OUT, 0 ≤ I_{LX} ≤ 1.1A, V_{BATT} = 3.7V		4.87	5.05	5.20	V
FB Regulation Voltage	Adjustable output, CLK/SEL = OUT, 0 ≤ I_{LX} ≤ 1.1A, V_{BATT} = 2.2V, V_{OUT} = 3.3V		1.21	1.24	1.255	V
FB Input Current	V_{FB} = 1.25V			0.1	20	nA
Output Voltage Adjust Range			2.5		5.5	V
Output Voltage Lockout Threshold	(Note 5)		2.0	2.15	2.3	V
Load Regulation (Note 6)	CLK/SEL = OUT, no load to full load			-1.6		%
Supply Current in Shutdown	$\overline{ON}$ = OUT			0.1	20	µA
Supply Current in Low-Power Mode	CLK/SEL = GND (Note 1)			65	120	µA
Supply Current in Low-Noise Mode	CLK/SEL = OUT (Note 1)			150	300	µA
DC-DC SWITCHES						
POUT, LXP Leakage Current	V_{LXP} = 0V, V_{OUT} = $V_{\overline{ON}}$ = 5.5V			0.1	20	µA
LXN Leakage Current	$V_{\overline{ON}}$ = V_{LXN} = V_{OUT} = 5.5V			0.1	20	µA
Switch On-Resistance	N-channel	CLK/SEL = GND		0.14	0.25	Ω
		CLK/SEL = OUT		0.075	0.13	
	P-channel			0.13	0.25	
N-Channel Current Limit	CLK/SEL = OUT		2200	2700	3200	mA
	CLK/SEL = GND		500	800	1100	mA
P-Channel Turn-Off Current	CLK/SEL = GND		20	160	260	mA
POWER-GOOD COMPARATOR						
POKIN Trip Level	Rising V_{POKIN}		1.225	1.250	1.275	V
POKIN Input Current	V_{POKIN} = 0.7V		-20		20	nA
POK Low Voltage	I_{SINK}(POK) = 1mA, V_{OUT} = 3.6V or I_{SINK}(POK) = 20µA, V_{OUT} = 1V			0.03	0.4	V
POK High Leakage Current	V_{OUT} = V_{POK} = 5.5V			0.01	1	µA

ELECTRICAL CHARACTERISTICS (continued)

(CLK/SEL = AIN = $\overline{ON}$ = POKIN = FB = PGND = GND, OUT = POUT, LXP = LXN, V_{OUT} = 5.3V (Note 1), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GAIN BLOCK					
AIN Reference Voltage	I_{AO} = 20µA	1.237	1.25	1.263	V
AIN Input Current	V_{AIN} = 1.5V	-30		30	nA
Transconductance	10µA < I_{AO} < 100µA	5	10	16	mmho
AO Output Low Voltage	V_{AIN} = 0.5V, I_{AO} = 100µA		0.1	0.4	V
AO Output High Leakage	V_{AIN} = 1.5V, V_{AO} = 5.5V		0.01	1	µA
REFERENCE					
Reference Output Voltage	I_{REF} = 0µA	1.237	1.250	1.263	V
REF Load Regulation	-1µA < I_{REF} < 50µA		5	15	mV
REF Supply Rejection	2.5V < V_{OUT} < 5.5V		0.2	5	mV
LOGIC INPUTS					
Input Low Voltage	$\overline{ON}$, 1.2V < V_{OUT} < 5.5V (Note 7)			0.2V_{OUT}	V
	CLK/SEL, V_{OUT} = 2.5V			0.2V_{OUT}	
Input High Voltage	$\overline{ON}$, 1.2V < V_{OUT} < 5.5V	0.8V_{OUT}			V
	CLK/SEL, V_{OUT} = 5.5V	0.8V_{OUT}			
Logic Input Current	$\overline{ON}$, CLK/SEL	-1	0.01	1	µA
Internal Oscillator Frequency	CLK/SEL = OUT, V_{FB} = 0.5V	260	300	340	kHz
Oscillator Maximum Duty Cycle	CLK/SEL = OUT, V_{FB} = 0.5V	80	86	90	%
External Clock Frequency Range		200		400	kHz
Minimum CLK/SEL Pulse Width			200		ns
Maximum CLK/SEL Rise/Fall Time			100		ns

ELECTRICAL CHARACTERISTICS

(CLK/SEL = AIN = $\overline{ON}$ = POKIN = FB = PGND = GND, OUT = POUT, LXP = LXN, V_{OUT} = 5.3V (Note 1), **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 8)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC-DC CONVERTER					
Output Voltage (Note 4)	V_{FB} < 0.1V, CLK/SEL = OUT, 0 ≤ I_{LX} ≤ 1.1A, V_{BATT} = 3.7V	4.87		5.20	V
FB Regulation Voltage	Adjustable output, CLK/SEL = OUT, 0 ≤ I_{LX} ≤ 1.1A, V_{OUT} = 3.3V, V_{BATT} = 2.2V	1.20		1.27	V
Output Voltage Lockout Threshold	(Note 5)	2.0		2.3	V
Supply Current in Shutdown	$\overline{ON}$ = OUT			20	µA
Supply Current in Low-Power Mode	CLK/SEL = GND (Note 1)			120	µA
Supply Current in Low-Noise Mode	CLK/SEL = OUT (Note 1)			300	µA

1-Cell to 3-Cell, High-Power (1.5A), Low-Noise, Step-Up DC-DC Converter

ELECTRICAL CHARACTERISTICS (continued)

(CLK/SEL = AIN = $\overline{ON}$ = POKIN = FB = PGND = GND, OUT = POUT, LXP = LXN, V_{OUT} = 5.3V (Note 1), **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 8)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC-DC SWITCHES						
Switch On-Resistance	N-channel	CLK/SEL = GND			0.25	Ω
		CLK/SEL = OUT			0.13	
	P-channel				0.25	
N-Channel Current Limit	CLK/SEL = OUT		2200		3600	mA
	CLK/SEL = GND		500		1100	mA
POWER-GOOD COMPARATOR						
POKIN Trip Level	Rising V_{POKIN}		1.225		1.275	V
GAIN BLOCK						
AIN Reference Voltage	I_{AO} = 20µA		1.23		1.27	V
Transconductance	10µA < I_{AO} < 100µA		5		16	mmho
REFERENCE						
Reference Output Voltage	I_{REF} = 0µA		1.23		1.27	V
LOGIC INPUTS						
Internal Oscillator Frequency	CLK/SEL = OUT, V_{FB} = 0.5V		260		340	kHz
Oscillator Maximum Duty Cycle	CLK/SEL = OUT, V_{FB} = 0.5V		80		92	%

Note 1: Supply current from the 5.05V output is measured between the 5.05V output and the OUT pin. This current correlates directly to the actual battery supply current, but is reduced in value according to the step-up ratio and efficiency. Set V_{OUT} = 5.3V to keep the internal switch open when measuring the device operating current.

Note 2: Minimum operating voltage. Since the regulator is bootstrapped to the output, once started it will operate down to a 0.7V input.

Note 3: Start-up is tested with the circuit of Figure 2.

Note 4: In low-power mode (CLK/SEL = GND) the output voltage regulates 1% higher than low-noise mode (CLK/SEL = OUT or synchronized).

Note 5: The regulator is in start-up mode until this voltage is reached. Do not apply full-load current below this voltage.

Note 6: Load regulation is measured from no-load to full load, where full load is determined by the N-channel switch current limit.

Note 7: The $\overline{ON}$ input has a total hysteresis of approximately 0.15 x V_{OUT}.

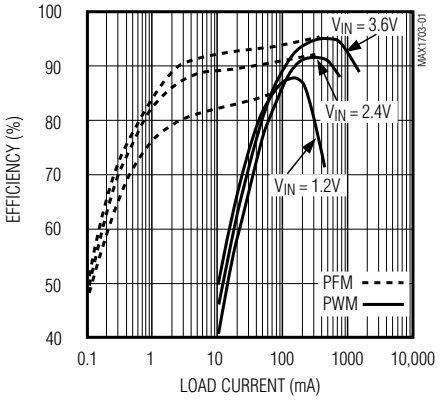
Note 8: Specifications to -40°C are guaranteed by design and not production tested.

1-Cell to 3-Cell, High-Power (1.5A), Low-Noise, Step-Up DC-DC Converter

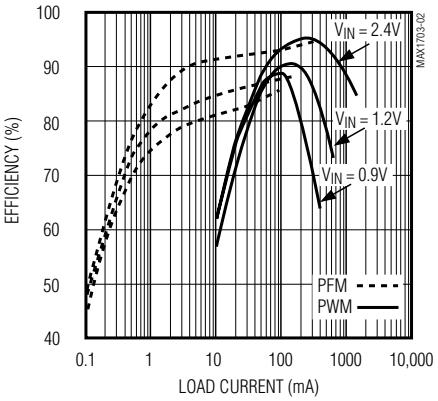
Typical Operating Characteristics

(V_{IN} = +3.6V, V_{OUT} = 5V, T_A = +25°C, unless otherwise noted.)

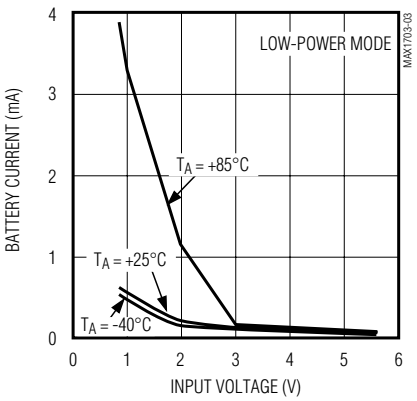
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 5V)



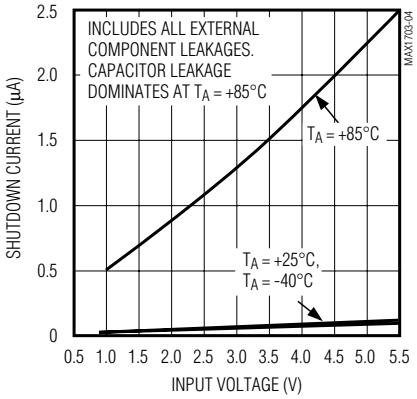
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 3.3V)



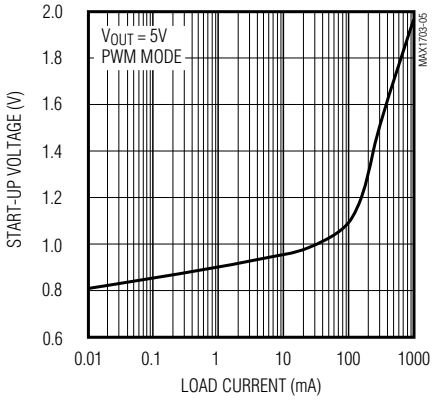
NO-LOAD BATTERY CURRENT vs. INPUT VOLTAGE



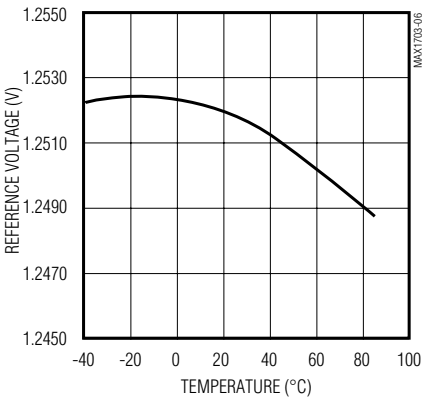
SHUTDOWN SUPPLY CURRENT vs. INPUT VOLTAGE



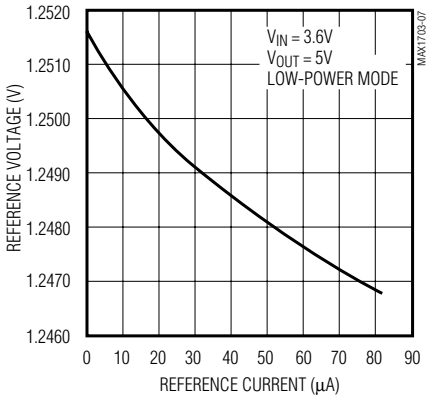
START-UP VOLTAGE vs. LOAD CURRENT



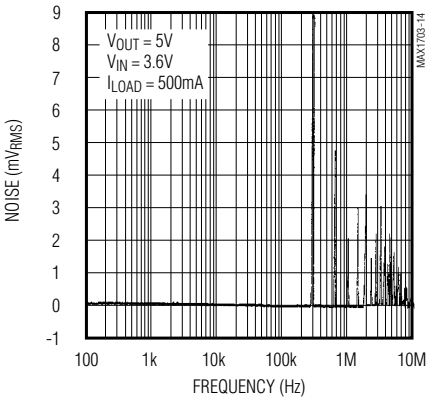
REFERENCE VOLTAGE vs. TEMPERATURE



REFERENCE VOLTAGE vs. REFERENCE CURRENT



NOISE SPECTRUM

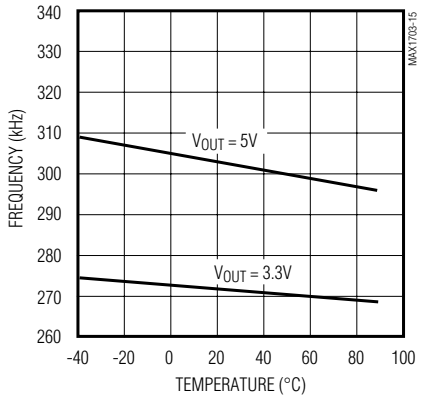


1-Cell to 3-Cell, High-Power (1.5A), Low-Noise, Step-Up DC-DC Converter

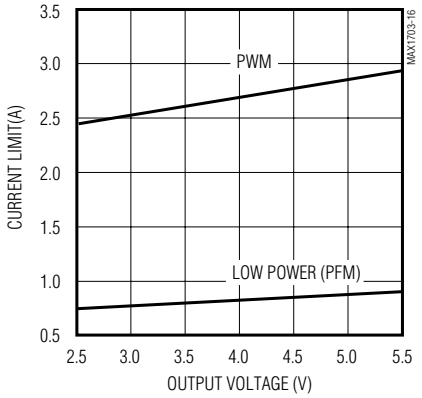
Typical Operating Characteristics (continued)

(V_{IN} = +3.6V, V_{OUT} = 5V, T_A = +25°C, unless otherwise noted.)

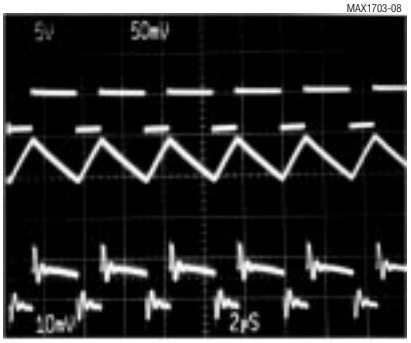
FREQUENCY vs. TEMPERATURE



PEAK INDUCTOR CURRENT LIMIT vs. OUTPUT VOLTAGE



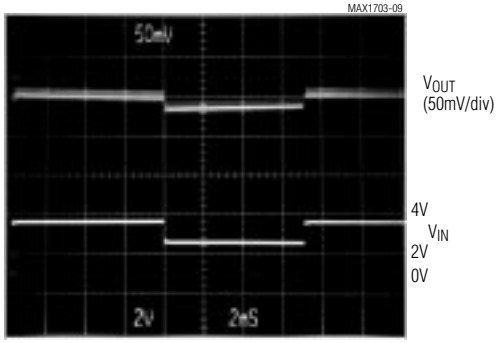
HEAVY LOAD SWITCHING



2µs/div

I_{LOAD} = 1.5A, C7 = 0.47µF

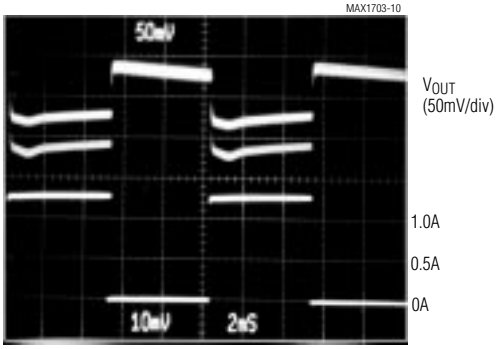
LINE-TRANSIENT RESPONSE



2ms/div

V_{IN} = 2.6V TO 3.6V, V_{OUT} IS AC COUPLED

LOAD-TRANSIENT RESPONSE

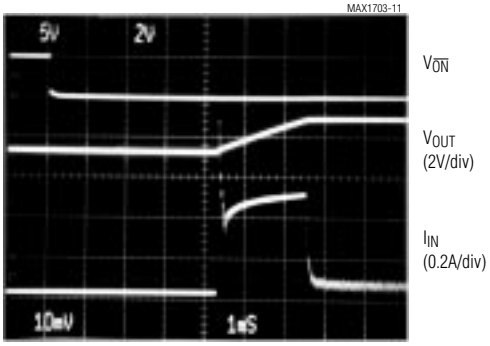


2ms/div

V_{OUT} IS AC COUPLED

LOAD CURRENT = 0A TO 1.5A

POWER-ON DELAY (PFM MODE)



1ms/div

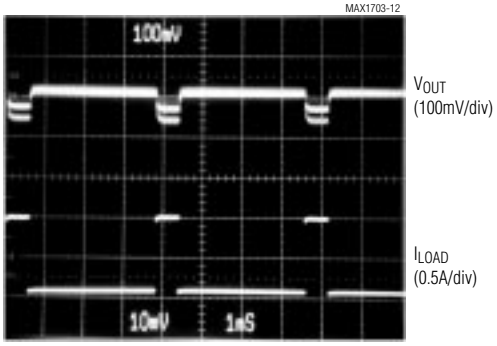
V_{IN} = 2.6V TO 3.6V, V_{OUT} IS AC COUPLED

1-Cell to 3-Cell, High-Power (1.5A), Low-Noise, Step-Up DC-DC Converter

Typical Operating Characteristics (continued)

(V_{IN} = +3.6V, V_{OUT} = 5V, T_A = +25°C, unless otherwise noted.)

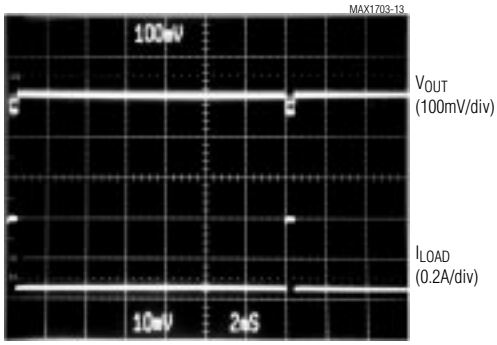
GSM LOAD-TRANSIENT RESPONSE



1ms/div

V_{IN} = 3.6V, V_{OUT} = 5V, C_{OUT} = 470µF,
PULSE WIDTH = 577µs, LOAD CURRENT = 100mA TO 1A

DECT LOAD-TRANSIENT RESPONSE



2ms/div

V_{IN} = 1.2V, V_{OUT} = 3.3V, C_{OUT} = 470µF,
PULSE WIDTH = 416µs, LOAD CURRENT = 50mA TO 400mA

Pin Description

PIN	NAME	FUNCTION
1	REF	Reference Output. Bypass with a 0.22µF bypass capacitor to GND.
2	FB	Dual-Mode™ Feedback Input. Connect FB to ground to set a fixed output voltage of +5V. Connect a divider between the output voltage and GND to set the output voltage from 2.5V to 5.5V.
3	POKIN	Power-Good Comparator Input. Threshold is 1.250V, with 1% hysteresis on the threshold's rising edge.
4	OUT	DC-DC Converter Output. Power source for the IC.
5	GND	Ground
6	AIN	Gain-Block Input. When AIN is low, AO sinks current. The nominal transconductance from AIN to AO is 10mmhos.
7	AO	Gain-Block Output. This open-drain output sinks current when $V_{AIN} < V_{REF}$.
8	POK	Power-Good Comparator Output. This open-drain N-channel output is low when $V_{POKIN} < 1.250V$.
9	CLK/SEL	Switch-Mode Selection and External-Clock Synchronization Input: • CLK/SEL = Low: Low-power, low-quiescent-current PFM mode. Delivers up to 10% of full load current. • CLK/SEL = High: High-power PWM mode. Full output power available. Operates in low-noise, constant-frequency mode. • CLK/SEL = External Clock: High-power PWM mode with the internal oscillator synchronized to the external CLK Turning on with CLK/SEL = 0V also serves as a soft-start function, since peak inductor current is limited to 25% of that allowed in PWM mode.
10, 12	PGND	Source of N-Channel Power MOSFET Switch
11	LXN	Drain of N-Channel Power Switch. Connect LXP to LXN.
13, 15	POUT	Source of P-Channel Synchronous Rectifier MOSFET Switch. Connect an external Schottky diode from LXN and LXP to POUT.
14	LXP	Drain of P-Channel Synchronous Rectifier. Connect LXP to LXN.
16	$\overline{ON}$	On/Off Input. When $\overline{ON}$ is low, the IC turns on.

Dual Mode is a trademark of Maxim Integrated Products.

1-Cell to 3-Cell, High-Power (1.5A), Low-Noise, Step-Up DC-DC Converter

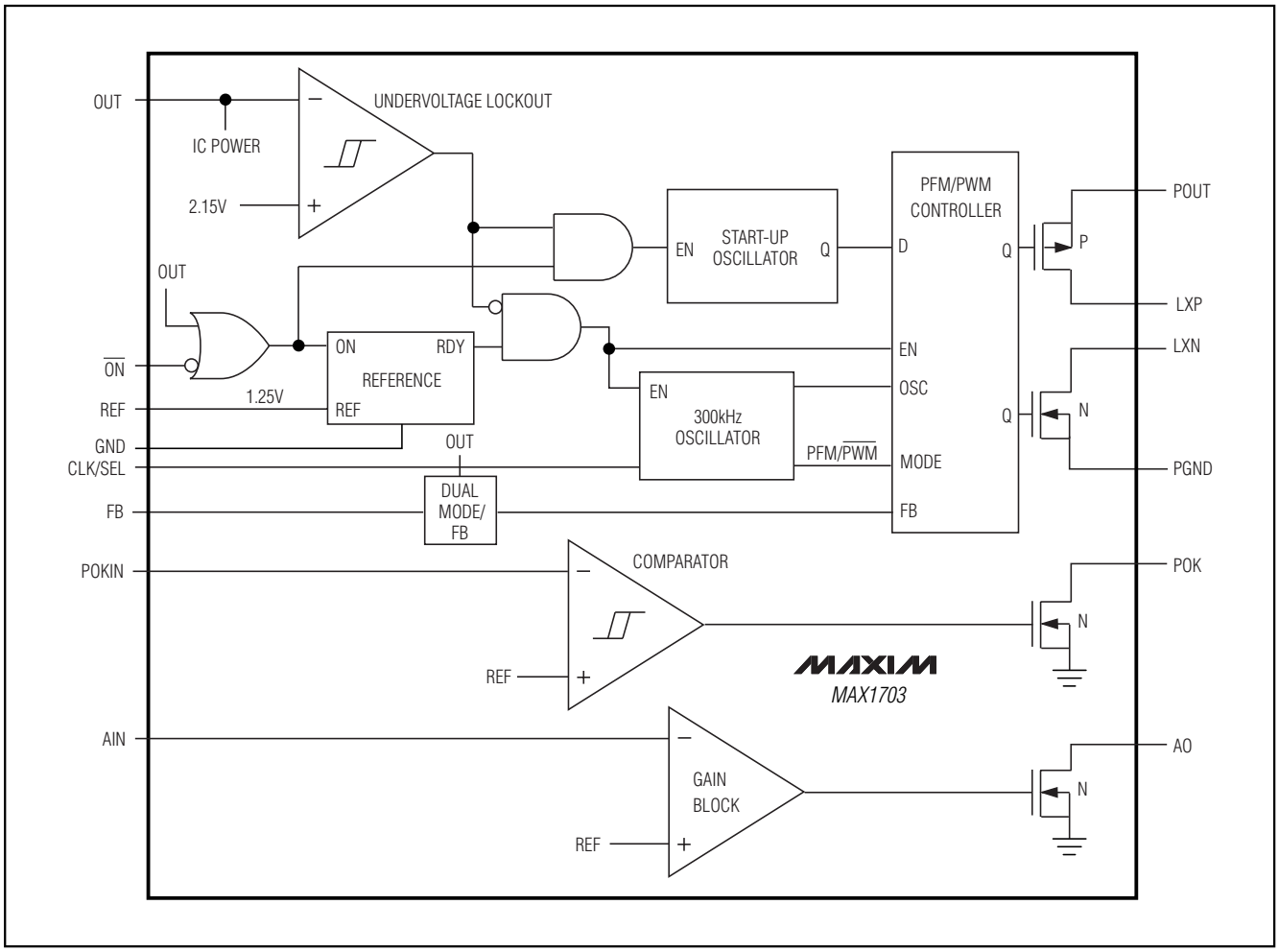


Figure 1. Functional Block Diagram

Detailed Description

The MAX1703 is a highly efficient, low-noise power supply for portable RF and data-acquisition instruments. It combines a boost switching regulator, N-channel power MOSFET, P-channel synchronous rectifier, precision reference, shutdown control, versatile gain block, and power-good (POK) comparator (Figure 1) in a 16-pin narrow SO package.

The switching DC-DC converter boosts a 1- to 3-cell input to a fixed 5V or an adjustable output between 2.5V and 5.5V. Typically the MAX1703 starts from a low, 0.9V input and remains operational down to 0.7V.

The MAX1703 is optimized for use in cellular phones and other applications requiring low noise during full-power operation, as well as low quiescent current for maximum battery life in low-power mode and shutdown. It features constant-frequency (300kHz), low-noise PWM operation with up to 1.5A output capability. See Table 1 for typical outputs. A low-quiescent-current, low-power mode offers an output up to 150mA and reduces quiescent power consumption to 300µW. In shutdown mode, the quiescent current is further reduced to just 1µA. Figure 2 shows the standard application circuit for the MAX1703.

Table 1. Typical Available Output Current

NO. OF CELLS	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (mA)
1 NiCd/NiMH	1.2	3.3	600
2 NiCd/NiMH	2.4	3.3	1400
	2.4	5.0	950
3 NiCd/NiMH	3.6	5.0	1600

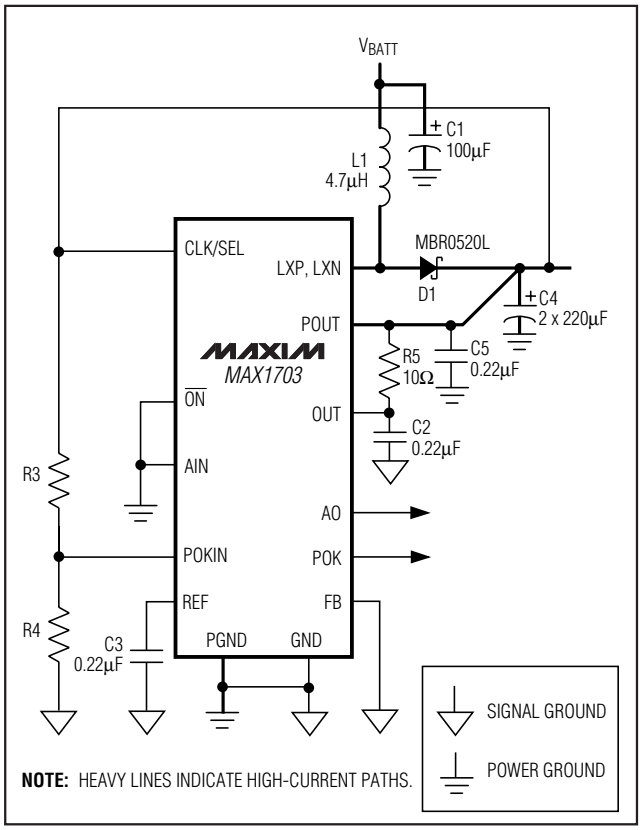


Figure 2. MAX1703 in High-Power PWM Mode

Additional features include synchronous rectification for high efficiency and improved battery life, and an uncommitted comparator (POK) for monitoring the regulator's output or battery voltage. The MAX1703 also includes a gain block that can be used to build a linear regulator using an external P-channel MOSFET pass device; this gain block can also function as a second comparator. A CLK input allows frequency synchronization to reduce interference.

Table 2. Selecting the Operating Mode

CLK/SEL	MODE	FEATURES
0	Low power	Low supply current
1	PWM	Low noise, high output current
External Clock (200kHz to 400kHz)	Synchronized PWM	Low noise, high output current

Step-Up Converter

The step-up switching DC-DC converter generates an adjustable output from 2.5V to 5.5V. The internal N-channel MOSFET switch is turned on during the first part of each cycle, allowing current to ramp up in the inductor and store energy in a magnetic field. During the second part of each cycle, when the MOSFET is turned off, the voltage across the inductor reverses and forces current through the diode and synchronous rectifier to the output filter capacitor and load. As the energy stored in the inductor is depleted, the current ramps down and the output diode and synchronous rectifier turn off. Depending on the CLK/SEL pin setting, voltage across the load is regulated using either low-noise PWM or low-power operation (Table 2).

Low-Noise PWM Operation

When CLK/SEL is pulled high, the MAX1703 operates in a high-power, low-noise PWM mode. During PWM operation, the MAX1703 switches at a constant frequency (300kHz), and modulates the MOSFET-switch pulse width to control the power transferred per cycle and regulate the voltage across the load. In PWM mode the device can output up to 1.5A. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered. See the Noise Spectrum plot in the *Typical Operating Characteristics*.

During PWM operation, each of the internal clock's rising edges sets a flip-flop, which turns on the N-channel MOSFET switch (Figure 3). The switch turns off when the sum of the voltage-error, slope-compensation, and current-feedback signals trips a multi-input comparator and resets the flip-flop; the switch remains off for the rest of the cycle. When a change occurs in the output voltage error signal, the comparator shifts the level to which the inductor current ramps during each cycle. A second comparator enforces an inductor current limit of 2.7A (typical).

1-Cell to 3-Cell, High-Power (1.5A), Low-Noise, Step-Up DC-DC Converter

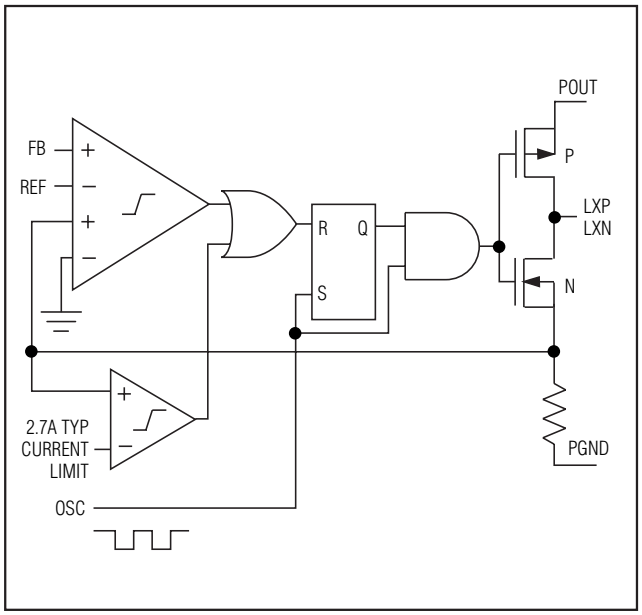


Figure 3. Simplified PWM Controller Block Diagram

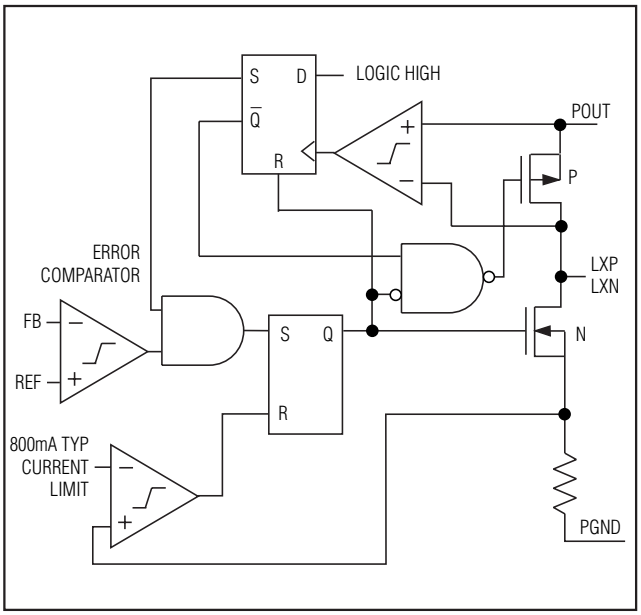


Figure 4. Controller Block Diagram in Low-Power PFM Mode

Synchronized PWM Operation

The MAX1703 can be synchronized in PWM mode to a 200kHz to 400kHz frequency by applying an external clock to CLK/SEL. This allows the user to set the harmonics to avoid IF bands in wireless applications. The synchronous rectifier is also active during synchronized PWM operation.

Low-Power PFM Operation

Pulling CLK/SEL low places the MAX1703 in a low-power mode. During low-power mode, PFM operation regulates the output voltage by transferring a fixed amount of energy during each cycle, and then modulating the pulse frequency to control the power delivered to the output. The devices switch only as needed to service the load, resulting in the highest possible efficiency at light loads. Output current capability in PFM mode is 150mA (max). The output voltage is typically 1% higher than in PWM mode.

During PFM operation, the error comparator detects the output voltage falling out of regulation and sets a flip-flop, which turns on the N-channel MOSFET switch (Figure 4). When the inductor current ramps to the PFM mode current limit (800mA typical) and stores a fixed amount of energy, the current-sense comparator resets a flip-flop. The flip-flop turns off the N-channel switch and turns on the P-channel synchronous rectifier. A second flip-flop, previously reset by the switch's "on" signal, inhibits the error comparator from initiating another cycle until the energy stored in the inductor is transferred to the output filter capacitor and the synchronous rectifier current has ramped down to 80mA. This forces operation with a discontinuous inductor current.

Synchronous Rectifier

The MAX1703 features an internal 140mΩ, P-channel synchronous rectifier to enhance efficiency. Synchronous rectification provides a 5% efficiency improvement over similar nonsynchronous boost regulators. In PWM mode, the synchronous rectifier is turned on during the second half of each switching cycle. In low-power mode, an internal comparator turns on the synchronous rectifier when the voltage at LX exceeds the boost regulator output, and then turns it off when the inductor current drops below 80mA.

Low-Voltage Start-Up Oscillator

The MAX1703 uses a CMOS, low-voltage start-up oscillator for a 1.1V guaranteed minimum start-up input voltage at +25°C. On start-up, the low-voltage oscillator switches the N-channel MOSFET until the output voltage reaches 2.15V. Above this level, the normal boost-converter feedback and control circuitry take over. Once the device is in regulation, it can operate down to a 0.7V input, since internal power for the IC is bootstrapped from the output via the OUT pin. Do not apply full load until the output exceeds 2.3V (max).

Shutdown

The MAX1703 shuts down to reduce quiescent current to 1µA. During shutdown ($\overline{ON}$ = V_{OUT}), the reference, low-battery comparator, gain block, and all feedback and control circuitry are off. The boost converter's output drops to one Schottky diode drop below the input.

Power-Good (POK) Comparator

The MAX1703 features an uncommitted POK comparator. The internal POK comparator has an open-drain output (POK) capable of sinking 1mA. When the input (POKIN) rises above the 1.25V reference, the POK open-drain output turns off. The POKIN input has 10mV of hysteresis.

To provide a power-good signal, connect the POKIN input to an external resistor-divider between OUT and GND (Figure 5). Calculate the resistor values as follows:

$$R3 = R4(V_{TH} / V_{REF} - 1)$$

where V_{TH} is the desired input voltage trip threshold.

Since the input bias current into POKIN is less than 20nA, R4 can be a large value (such as 270kΩ or less) without sacrificing accuracy. Connect the resistor voltage-divider as close to the IC as possible, within 0.2in. (5mm) of POKIN.

Reference

The MAX1703 has an internal 1.250V, 1% bandgap reference. Connect a 0.22µF bypass capacitor to GND within 0.2in. (5mm) of the REF pin. REF can source up to 50µA of external load current.

Gain Block

The MAX1703 gain block can function as a second comparator, or can be used to build a linear regulator using an external P-channel MOSFET pass device. The gain-block output is a single-stage transconductance amplifier that drives an open-drain N-channel MOSFET. The g_m of the entire gain-block stage is 10mmho. Figure 6 shows the gain block used in a linear-regulator application. The output of an external P-channel pass element is compared to the internal reference. The difference is amplified and used to drive the gate of the pass element. Use a logic-level PFET, such as an NDS336P ($R_{DS(ON)}$ = 270mΩ) from Fairchild. This configuration allows ripple reduction at the output. If a lower $R_{DS(ON)}$ PFET is used, then the linear regulator output filter capacitance may need to be increased.

To use the gain block as a comparator, refer to the *Power-Good (POK) Comparator* section.

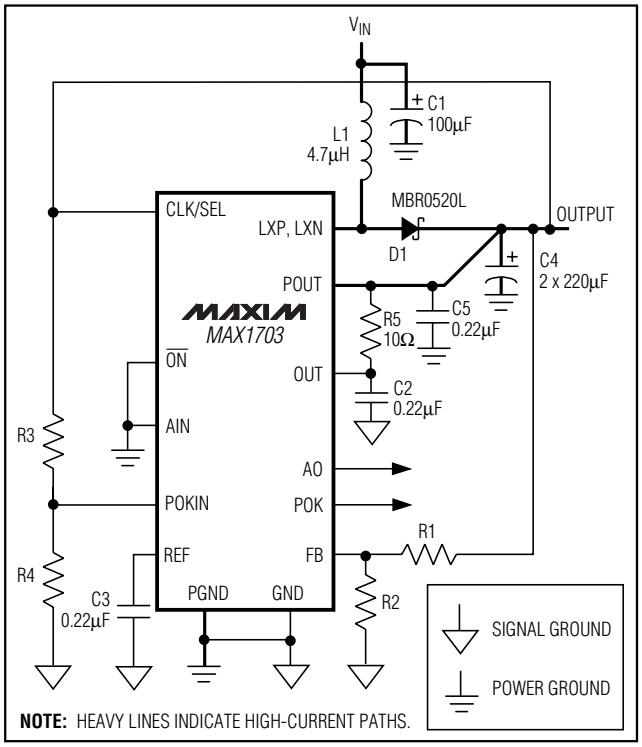


Figure 5. Adjustable Output (PWM Mode)

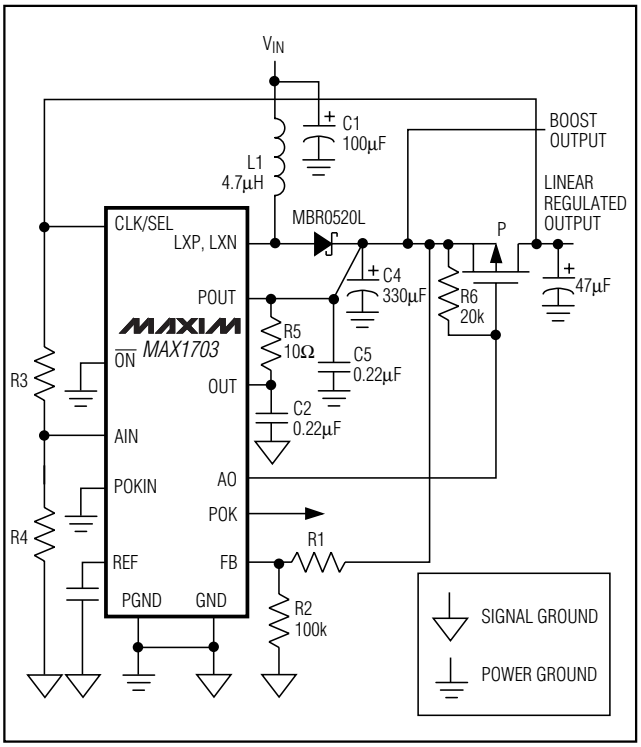


Figure 6. Using the Gain Block as a Linear Regulator

1-Cell to 3-Cell, High-Power (1.5A), Low-Noise, Step-Up DC-DC Converter

Table 3. Component Selection Guide

PRODUCTION	INDUCTORS	CAPACITORS	DIODES
Surface Mount	Sumida CDR125	Matsuo 267 series	Motorola MBR0520L
		Sprague 595D series	
	Coilcraft DO3316	AVX TPS series	
Through Hole	Sumida RCH654 series	Sanyo OS-CON series	1N5817
		Nichicon PL series	

Design Procedure

Setting the Output Voltages

Set the output voltage between 2.5V and 5.5V by connecting a resistor voltage-divider to FB from OUT to GND, as shown in Figure 2. The resistor values are then as follows:

$$R1 = R2(V_{OUT} / V_{FB} - 1)$$

where V_{FB}, the boost-regulator feedback setpoint, is 1.24V. Since the input bias current into FB is less than 20nA, R2 can have a large value (such as 270kΩ or less) without sacrificing accuracy. Connect the resistor voltage-divider as close to the IC as possible, within 0.2in. (5mm) of the FB pin.

Inductor Selection

The MAX1703's high switching frequency allows the use of a small surface-mount inductor. A 4.7µH inductor should have a saturation-current rating that exceeds the N-channel switch current limit. However, it is generally acceptable to bias the inductor current into saturation by as much as 20%, although this will slightly reduce efficiency. For high efficiency, choose an inductor with a high-frequency core material, such as ferrite, to reduce core losses. To minimize radiated noise, use a toroid, pot core, or shielded bobbin inductor. See Table 3 for suggested components and Table 4 for a list of component suppliers. Connect the inductor from the battery to the LX pins as close to the IC as possible.

Output Diode

Use a Schottky diode such as a 1N5817, MBR0520L, or equivalent. The Schottky diode carries current during both start-up and PFM mode after the synchronous rectifier turns off. Thus, its current rating only needs to be 500mA. Connect the diode between LXN/LXP and POUT, as close to the IC as possible. Do not use ordinary rectifier diodes, since slow switching speeds and long reverse recovery times will compromise efficiency and load regulation.

Table 4. Component Suppliers

SUPPLIER	PHONE	FAX
AVX	USA: (803) 946-0690 (800) 282-4975	(803) 626-3123
Coilcraft	USA: (847) 639-6400	(847) 639-1469
Matsuo	USA: (714) 969-2491	(714) 960-6492
Motorola	USA: (602) 303-5454	(602) 994-6430
Sanyo	USA: (619) 661-6835 Japan: 81-7-2070-6306	(619) 661-1055 81-7-2070-1174
Sumida	USA: (847) 956-0666 Japan: 81-3-3607-5111	(847) 956-0702 81-3-3607-5144

Input and Output Filter Capacitors

Choose input and output filter capacitors that will service the input and output peak currents with acceptable voltage ripple. Choose input capacitors with working voltage ratings over the maximum input voltage, and output capacitors with working voltage ratings higher than the output.

A 330µF, 100mΩ, low-ESR tantalum capacitor is recommended for a 5V output. For full output load current, one 470µF or two 220µF, 100mΩ low-ESR tantalum capacitors are recommended for a 3.3V output. The input filter capacitor (C_{IN}) also reduces peak currents drawn from the input source and reduces input switching noise. The input voltage source impedance determines the required size of the input capacitor.

When operating directly from one or two NiCd cells placed close to the MAX1703, use a 100µF, low-ESR input filter capacitor.

Sanyo OS-CON and Panasonic SP/CB-series ceramic capacitors offer the lowest ESR. Low-ESR tantalum capacitors are a good choice and generally offer a good tradeoff between price and performance. Do not exceed the ripple current ratings of tantalum capacitors. Avoid most aluminum-electrolytic capacitors, because their ESR is often too high.

1-Cell to 3-Cell, High-Power (1.5A), Low-Noise, Step-Up DC-DC Converter

Bypass Capacitors

A few ceramic bypass capacitors are required for proper operation. Bypass REF with a 0.22µF capacitor to GND. Connect a 0.22µF ceramic capacitor from OUT to GND. Each of these should be placed as close to their respective pins as possible, within 0.2in. (5mm) of the DC-DC converter IC. See Table 4 for suggested suppliers.

Applications Information

Intermittent Supply/Battery Connections

When boosting an input supply connected via a mechanical switch, or a battery connected via spring contacts, input power may sometimes be intermittent as a result of contact bounce. When operating in PFM mode with input voltages greater than 2.5V, restarting after such dropouts may initiate high current pulses that interfere with the MAX1703's internal MOSFET switch control. If contact or switch bounce is anticipated in the design, use one of the following solutions:

1) Connect a capacitor ($C_{\overline{ON}}$) from $\overline{ON}$ to V_{IN} and a 1MΩ resistor ($R_{\overline{ON}}$) from $\overline{ON}$ to GND, as shown in Figure 7. This resistor-capacitor network differentiates fast input edges at V_{IN} and momentarily holds the IC off until V_{IN} settles. The appropriate value of $C_{\overline{ON}}$ is 10^{-5} times the total output filter capacitance (C_{OUT}), so a C_{OUT} of 440µF results in $C_{\overline{ON}}$ = 4.7nF.
2) Use the system microcontroller to hold the MAX1703 in shutdown from the time when power is applied (or reapplied) until C_{OUT} has charged to at least the input voltage. Standard power-on-reset times accomplish this.
3) Ensure that the IC operates, or at least powers up, in PWM mode (CLK/SEL = high). Activate PFM mode only after the output voltage has settled and all of the system's power-on-reset flags are cleared.

Use in a Typical Wireless Phone Application

The MAX1703 is ideal for use in digital cordless and PCS phones. The power amplifier (PA) is connected directly to the boost-converter output for maximum voltage swing (Figure 8). Low-dropout linear regulators are used for post-regulation to generate low-noise power for DSP, control, and RF circuitry. Typically, RF phones spend most of their life in standby mode with only short periods in transmit/receive mode. During standby, maximize battery life by setting CLK/SEL = 0; this places the IC in low-power mode (for the lowest quiescent power consumption). See *Gain Block* section for information on configuring an external MOSFET as a linear regulator.

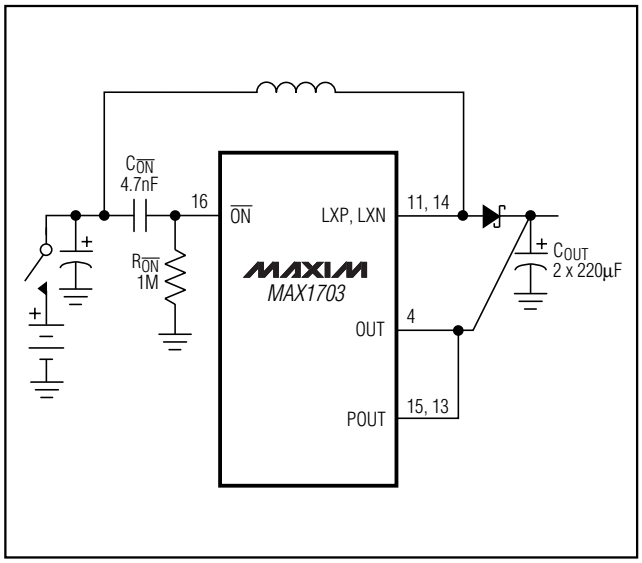


Figure 7. Connecting $C_{\overline{ON}}$ and $R_{\overline{ON}}$ when Switch or Battery-Contact Bounce is Anticipated

Designing a PC Board

High switching frequencies and large peak currents make PC board layout an important part of design. Poor design can cause excessive EMI and ground bounce, both of which can cause instability or regulation errors by corrupting the voltage and current feedback signals.

Power components—such as the inductor, converter IC, filter capacitors, and output diode—should be placed as close together as possible, and their traces should be kept short, direct, and wide. A separate low-noise ground plane containing the reference and signal grounds should only connect to the power-ground plane at one point. This minimizes the effect of power-ground currents on the part.

Keep the voltage feedback network very close to the IC, within 0.2in. (5mm) of the FB pins. Keep noisy traces, such as from the LX pin, away from the voltage feedback networks and separated from them using grounded copper. Consult the MAX1703 EV kit for a full PC board example.

Soft-Start

To implement soft-start, set CLK/SEL low on power-up; this forces PFM operation and reduces the peak switching current to 800mA max. Once the circuit is in regulation and start-up transients have settled, CLK/SEL can be set high for full-power operation.

1-Cell to 3-Cell, High-Power (1.5A), Low-Noise, Step-Up DC-DC Converter

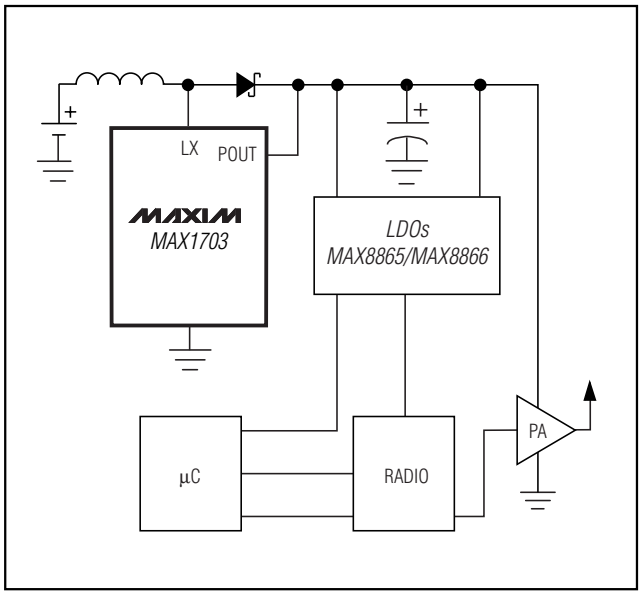


Figure 8. Typical Phone Application

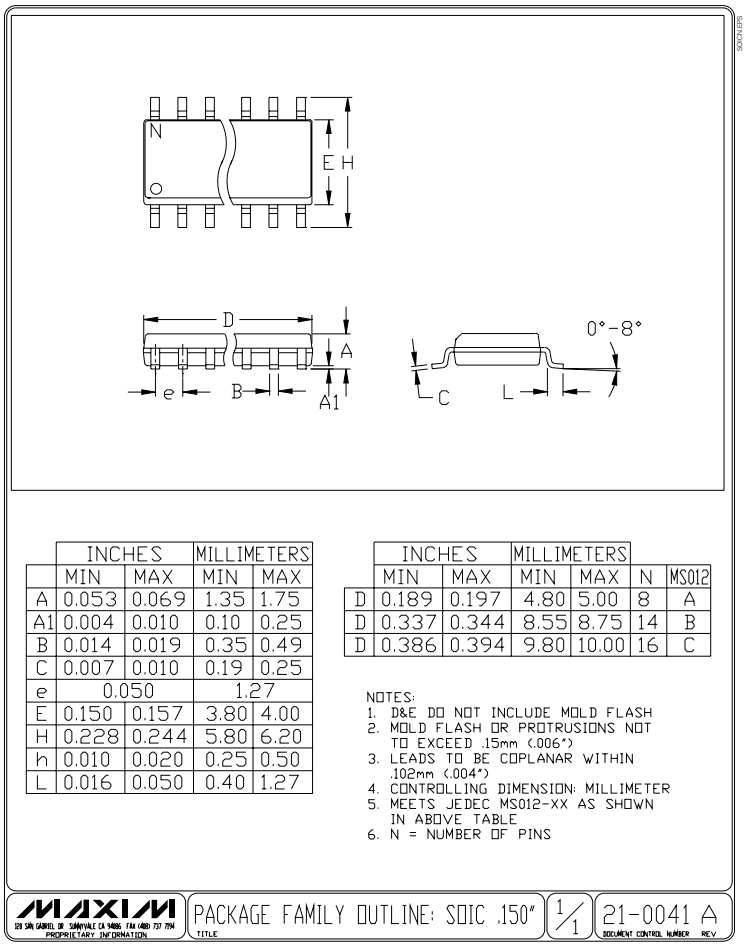
Chip Information

TRANSISTOR COUNT: 554

SUBSTRATE CONNECTED TO GND

1-Cell to 3-Cell, High-Power (1.5A), Low-Noise, Step-Up DC-DC Converter

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | TITLE: PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | DOCUMENT CONTROL NUMBER: 21-0041 A REV

NOTES