Single Quick-PWM Step-Down Controller with Dynamic REFIN

ABSOLUTE MAXIMUM RATINGS

TON to GND .....-0.3V to +28V
V_{DD} to GND .....-0.3V to +6V
V_{CC} to GND .....-0.3V to (V_{DD} + 0.3V)
EN, PGOOD to GND .....-0.3V to +6V
REF, REFIN to GND .....-0.3V to (V_{CC} + 0.3V)
CS, FB to GND .....-0.3V to (V_{CC} + 0.3V)
DL to GND .....-0.3V to (V_{DD} + 0.3V)
BST to GND .....(V_{DD} - 0.3V) to +34V
BST to LX .....-0.3V to +6V
BST to V_{DD} .....-0.3V to +28V
DH to LX .....-0.3V to (V_{BST} + 0.3V)
REF Short Circuit to GND .....Continuous
Continuous Power Dissipation (T_A = +70°C)
14-Pin 3mm x 3mm TDFN
(derated 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range (extended) .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, REFIN = REF. T_A = **0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range	V_{IN}			2		26	V
Quiescent Supply Current (V_{DD})	I_{DD} + I_{CC}	FB forced above REFIN			0.7	1.2	mA
Shutdown Supply Current (V_{DD})	I_{SHDN}	EN = GND, T_A = +25°C			0.1	2	µA
V_{DD}-to-V_{CC} Resistance	R_{CC}				20		Ω
On-Time	t_{ON}	V_{IN} = 12V, V_{FB} = 1.0V (Note 3)	R_{TON} = 97.5kΩ (600kHz)	118	139	160	ns
			R_{TON} = 200kΩ (300kHz)	250	278	306	
			R_{TON} = 302.5kΩ	354	417	480	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)			200	300	ns
TON Shutdown Supply Current		EN = GND, V_{TON} = 26V, V_{CC} = 0V or 5V, T_A = +25°C			0.01	1	µA
REFIN Voltage Range	V_{REFIN}	(Note 2)		0		V_{REF}	V
REFIN Input Current	I_{REFIN}	REFIN = 0.5V to 2V, T_A = +25°C		-50		+50	nA
FB Voltage Range	V_{FB}	(Note 2)		0		V_{REF}	V
FB Voltage Accuracy	V_{FB}	V_{REFIN} = 0.5V, measured at FB, V_{IN} = 2V to 26V	T_A = +25°C	0.495	0.5	0.505	V
			T_A = 0°C to +85°C	0.493		0.507	
		V_{REFIN} = 1.0V	T_A = +25°C	0.995	1.0	1.005	
			T_A = 0°C to +85°C	0.993		1.007	
		V_{REFIN} = 2.0V	T_A = 0°C to +85°C	1.990	2.0	2.010	
FB Input Bias Current	I_{FB}	0.5V to 2.0V, T_A = +25°C		-0.1		+0.1	µA
FB Output Low Voltage		I_{SINK} = 3mA				0.4	V
Load-Regulation Error		V_{CS} = 2mV to 20mV			0.1		%
Line-Regulation Error		V_{CC} = 4.5V to 5.5V, V_{IN} = 4.5V to 26V			0.25		%
Soft-Start/Stop Slew Rate	SS_{SR}	Rising/falling edge on EN		0.4	1.2	2.2	mV/µs
Dynamic REFIN Slew Rate	DYN_{SR}	Rising edge on REFIN		3	9.45	18	mV/µs

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, REFIN = REF. T_A = **0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE							
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V	No load	1.990	2.00	2.010	V
			I_{REF} = -10µA to +50µA	1.98	2.00	2.02	
FAULT DETECTION							
Upper PGOOD Trip Threshold	V_{PGOOD_H}	With respect to the internal target voltage (error comparator threshold); rising edge; hysteresis = 50mV		250	300	350	mV
		Dynamic transition			V_{REF} + 0.30		V
		Minimum V_{PGOOD_H} threshold			0.7		
Lower PGOOD Trip Threshold	V_{PGOOD_L}	With respect to the internal target voltage (error comparator threshold) falling edge; hysteresis = 50mV		-240	-200	-160	mV
Output Undervoltage Fault-Propagation Delay	t_{UVP}	FB forced 25mV below V_{PGOOD_L} trip threshold		100	200	350	µs
PGOOD Propagation Delay	t_{PGOOD}	V_{PGOOD_L} falling edge, 25mV overdrive			5		µs
		V_{PGOOD_H} rising edge, 25mV overdrive			5		
		Startup delay		100	200	350	
PGOOD Output Low Voltage		I_{SINK} = 3mA				0.4	V
PGOOD Leakage Current	I_{PGOOD}	FB = REFIN (PGOOD high impedance), PGOOD forced to 5V, T_A = +25°C				1	µA
Dynamic REFIN Transition Fault Blanking Threshold		Fault blanking initiated; REFIN deviation from the internal target voltage (error comparator threshold); hysteresis = 10mV			±50		mV
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C			160		°C
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, PWM disabled below this level; hysteresis = 100mV		3.95	4.2	4.45	V
CURRENT LIMIT							
Current-Limit Threshold	V_{CS}			18	20	22	mV
Current-Limit Threshold (Negative)	V_{INEG}				-24		mV
Current-Limit Threshold (Zero Crossing)	V_{ZX}	V_{GND} - V_{CS}			1		mV
CS Input Current	I_{CS}	V_{CS} = ±200mV, T_A = +25°C		-1		+1	µA

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Single Quick-PWM Step-Down Controller with Dynamic REFIN

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, REFIN = REF. T_A = **0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GATE DRIVERS							
DH Gate Driver On-Resistance	$R_{ON(DH)}$	BST - LX forced to 5V	Low state		1.2	3.5	Ω
			High state (pullup)		1.2	3.5	
DL Gate Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			1.7	4	Ω
		Low state (pulldown)			0.9	2	
DH Gate Driver Source/ Sink Current	I_{DH}	DH forced to 2.5V, BST - LX forced to 5V			1.5		A
DL Gate Driver Source Current	$I_{DL(SOURCE)}$	DL forced to 2.5V			1		A
DL Gate Driver Sink Current	$I_{DL(SINK)}$	DL forced to 2.5V			2.4		A
Driver Propagation Delay		DH low to DL high		10	25		ns
		DL low to DH high		15	35		
DL Transition Time		DL falling, C_{DL} = 3nF			20		ns
		DL rising, C_{DL} = 3nF			20		
DH Transition Time		DH falling, C_{DH} = 3nF			20		ns
		DH rising, C_{DH} = 3nF			20		
Internal BST Switch On-Resistance	R_{BST}	I_{BST} = 10mA, V_{DD} = 5V			4	7	Ω
INPUTS AND OUTPUTS							
EN Logic-Input Threshold	V_{EN}	EN rising edge, hysteresis = 450mV (typ)		1.20	1.7	2.20	V
EN Logic-Input Current	I_{EN}	EN forced to GND or V_{DD}, T_A = +25°C		-0.5		+0.5	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, REFIN = REF. T_A = **-40°C to +85°C**, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
PWM CONTROLLER						
Input Voltage Range	V_{IN}			2	26	V
Quiescent Supply Current (V_{DD})	I_{DD} + I_{CC}	FB forced above REFIN			1.2	mA
On-Time	t_{ON}	V_{IN} = 12V, V_{FB} = 1.0V (Note 3)	R_{TON} = 97.5kΩ (600kHz)	115	163	ns
			R_{TON} = 200kΩ (300kHz)	250	306	
			R_{TON} = 302.5kΩ (200kHz)	348	486	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)			350	ns
REFIN Voltage Range	V_{REFIN}	(Note 2)		0	V_{REF}	V
FB Voltage Range	V_{FB}	(Note 2)		0	V_{REF}	V
FB Voltage Accuracy	V_{FB}	Measured at FB, V_{IN} = 2V to 26V	V_{REFIN} = 0.5V	0.49	0.51	V
			V_{REFIN} = 1.0V	0.99	1.01	
			V_{REFIN} = 2.0V	1.985	2.015	
FB Output Low Voltage		I_{SOURCE} = 3mA			0.4	V

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN} = 5V, REFIN = REF. T_A = **-40°C to +85°C**, unless otherwise specified.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
REFERENCE						
Reference Voltage	V_{REF}	V_{DD} = 4.5V to 5.5V		1.985	2.015	V
FAULT DETECTION						
Upper PGOOD Trip Threshold	V_{PGOOD_H}	With respect to the internal target voltage (error comparator threshold) rising edge; hysteresis = 50mV		250	350	mV
Lower PGOOD Trip Threshold	V_{PGOOD_L}	With respect to the internal target voltage (error comparator threshold) falling edge; hysteresis = 50mV		-240	-160	mV
Output Undervoltage Fault-Propagation Delay	t_{UVP}	FB forced 25mV below V_{PGOOD_L} trip threshold		80	400	µs
PGOOD Output Low Voltage		I_{SINK} = 3mA			0.4	V
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, PWM disabled below this level, hysteresis = 100mV		3.95	4.45	V
CURRENT LIMIT						
Current-Limit Threshold	V_{CS}			17	23	mV
GATE DRIVERS						
DH Gate Driver On-Resistance	$R_{ON(DH)}$	BST - LX forced to 5V	Low state (pulldown)		3.5	Ω
			High state (pullup)		3.5	
DL Gate Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			4	Ω
		Low state (pulldown)			2	
Internal BST Switch On-Resistance	R_{BST}	I_{BST} = 10mA, V_{DD} = 5V			7	Ω
INPUTS AND OUTPUTS						
EN Logic-Input Threshold	V_{EN}	EN rising edge hysteresis = 450mV (typ)		1.20	2.20	V

Note 1: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed by design and characterization.

Note 2: The 0 to 0.5V range is guaranteed by design, not production tested.

Note 3: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = GND, V_{BST} = 5V, and a 250pF capacitor connected from DH to LX. Actual in-circuit times can differ due to MOSFET switching speeds.

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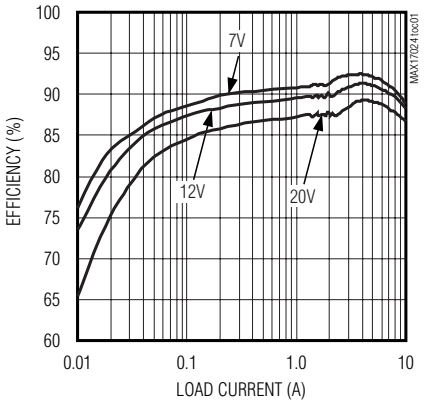
Single Quick-PWM Step-Down Controller with Dynamic REFIN

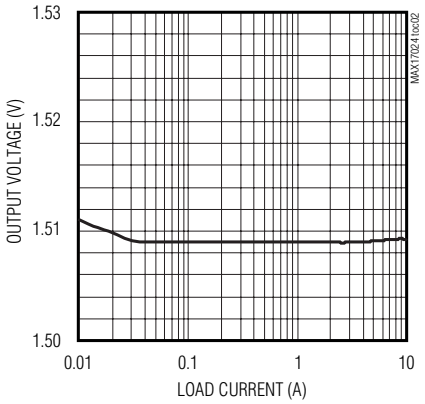
Typical Operating Characteristics

(MAX17024 Circuit of Figure 1, V_{IN} = 12V, V_{DD} = 5V, R_{TON} = 200kΩ, T_A = +25°C, unless otherwise noted.)

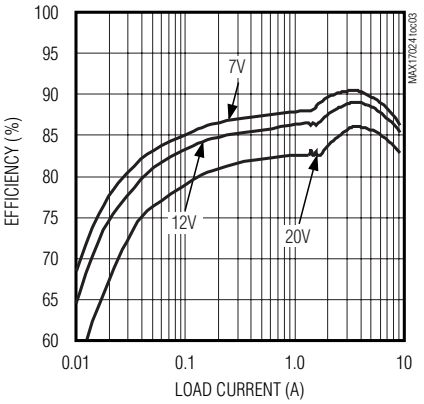
1.5V OUTPUT EFFICIENCY vs. LOAD CURRENT



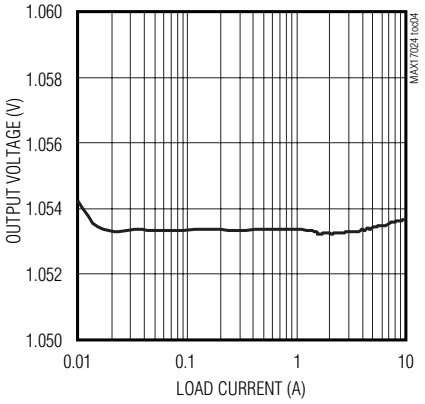
1.5V OUTPUT VOLTAGE vs. LOAD CURRENT



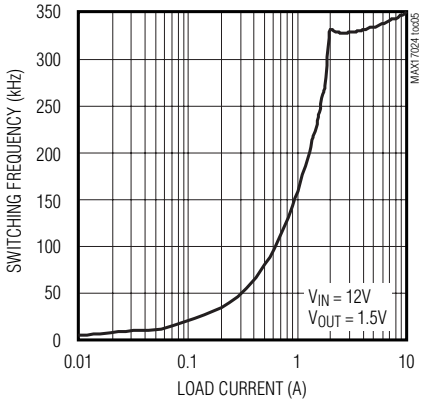
1.05V OUTPUT EFFICIENCY vs. LOAD CURRENT



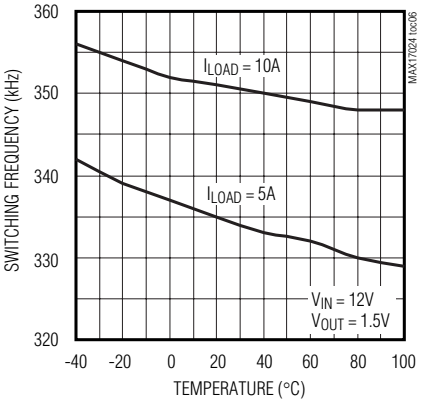
1.05V OUTPUT VOLTAGE vs. LOAD CURRENT



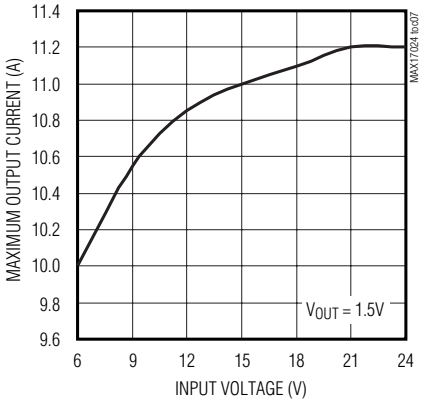
SWITCHING FREQUENCY vs. LOAD CURRENT



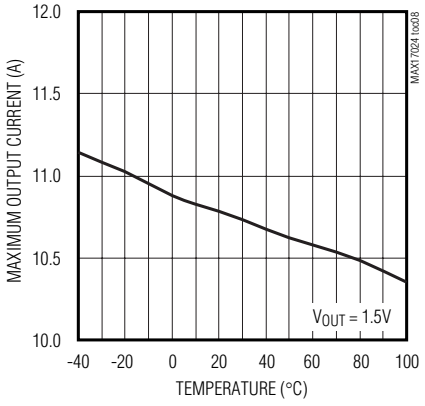
SWITCHING FREQUENCY vs. TEMPERATURE



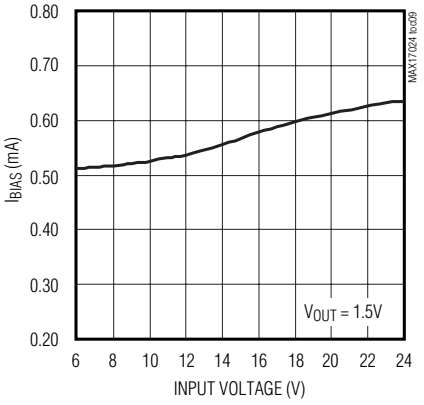
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



MAXIMUM OUTPUT CURRENT vs. TEMPERATURE



NO-LOAD SUPPLY CURRENT I_{BIAS} vs. INPUT VOLTAGE



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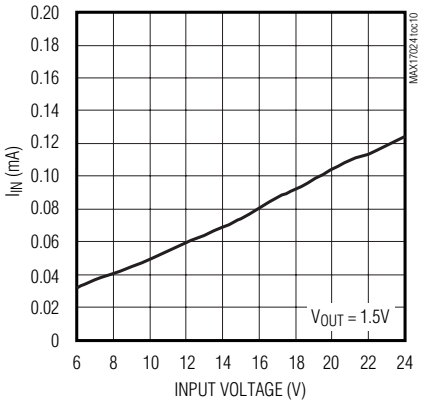
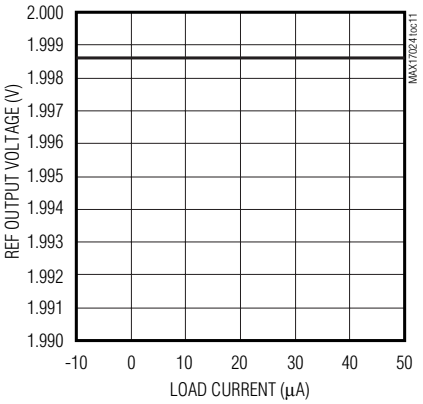
Typical Operating Characteristics (continued)

(MAX17024 Circuit of Figure 1, V_{IN} = 12V, V_{DD} = 5V, R_{TON} = 200kΩ, T_A = +25°C, unless otherwise noted.)

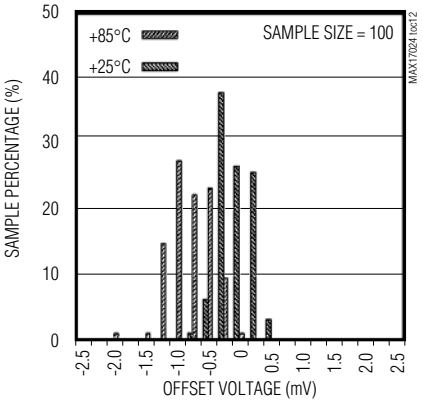
NO-LOAD SUPPLY CURRENT I_{IN} vs. INPUT VOLTAGE



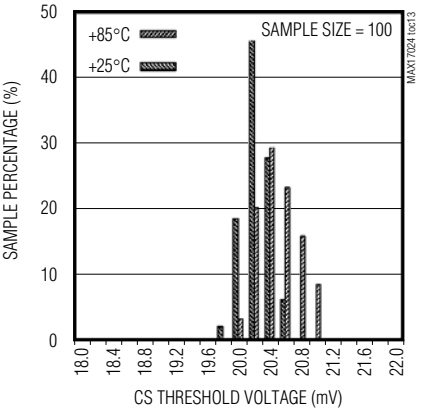
REF OUTPUT VOLTAGE vs. LOAD CURRENT



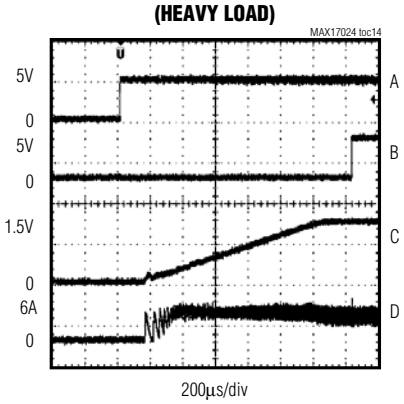
REFIN-TO-FB OFFSET VOLTAGE DISTRIBUTION



CURRENT-LIMIT THRESHOLD VOLTAGE DISTRIBUTION



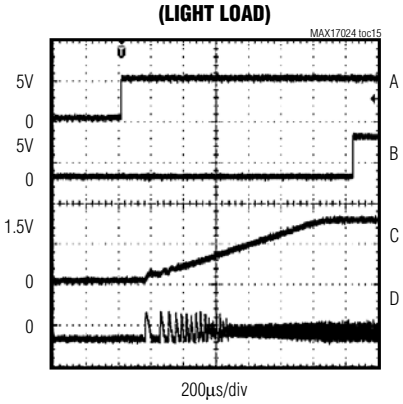
SOFT-START WAVEFORM (HEAVY LOAD)



A. EN, 5V/div
B. PWRGD, 5V/div
C. V_{OUT}, 1V/div
D. INDUCTOR CURRENT, 10A/div

I_{OUT} = 6A

SOFT-START WAVEFORM (LIGHT LOAD)



A. EN, 5V/div
B. PWRGD, 5V/div
C. V_{OUT}, 1V/div
D. INDUCTOR CURRENT, 10A/div

I_{OUT} = 1A

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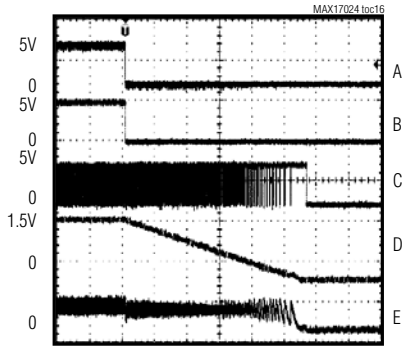
Single Quick-PWM Step-Down Controller with Dynamic REFIN

Typical Operating Characteristics (continued)

(MAX17024 Circuit of Figure 1, V_{IN} = 12V, V_{DD} = 5V, R_{TON} = 200kΩ, T_A = +25°C, unless otherwise noted.)

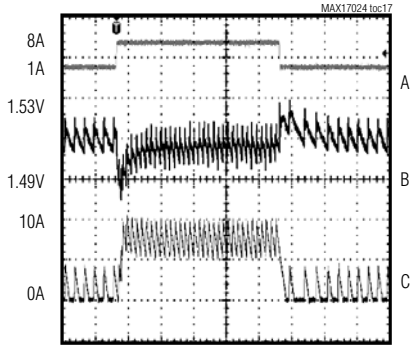
SHUTDOWN WAVEFORM



A. EN, 5V/div
B. PWRGD, 5V/div
C. DL, 5V/div
D. V_{OUT}, 1V/div
E. INDUCTOR CURRENT, 5A/div

I_{OUT} = 6A

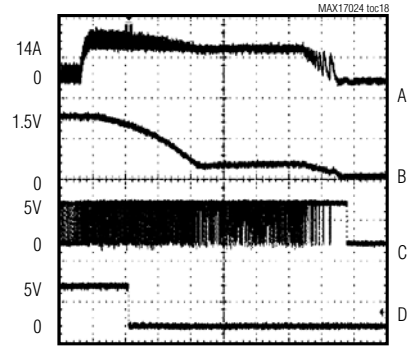
LOAD-TRANSIENT RESPONSE



A. I_{OUT} 10A/div
B. V_{OUT}, 20mV/div
C. INDUCTOR CURRENT, 5A/div

I_{OUT} = 1A TO 8A TO 1A

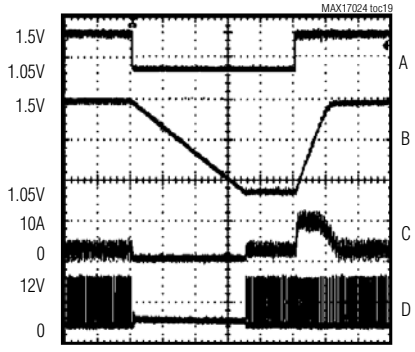
OUTPUT OVERLOAD WAVEFORM



A. INDUCTOR CURRENT, 10A/div
B. V_{OUT}, 1V/div
C. DL, 5V/div
D. PGOOD, 5V/div

I_{OUT} = 2A TO 14A

DYNAMIC OUTPUT-VOLTAGE TRANSITION



A. REFIN, 500mV/div
B. V_{OUT}, 200mV/div
C. INDUCTOR CURRENT, 10A/div
D. LX, 10V/div

I_{OUT} = 2A

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Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Supply Voltage Input for the DL Gate Driver. Connect to the system supply voltage (+4.5V to +5.5V). Bypass V_{DD} to power ground with a 1µF or greater ceramic capacitor.
2	DL	Low-Side Gate Driver. DL swings from GND to V_{DD}. The MAX17024 forces DL low during V_{CC} UVLO and REFOK lockout conditions.
3	N.C.	Not Connected
4	LX	Inductor Connection. Connect LX to the switched side of the inductor as shown in Figure 1.
5	DH	High-Side Gate Driver. DH swings from LX to BST. The MAX17024 pulls DH low whenever the controller is disabled.
6	BST	Boost Flying-Capacitor Connection. Connect to an external 0.1µF 6V capacitor as shown in Figure 1. The MAX17024 contains an internal boost switch/diode (see Figure 2).
7	TON	Switching Frequency-Setting Input. An external resistor between the input power source and TON sets the switching period (T_{SW} = 1 / f_{SW}) according to the following equation: $$T_{SW} = C_{TON}(R_{TON} + 6.5k\Omega)\left(\frac{V_{FB}}{V_{OUT}}\right)$$ where C_{TON} = 16.26pF and V_{FB} = V_{REFIN} under normal operating conditions. If the TON current drops below 10µA, the MAX17024 shuts down and enters a high-impedance state. TON is high impedance in shutdown.
8	FB	Feedback Voltage-Sense Connection. Connect directly to the positive terminal of the output capacitors for output voltages less than 2V as shown in Figure 1. For fixed-output voltages greater than 2V, connect REFIN to REF and use a resistive divider to set the output voltage (Figure 4). FB senses the output voltage to determine the on-time for the high-side switching MOSFET.
9	CS	Current-Sense Input Pin. Connect to low-side MOSFET current-sense resistor. The current-limit threshold is 20mV (typ).
10	REFIN	External Reference Input. REFIN sets the feedback regulation voltage (V_{FB} = V_{REFIN}) of the MAX17024 using the resistor-divider connected between REF and GND. The MAX17024 includes an internal window comparator to detect REFIN voltage transitions, allowing the controller to blank PGOOD and the fault protection.
11	REF	2V Reference Voltage. Bypass to analog ground using a 470pF to 1nF ceramic capacitor. The reference can source up to 50µA for external loads.
12	EN	Shutdown Control Input. Connect to V_{DD} for normal operation. Pull EN low to place the controller into its 2µA shutdown state. When disabled, the MAX17024 slowly ramps down the target/output voltage to ground and after the target voltage reaches 0.1V, the controller forces both DH and DL low and enters the low-power shutdown state. Toggle EN to clear the fault-protection latch.
13	V_{CC}	5V Analog Supply Voltage. Internally connected to V_{DD} through an internal 20Ω resistor. Bypass V_{CC} to analog ground using a 1µF ceramic capacitor.
14	PGOOD	Open-Drain Power-Good Output. PGOOD is low when the output voltage is more than 200mV (typ) below or 300mV (typ) above the target voltage (V_{REFIN}) during soft-start and soft-shutdown. After the soft-start circuit has terminated, PGOOD becomes high impedance if the output is in regulation. PGOOD is blanked—forced high-impedance state—when a dynamic REFIN transition is detected.
EP (15)	GND	Ground/Exposed Pad. Internally connected to the controller's ground plane and substrate. **Connect directly to ground.**

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Single Quick-PWM Step-Down Controller with Dynamic REFIN

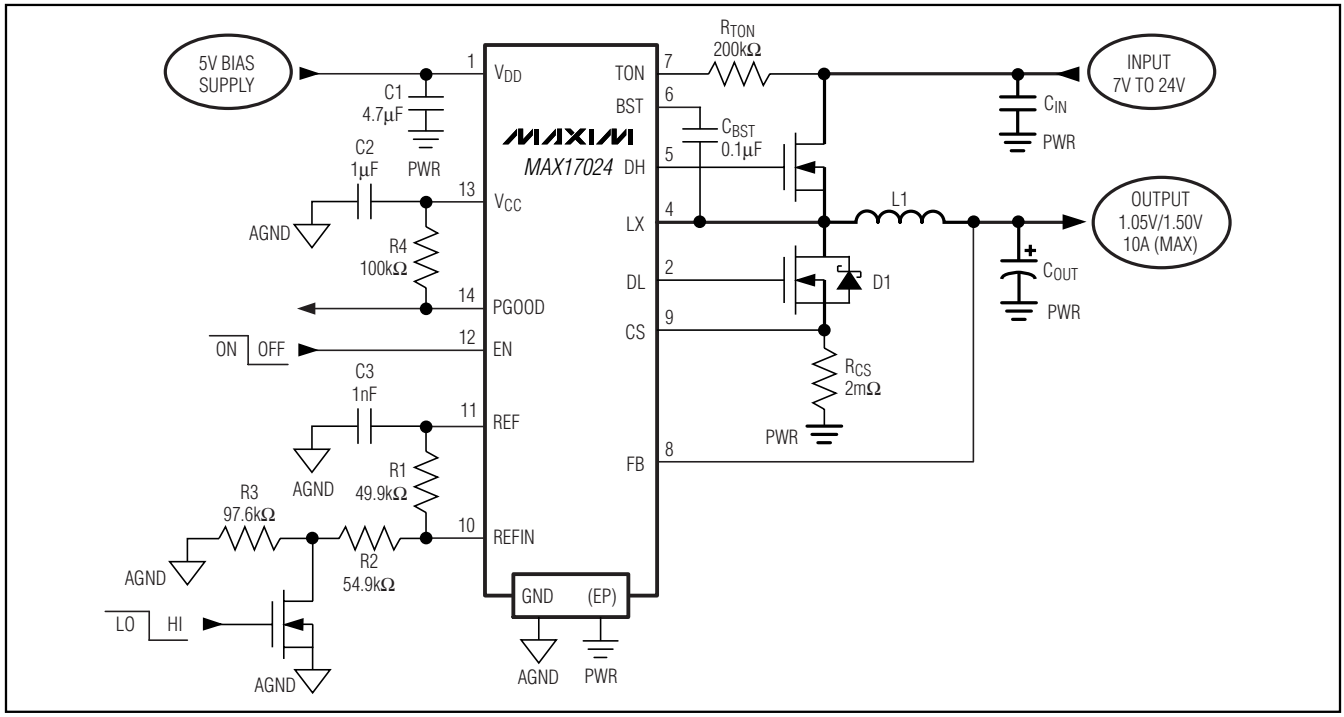

Figure 1. MAX17024 Standard Application Circuit

Table 1. Component Suppliers

MANUFACTURER	WEBSITE
AVX	www.avxcorp.com
BI Technologies	www.bitechnologies.com
Central Semiconductor	www.centralsemi.com
Coiltronics	www.cooperet.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET	www.kemet.com
NEC Tokin	www.nec-tokin.com
Panasonic	www.panasonic.com
Pulse	www.pulseeng.com
Renesas	www.renesas.com
SANYO	www.edc.sanyo.com
Siliconix (Vishay)	www.vishay.com
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com
TOKO	www.tokoam.com
Toshiba	www.toshiba.com
Wurth	www.we-online.com

Standard Application Circuit

The MAX17024 standard application circuit (Figure 1) generates a 1.5V or 1.05V output rail for general-purpose use in a notebook computer. Table 1 lists the component manufacturers.

Detailed Description

The MAX17024 step-down controller is ideal for the low-duty-cycle (high-input voltage to low-output voltage) applications required by notebook computers. Maxim's proprietary Quick-PWM pulse-width modulator in the MAX17024 is specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency, current-mode PWMs while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time (regardless of input voltage) PFM control schemes.

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+5V Bias Supply (V_{CC}/V_{DD})

The MAX17024 requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's main 95% efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V supply can be generated with an external linear regulator, such as the MAX1615.

The 5V bias supply powers both the PWM controller and internal gate drive, so the maximum current drawn is determined by:

$$I_{BIAS} = I_Q + f_{SW}Q_G = 2mA \text{ to } 20mA \text{ (typ)}$$

The MAX17024 includes a 20Ω resistor between V_{DD} and V_{CC}, simplifying the PCB layout request.

Free-Running Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant on-time, current-mode regulator with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a

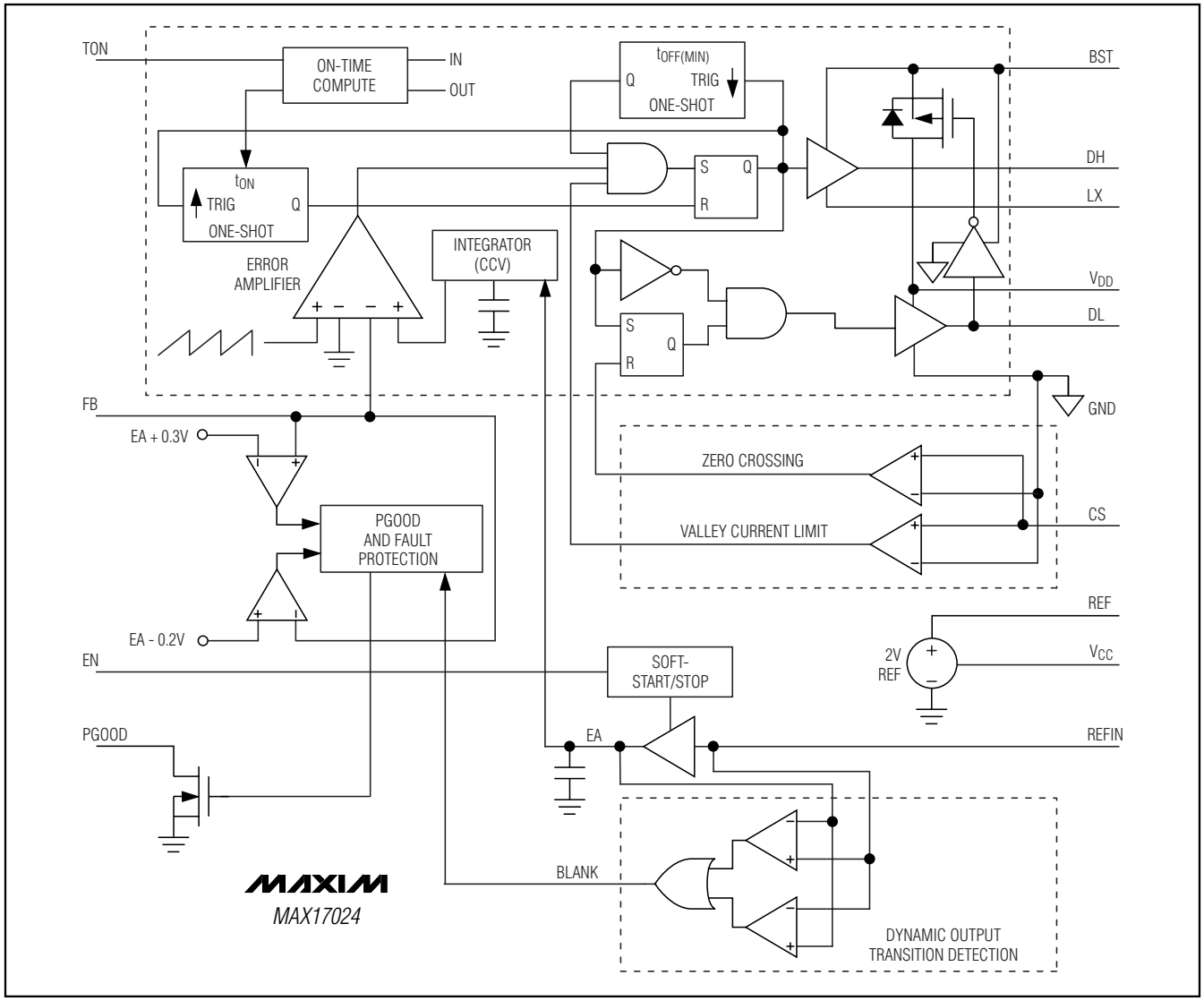

Figure 2. MAX17024 Functional Block Diagram

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Single Quick-PWM Step-Down Controller with Dynamic REFIN

one-shot whose pulse width that is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (200ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to input and output voltage. The high-side switch on-time is inversely proportional to the input voltage as sensed by the TON input, and proportional to the feedback voltage as sensed by the FB input:

$$\text{On-Time } (t_{ON}) = T_{SW} (V_{FB} / V_{IN})$$

where T_{SW} (switching period) is set by the resistance (R_{TON}) between TON and V_{IN}. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. Connect a resistor (R_{TON}) between TON and V_{IN} to set the switching period $T_{SW} = 1 / f_{SW}$:

$$T_{SW} = C_{TON}\left(R_{TON} + 6.5k\Omega\right)\left(\frac{V_{FB}}{V_{OUT}}\right)$$

where C_{TON} = 16.26pF. When used with unity-gain feedback ($V_{OUT} = V_{FB}$), a 96.75kΩ to 303.25kΩ corresponds to switching periods of 167ns (600kHz) to 500ns (200kHz), respectively. High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

For continuous conduction operation, the actual switching frequency can be estimated by:

$$f_{SW} = \frac{V_{FB} + V_{DIS}}{t_{ON}(V_{IN} - V_{CHG} + V_{DIS})}$$

where V_{DIS} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; V_{CHG} is the sum of the resistances in the charging path, including the high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time calculated by the MAX17024.

Power-Up Sequence (POR, UVLO)

The MAX17024 is enabled when EN is driven high, and the 5V bias supply (V_{DD}) is present. The reference powers up first. Once the reference exceeds its UVLO threshold, the internal analog blocks are turned on and masked by a 50µs one-shot delay to allow the bias circuitry and analog blocks enough time to settle to their proper states. With the control circuitry reliably powered up, the PWM controller may begin switching.

Power-on reset (POR) occurs when V_{CC} rises above approximately 3V, resetting the fault latch and preparing the controller for operation. The V_{CC} UVLO circuitry inhibits switching until V_{CC} rises above 4.25V. The controller powers up the reference once the system enables the controller, V_{CC} exceeds 4.25V, and EN is driven high. With the reference in regulation, the controller ramps the output voltage to the target REFIN voltage with a 1.2mV/µs slew rate:

$$t_{START} = \frac{V_{FB}}{1.2mV/\mu s} = \frac{V_{FB}}{1.2V/ms}$$

The soft-start circuitry does not use a variable current limit, so full output current is available immediately. PGOOD becomes high impedance approximately 200µs after the target REFIN voltage has been reached. The MAX17024 automatically uses pulse-skipping mode during soft-start and uses forced-PWM mode during soft-shutdown.

For automatic startup, the battery voltage should be present before V_{CC}. If the controller attempts to bring the output into regulation without the battery voltage present, the fault latch trips. The controller remains shut down until the fault latch is cleared by toggling EN or cycling the V_{CC} power supply below 0.5V.

If the V_{CC} voltage drops below 4.25V, the controller assumes that there is not enough supply voltage to make valid decisions. To protect the output from overvoltage faults, the controller shuts down immediately and forces a high-impedance output (DL and DH pulled low).

Shutdown

When the system pulls EN low, the MAX17024 enters low-power shutdown mode. PGOOD is pulled low immediately, and the output voltage ramps down with a 1.2mV/µs slew rate:

$$t_{SHDN} = \frac{V_{FB}}{1.2mV/\mu s} = \frac{V_{FB}}{1.2V/ms}$$

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Slowly discharging the output capacitors by slewing the output over a long period of time (typically 0.5ms to 2ms) keeps the average negative inductor current low (damped response), thereby preventing the negative output-voltage excursion that occurs when the controller discharges the output quickly by permanently turning on the low-side MOSFET (underdamped response). This eliminates the need for the Schottky diode normally connected between the output and ground to clamp the negative output-voltage excursion. After the controller reaches the zero target, the MAX17024 shuts down completely—the drivers are disabled (DL and DH pulled low)—the reference turns off, activates 10Ω pulldown on FB, and the supply currents drop to about 0.1µA (typ).

When a fault condition—output UVP or thermal shutdown—activates the shutdown sequence, the protection circuitry sets the fault latch to prevent the controller from restarting. To clear the fault latch and reactivate the controller, toggle EN or cycle V_{CC} power below 0.5V.

The MAX17024 automatically uses pulse-skipping mode during soft-start and uses forced-PWM mode during soft-shutdown.

Automatic Pulse-Skipping

The MAX17024 permanently operates in automatic skip mode. An inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator threshold is set by the differential across the low-side MOSFET sense resistor.

The controller automatically transitions to fixed-frequency PWM operation when the load reaches the same critical condition point ($I_{LOAD(SKIP)}$) that occurs at the skip and the PWM boundary.

DC output-accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the MAX17024 regulates the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction ($I_{OUT} < I_{LOAD(SKIP)}$), the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation.

Since the output is not able to sink current, the timing for negative dynamic output-voltage transitions depends on the load current and output capacitance. Letting the output voltage drift down is typically recommended to reduce the potential for audible noise since this eliminates the input current surge during negative output-voltage transitions.

Valley Current-Limit Protection

The current-limit circuit employs a unique "valley" current-sensing algorithm that senses the inductor current through the low-side MOSFET sense resistor. If the current through the low-side MOSFET exceeds the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and input voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

Integrated Output Voltage

The MAX17024 regulates the valley of the output ripple, so the actual DC output voltage is higher than the slope-compensated target by 50% of the output ripple voltage. Under steady-state conditions, the MAX17024's internal integrator corrects for this 50% output ripple-voltage error, resulting in an output voltage accuracy that is dependent only on the offset voltage of the integrator amplifier provided in the *Electrical Characteristics* table.

Dynamic Output Voltages

The MAX17024 regulates FB to the voltage set at REFIN. By changing the voltage at REFIN (Figure 1), the MAX17024 can be used in applications that require dynamic output-voltage changes between two set points. For a step-voltage change at REFIN, the rate of change of the output voltage is limited either by the internal 9.45mV/µs slew-rate circuit or by the component selection—inductor current ramp, the total output capacitance, the current limit, and the load during the transition—whichever is slower. The total output capacitance determines how much current is needed to change the output voltage, while the inductor limits the current ramp rate. Additional load current may slow down the output voltage change during a positive REFIN voltage change, and may speed up the output voltage change during a negative REFIN voltage change.

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Single Quick-PWM Step-Down Controller with Dynamic REFIN

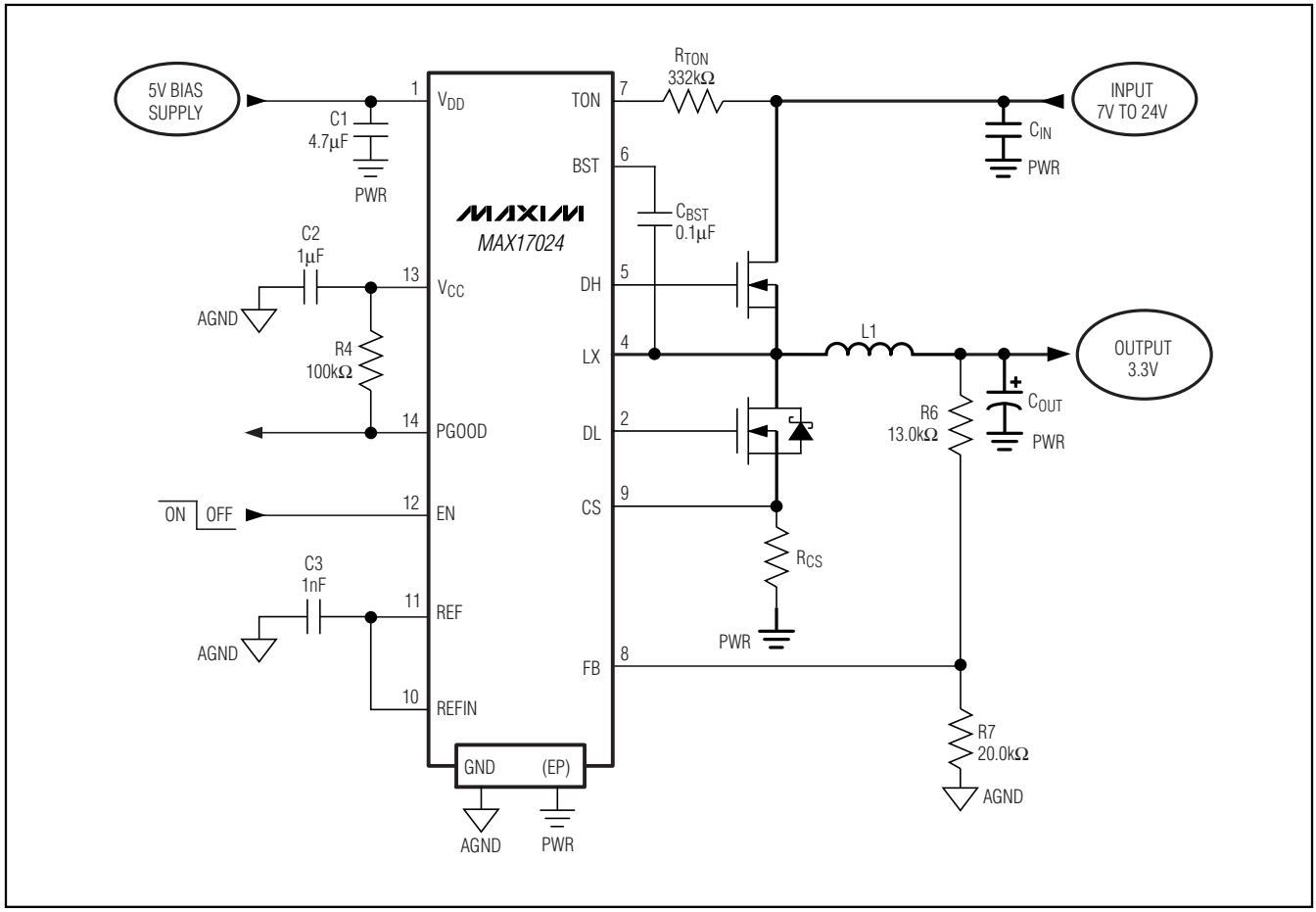

Figure 3. High Output-Voltage Application Using a Feedback Divider

Output Voltages Greater than 2V

Although REFIN is limited to a 0 to 2V range, the output-voltage range is unlimited since the MAX17024 utilizes a high-impedance feedback input (FB). By adding a resistive voltage-divider from the output to FB to analog ground (Figure 3), the MAX17024 supports output voltages above 2V. However, the controller also uses FB to determine the on-time, so the voltage-divider influences the actual switching frequency, as detailed in the *On-Time One-Shot* section.

Internal Integration

An integrator amplifier forces the DC average of the FB voltage to equal the target voltage. This internal amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 2), allowing accurate DC output-voltage regulation regardless of the compensated feedback ripple voltage and internal slope-compensation variation. The integrator amplifier has the ability to shift the output voltage by ±55mV (typ).

The MAX17024 disables the integrator by connecting the amplifier inputs together at the beginning of all downward REFIN transitions done in pulse-skipping mode. The integrator remains disabled until 20µs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

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Power-Good Outputs (PGOOD) and Fault Protection

PGOOD is the open-drain output that continuously monitors the output voltage for undervoltage and overvoltage conditions. PGOOD is actively held low in shutdown (EN = GND) during soft-start and soft-shutdown. Approximately 200µs (typ) after the soft-start terminates, PGOOD becomes high impedance as long as the feedback voltage is above the PGOOD_L threshold (REFIN - 200mV) and below the PGOOD_H threshold (REFIN + 300mV). PGOOD goes low if the feedback voltage drops 200mV below the target voltage (REFIN) or rises 300mV above the target voltage (REFIN), or the SMPS controller is shut down. For a logic-level PGOOD output voltage, connect an external pullup resistor between PGOOD and V_{DD}. A 100kΩ pullup resistor works well in most applications. Figure 4 shows the power-good and fault-protection circuitry.

PGOOD

When the feedback voltage drops 200mV below the target voltage (REFIN), the controller immediately pulls PGOOD low and triggers a 200µs one-shot timer. If the feedback voltage remains below the V_{PGOOD_L} threshold for the entire 200µs, the undervoltage fault latch is set and the SMPS begins the shutdown sequence. When the internal target voltage drops below 0.1V, the MAX17024 forces DL low. Toggle EN or cycle V_{CC} power below V_{CC} POR to clear the fault latch and restart the controller.

Thermal-Fault Protection (TSHDN)

The MAX17024 features a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD low, and shuts down the controller. Both DL and DH are pulled low. Toggle EN or cycle V_{CC} power below V_{CC} POR to reactivate the controller after the junction temperature cools by 15°C.

MOSFET Gate Drivers

The DH and DL drivers are optimized for driving moderate-sized high-side and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. The high-side gate driver (DH) sources and sinks 1.5A, and the low-side gate driver (DL) sources 1.0A and sinks 2.4A. This ensures robust gate drive for high-current applications. The DH floating high-side MOSFET driver is powered by internal boost switch charge pumps at BST, while the DL synchronous-rectifier driver is powered directly by the 5V bias supply (V_{DD}).

Adaptive dead-time circuits monitor the DL and DH drivers and prevent either FET from turning on until the other is fully off. The adaptive driver dead time allows operation without shoot-through with a wide range of MOSFETs, minimizing delays and maintaining efficiency.

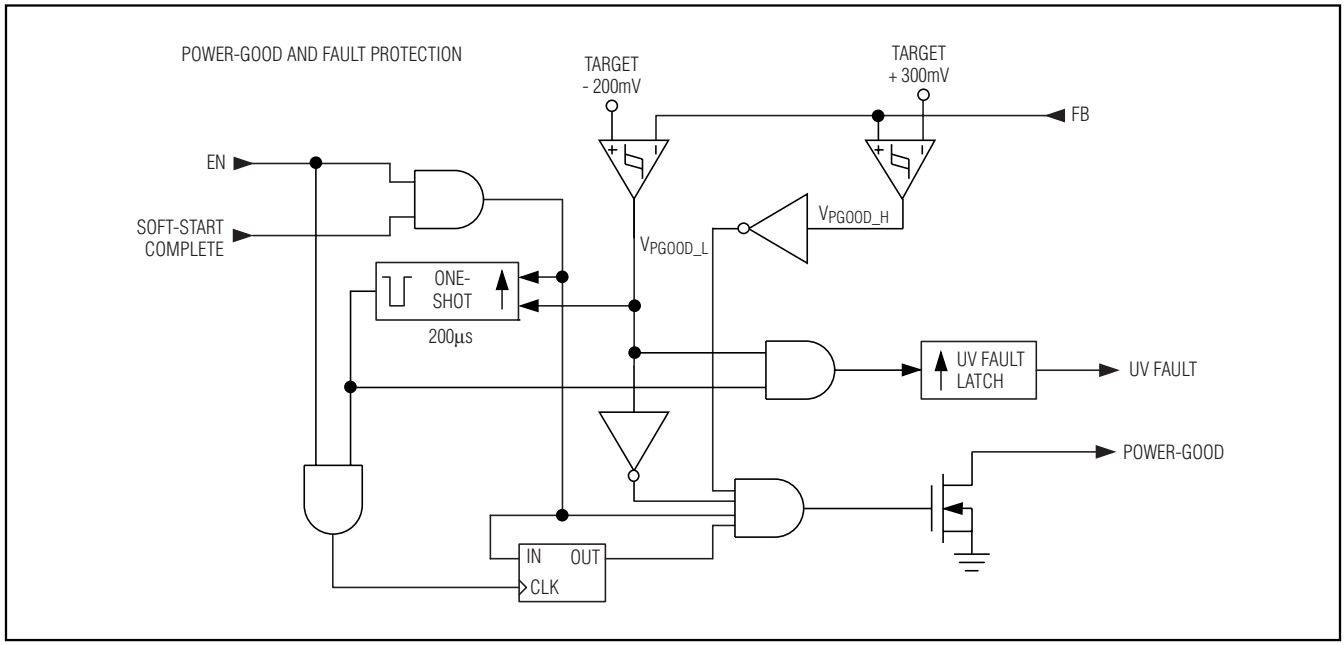

Figure 4. Power-Good and Fault Protection

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Single Quick-PWM Step-Down Controller with Dynamic REFIN

There must be a low-resistance, low-inductance path from the DL and DH drivers to the MOSFET gates for the adaptive dead-time circuits to work properly; otherwise, the sense circuitry in the MAX17024 interprets the MOSFET gates as "off" while charge actually remains. Use very short, wide traces (50 mils to 100 mils wide if the MOSFET is 1in from the driver).

The internal pulldown transistor that drives DL low is robust, with a 0.9Ω (typ) on-resistance. This helps prevent DL from being pulled up due to capacitive coupling from the drain to the gate of the low-side MOSFETs when the inductor node (LX) quickly switches from ground to V_{IN}. Applications with high-input voltages and long inductive driver traces must ensure rising LX edges do not pull up the low-side MOSFETs' gate, causing shoot-through currents. The capacitive coupling between LX and DL created by the MOSFET's gate-to-drain capacitance (C_{RSS}), gate-to-source capacitance (C_{ISS} - C_{RSS}), and additional board parasitics should not exceed the following minimum threshold:

$$V_{GS(TH)} > V_{IN}\left(\frac{C_{RSS}}{C_{ISS}}\right)$$

Typically, adding a 4700pF between DL and power ground (C_{NL} in Figure 5), close to the low-side MOSFETs, greatly reduces coupling. Do not exceed 22nF of total gate capacitance to prevent excessive turn-off delays.

Alternatively, shoot-through currents can be caused by a combination of fast high-side MOSFETs and slow low-side MOSFETs. If the turn-off delay time of the low-side MOSFET is too long, the high-side MOSFETs can turn on before the low-side MOSFETs have actually turned off. Adding a resistor less than 5Ω in series with BST slows down the high-side MOSFET turn-on time, eliminating the shoot-through currents without degrading the turn-off time (R_{BST} in Figure 5). Slowing down the high-side MOSFET also reduces the LX node rise time, thereby reducing EMI and high-frequency coupling responsible for switching noise.

Quick-PWM Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input voltage range:** The maximum value ($V_{IN(MAX)}$) must accommodate the worst-case input supply voltage allowed by the notebook's AC adapter voltage. The minimum value ($V_{IN(MIN)}$) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum load current:** There are two values to consider. The peak load current ($I_{LOAD(MAX)}$) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Most notebook loads generally exhibit $I_{LOAD} = I_{LOAD(MAX)}$ x 80%.
- **Switching frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that are proportional to frequency and V_{IN}^2. The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.

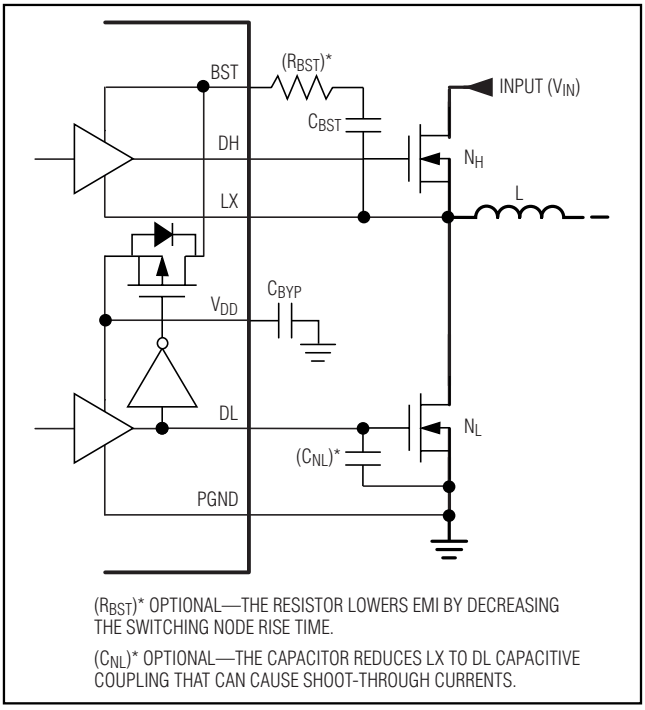

Figure 5. Gate Drive Circuit

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- **Inductor operating point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \left(\frac{V_{IN} - V_{OUT}}{f_{SW} I_{LOAD(MAX)} LIR}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current (I_{PEAK}):

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2}$$

Transient Response

The inductor ripple current impacts transient-response performance, especially at low V_{IN} - V_{OUT} differentials. Low inductor values allow the inductor current to slew faster, replenishing charge removed from the output filter capacitors by a sudden load step. The amount of output sag is also a function of the maximum duty factor, which can be calculated from the on-time and minimum off-time. The worst-case output sag voltage can be determined by:

$$V_{SAG} = \frac{L(\Delta I_{LOAD(MAX)})^2\left[\left(\frac{V_{OUT} T_{SW}}{V_{IN}}\right) + t_{OFF(MIN)}\right]}{2C_{OUT}V_{OUT}\left[\left(\frac{(V_{IN} - V_{OUT})T_{SW}}{V_{IN}}\right) - t_{OFF(MIN)}\right]}$$

where $t_{OFF(MIN)}$ is the minimum off-time (see the *Electrical Characteristics* table).

The amount of overshoot due to stored inductor energy when the load is removed can be calculated as:

$$V_{SOAR} \approx \frac{(\Delta I_{LOAD(MAX)})^2 L}{2C_{OUT}V_{OUT}}$$

Setting the Valley Current Limit

The minimum current-limit threshold must be high enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at $I_{LOAD(MAX)}$ minus half the inductor ripple current (ΔI_L), therefore:

$$I_{LIMIT(LOW)} > I_{LOAD(MAX)} - \frac{\Delta I_L}{2}$$

where $I_{LIMIT(LOW)}$ equals the minimum current-sense threshold voltage (see the *Electrical Characteristics* table) divided by the low-side MOSFET sense resistance R_{CS}.

Output Capacitor Selection

The output filter capacitor must have low-enough effective series resistance (ESR) to meet output ripple and load-transient requirements. Additionally, the ESR impacts stability requirements. Capacitors with a high ESR value (polymers/tantalums) do not need additional external compensation components.

In core and chipset converters and other applications where the output is subject to large-load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \le \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In low-voltage applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR. The maximum ESR to meet ripple requirements is:

$$R_{ESR} \le \left[\frac{V_{IN} f_{SW} L}{(V_{IN} - V_{OUT})V_{OUT}}\right] V_{RIPPLE}$$

where f_{SW} is the switching frequency.

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Single Quick-PWM Step-Down Controller with Dynamic REFIN

With most chemistries (polymer, tantalum, aluminum electrolytic), the actual capacitance value required relates to the physical size needed to achieve low ESR and the chemistry limits of the selected capacitor technology. Ceramic capacitors provide low ESR, but the capacitance and voltage rating (after derating) are determined by the capacity needed to prevent V_{SAG} and V_{SOAR} from causing problems during load transients. Generally, once enough capacitance is added to meet the overshoot requirement, undershoot at the rising load edge is no longer a problem (see the V_{SAG} and V_{SOAR} equations in the *Transient Response* section). Thus, the output capacitor selection requires carefully balancing capacitor chemistry limitations (capacitance vs. ESR vs. voltage rating) and cost. See Figure 6.

Output Capacitor Stability Considerations

For Quick-PWM controllers, stability is determined by the in-phase feedback ripple relative to the switching frequency, which is typically dominated by the output ESR. The boundary of instability is given by the following equation:

$$\frac{f_{SW}}{\pi} \geq \frac{1}{2\pi R_{EFF} C_{OUT}}$$

$$R_{EFF} = R_{ESR} + R_{PCB} + R_{COMP}$$

where C_{OUT} is the total output capacitance, R_{ESR} is the total equivalent-series resistance of the output capacitors, R_{PCB} is the parasitic board resistance between the output capacitors and feedback sense point, and R_{COMP} is the effective resistance of the DC- or AC-coupled current-sense compensation (see Figure 8).

For a standard 300kHz application, the effective zero frequency must be well below 95kHz, preferably below 50kHz. With these frequency requirements, standard tantalum and polymer capacitors already commonly used have typical ESR zero frequencies below 50kHz, allowing the stability requirements to be achieved without any additional current-sense compensation. In the standard application circuit (Figure 1), the ESR needed to support a 15mV$_{P-P}$ ripple is 15mV / (10A x 0.3) = 5mΩ. Two 330µF, 9mΩ polymer capacitors in parallel provide 4.5mΩ (max) ESR and 1 / (2π x 330µF x 9mΩ) = 53kHz ESR zero frequency. See Figure 7.

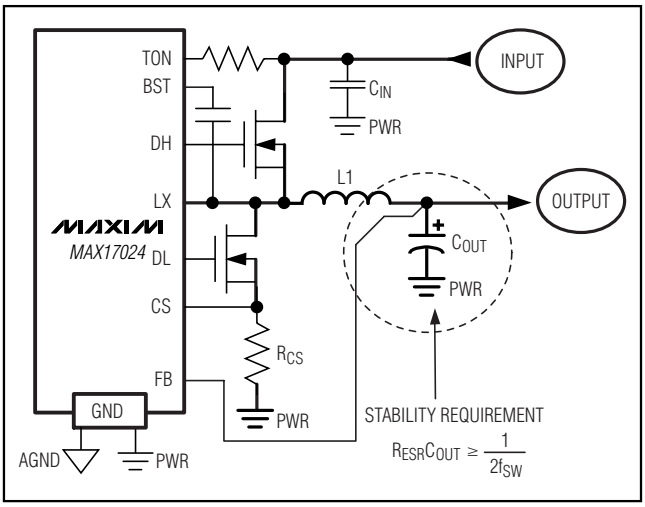

Figure 6. Standard Application with Output Polymer or Tantalum

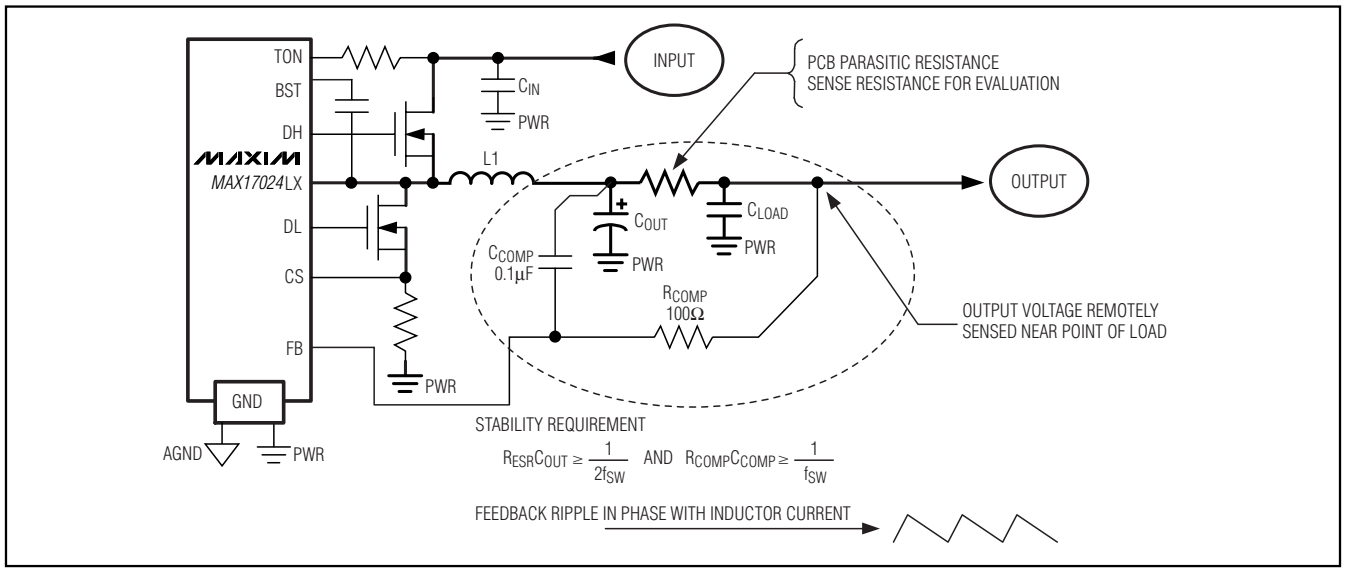

Figure 7. Remote-Sense Compensation for Stability and Noise Immunity

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Ceramic capacitors have a high-ESR zero frequency, but applications with sufficient current-sense compensation can still take advantage of the small size, low ESR, and high reliability of the ceramic chemistry. Using the inductor DCR, applications using ceramic output capacitors can be compensated using either a DC-compensation or AC-compensation method (Figure 8). The DC-coupling requires fewer external compensation capacitors, but this also creates an output load line that depends on the inductor's DCR (parasitic resistance). Alternatively, the current-sense information may be AC-coupled, allowing stability to be dependent only on the inductance value and compensation components and eliminating the DC load line.

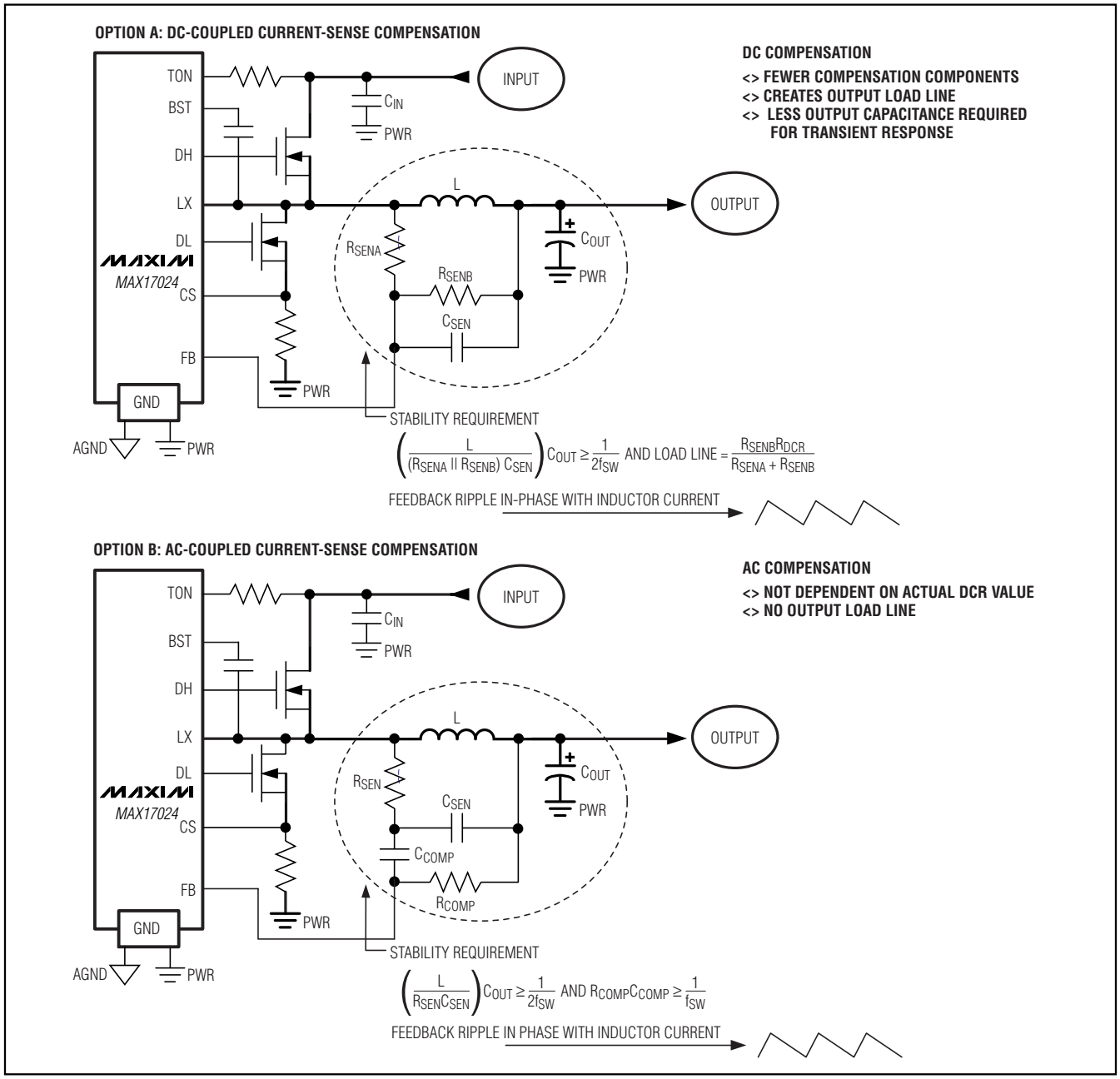

Figure 8. Feedback Compensation for Ceramic Output Capacitors

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Single Quick-PWM Step-Down Controller with Dynamic REFIN

When only using ceramic output capacitors, output overshoot (V_{SOAR}) typically determines the minimum output capacitance requirement. Their relatively low capacitance value may allow significant output overshoot when stepping from full-load to no-load conditions, unless designed with a small inductance value and high switching frequency to minimize the energy transferred from the inductor to the capacitor during load-step recovery.

Unstable operation manifests itself in two related but distinctly different ways: double pulsing and feedback-loop instability. Double pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after the minimum off-time period has expired. Double pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it can indicate the possible presence of loop instability due to insufficient ESR. Loop instability can result in oscillations at the output after line or load steps. Such perturbations are usually damped, but can cause the output voltage to rise above or fall below the tolerance limits.

The easiest method for checking stability is to apply a very fast zero-to-max load transient and carefully observe the output voltage-ripple envelope for overshoot and ringing. It can help to simultaneously monitor the inductor current with an AC current probe. Do not allow more than one cycle of ringing after the initial step-response under/overshoot.

Input Capacitor Selection

The input capacitor must meet the ripple current requirement (I_{RMS}) imposed by the switching currents. The I_{RMS} requirements can be determined by the following equation:

$$I_{RMS} = \left(\frac{I_{LOAD}}{V_{IN}}\right)\sqrt{V_{OUT}(V_{IN} - V_{OUT})}$$

The worst-case RMS current requirement occurs when operating with $V_{IN} = 2V_{OUT}$. At this point, the above equation simplifies to $I_{RMS} = 0.5 \times I_{LOAD}$.

For most applications, nontantalum chemistries (ceramic, aluminum, or OS-CON) are preferred due to their resistance to inrush surge currents typical of systems with a mechanical switch or connector in series with the input. If the Quick-PWM controller is operated as the second stage of a two-stage power-conversion system, tantalum input capacitors are acceptable. In either configuration, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal circuit longevity.

Power-MOSFET Selection

Most of the following MOSFET guidelines focus on the challenge of obtaining high load-current capability when using high-voltage (> 20V) AC adapters. Low-current applications usually require less attention.

The high-side MOSFET (N_H) must be able to dissipate the resistive losses plus the switching losses at both $V_{IN(MIN)}$ and $V_{IN(MAX)}$. Calculate both these sums. Ideally, the losses at $V_{IN(MIN)}$ should be roughly equal to losses at $V_{IN(MAX)}$, with lower losses in between. If the losses at $V_{IN(MIN)}$ are significantly higher than the losses at $V_{IN(MAX)}$, consider increasing the size of N_H (reducing $R_{DS(ON)}$ but with higher C_{GATE}). Conversely, if the losses at $V_{IN(MAX)}$ are significantly higher than the losses at $V_{IN(MIN)}$, consider reducing the size of N_H (increasing $R_{DS(ON)}$ to lower C_{GATE}). If V_{IN} does not vary over a wide range, the maximum efficiency occurs where the resistive losses equal the switching losses.

Choose a low-side MOSFET that has the lowest possible on-resistance ($R_{DS(ON)}$), comes in a moderate-sized package (i.e., one or two 8-pin SOs, DPAK, or D^2PAK), and is reasonably priced. Make sure that the DL gate driver can supply sufficient current to support the gate charge and the current injected into the parasitic gate-to-drain capacitor caused by the high-side MOSFET turning on; otherwise, cross-conduction problems may occur (see the *MOSFET Gate Drivers* section).

MOSFET Power Dissipation

Worst-case conduction losses occur at the duty factor extremes. For the high-side MOSFET (N_H), the worst-case power dissipation due to resistance occurs at the minimum input voltage:

$$PD\ (N_H\ \text{Resistive}) = \left(\frac{V_{OUT}}{V_{IN}}\right)(I_{LOAD})^2 R_{DS(ON)}$$

Generally, a small high-side MOSFET is desired to reduce switching losses at high-input voltages. However, the $R_{DS(ON)}$ required to stay within package-power dissipation often limits how small the MOSFET can be. Again, the optimum occurs when the switching losses equal the conduction ($R_{DS(ON)}$) losses. High-side switching losses do not usually become an issue until the input is greater than approximately 15V.

Calculating the power dissipation in the high-side MOSFET (N_H) due to switching losses is difficult since it must allow for difficult quantifying factors that influence the turn-on and turn-off times. These factors include the internal gate resistance, gate charge, threshold voltage, source inductance, and PCB layout characteristics. The following switching-loss calculation provides only a very

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rough estimate and is no substitute for breadboard evaluation, preferably including verification using a thermocouple mounted on N_H:

$$PD\,(N_H\ Switching) = V_{IN(MAX)} I_{LOAD} f_{SW} \left(\frac{Q_{G(SW)}}{I_{GATE}} \right) + \frac{C_{OSS} V_{IN(MAX)}^2 f_{SW}}{2}$$

where C_{OSS} is the N_H MOSFET's output capacitance, $Q_{G(SW)}$ is the charge needed to turn on the N_H MOSFET, and I_{GATE} is the peak gate-drive source/sink current (2.4A typ).

Switching losses in the high-side MOSFET can become an insidious heat problem when maximum AC adapter voltages are applied, due to the squared term in the C x V_{IN}^2 x f_{SW} switching-loss equation. If the high-side MOSFET chosen for adequate $R_{DS(ON)}$ at low battery voltages becomes extraordinarily hot when biased from $V_{IN(MAX)}$, consider choosing another MOSFET with lower parasitic capacitance.

For the low-side MOSFET (N_L), the worst-case power dissipation always occurs at maximum input voltage:

$$PD\ (N_L\ \ Resistive) = \left[1 - \left(\frac{V_{OUT}}{V_{IN(MAX)}} \right) \right] (I_{LOAD})^2 R_{DS(ON)}$$

The worst case for MOSFET power dissipation occurs under heavy overloads that are greater than $I_{LOAD(MAX)}$, but are not quite high enough to exceed the current limit and cause the fault latch to trip. To protect against this possibility, you can "overdesign" the circuit to tolerate:

$$I_{LOAD} = I_{VALLEY(MAX)} + \frac{\Delta I_L}{2} = I_{VALLEY(MAX)} + \left(\frac{I_{LOAD(MAX)} LIR}{2} \right)$$

where $I_{VALLEY(MAX)}$ is the maximum valley current allowed by the current-limit circuit, including threshold tolerance and on-resistance variation. The MOSFETs must have a good size heatsink to handle the overload power dissipation.

Choose a Schottky diode (D_L) with a forward voltage low enough to prevent the low-side MOSFET body diode from turning on during the dead time. Select a diode that can handle the load current during the dead times. This diode is optional and can be removed if efficiency is not critical.

Boost Capacitors

The boost capacitors (C_{BST}) must be selected large enough to handle the gate-charging requirements of the high-side MOSFETs. Typically, 0.1µF ceramic capacitors work well for low-power applications driving medium-sized MOSFETs. However, high-current applications driving large, high-side, MOSFETs require boost capacitors larger than 0.1µF. For these applications, select the boost capacitors to avoid discharging the capacitor more than 200mV while charging the high-side MOSFETs' gates:

$$C_{BST} = \frac{N \times Q_{GATE}}{200mV}$$

where N is the number of high-side MOSFETs used for one regulator, and Q_{GATE} is the gate charge specified in the MOSFET's data sheet. For example, assume (2) IRF7811W n-channel MOSFETs are used on the high side. According to the manufacturer's data sheet, a single IRF7811W has a maximum gate charge of 24nC (V_{GS} = 5V). Using the above equation, the required boost capacitance would be:

$$C_{BST} = \frac{2 \times 24nC}{200mV} = 0.24\mu F$$

Selecting the closest standard value, this example requires a 0.22µF ceramic capacitor.

Minimum Input-Voltage Requirements and Dropout Performance

The output voltage-adjustable range for continuous-conduction operation is restricted by the nonadjustable minimum off-time one-shot. For best dropout performance, use the slower (200kHz) on-time settings. When working with low-input voltages, the duty-factor limit must be calculated using worst-case values for on- and off-times. Manufacturing tolerances and internal propagation delays introduce an error to the on-times. This error is greater at higher frequencies. Also, keep in mind that transient response performance of buck regulators operated too close to dropout is poor, and bulk output capacitance must often be added (see the V_{SAG} equation in the *Transient Response* section).

The absolute point of dropout is when the inductor current ramps down during the minimum off-time (ΔI_{DOWN}) as much as it ramps up during the on-time (ΔI_{UP}). The ratio h = ΔI_{UP} / ΔI_{DOWN} is an indicator of the ability to slew the inductor current higher in response to increased load, and must always be greater than 1. As h approaches 1, the absolute minimum dropout point, the inductor current cannot increase as much during each switching cycle and V_{SAG} greatly increases unless additional output capacitance is used.

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A reasonable minimum value for h is 1.5, but adjusting this up or down allows trade-offs between V_{SAG}, output capacitance, and minimum operating voltage. For a given value of h, the minimum operating voltage can be calculated as:

$$V_{IN(MIN)} = \left(\frac{V_{FB} - V_{DROOP} + V_{CHG}}{1 - \left(h \times t_{OFF(MIN)} f_{SW}\right)} \right)$$

where V_{FB} is the voltage-positioning droop, V_{CHG}, is the parasitic voltage drop in the charge path, and $t_{OFF(MIN)}$ is from the *Electrical Characteristics* table. The absolute minimum input voltage is calculated with h = 1.

If the calculated $V_{IN(MIN)}$ is greater than the required minimum input voltage, then reduce the operating frequency or add output capacitance to obtain an acceptable V_{SAG}. If operation near dropout is anticipated, calculate V_{SAG} to be sure of adequate transient response.

Dropout design example:

V_{FB} = 1.5V

f_{SW} = 300kHz

$t_{OFF(MIN)}$ = 350ns

No droop/load line (V_{DROOP} = 0)

$V_{DROPCHG}$ = 150mV (10A load)

h = 1.5:

$$V_{IN(MIN)} = \left[\frac{1.5V - 0V + 150mV}{1 - (1.5 \times 350ns \times 300kHz)} \right] = 1.96V$$

Calculating again with h = 1 gives the absolute limit of dropout:

$$V_{IN(MIN)} = \left[\frac{1.5V - 0V + 150mV}{1 - (1.0 \times 350ns \times 300kHz)} \right] = 1.84V$$

Therefore, V_{IN} must be greater than 1.84V, even with very large output capacitance, and a practical input voltage with reasonable output capacitance would be 2.0V.

Applications Information

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. The switching power stage requires particular attention. If possible, mount all the power components on the top side of the board with their ground terminals flush against one another. Follow these guidelines for good PCB layout:

- Keep the high-current paths short, especially at the ground terminals. This is essential for stable, jitter-free operation.
- Connect all analog grounds to a separate solid copper plane, which connects to the GND pin of the Quick-PWM controller. This includes the V_{CC} bypass capacitor, REF bypass capacitors, REFIN components, and feedback compensation/dividers.
- Keep the power traces and load connections short. This is essential for high efficiency. The use of thick copper PCBs (2oz vs. 1oz) can enhance full-load efficiency by 1% or more. Correctly routing PCB traces is a difficult task that must be approached in terms of fractions of centimeters, where a single mΩ of excess trace resistance causes a measurable efficiency penalty.
- Keep the high-current, gate-driver traces (DL, DH, LX, and BST) short and wide to minimize trace resistance and inductance. This is essential for high-power MOSFETs that require low-impedance gate drivers to avoid shoot-through currents.
- When trade-offs in trace lengths must be made, it is preferable to allow the inductor charging path to be made longer than the discharge path. For example, it is better to allow some extra distance between the input capacitors and the high-side MOSFET than to allow distance between the inductor and the low-side MOSFET or between the inductor and the output filter capacitor.
- Route high-speed switching nodes away from sensitive analog areas (REF, REFIN, FB).

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Layout Procedure

1) Place the power components first, with ground terminals adjacent (low-side MOSFET source, C_{IN}, C_{OUT}, and D1 anode). If possible, make all these connections on the top layer with wide, copper-filled areas.
2) Mount the controller IC adjacent to the low-side MOSFET. The DL gate traces must be short and wide (50 mils to 100 mils wide if the MOSFET is 1in from the controller IC).
3) Group the gate-drive components (BST capacitors, V_{DD} bypass capacitor) together near the controller IC.
4) Make the DC-DC controller ground connections as shown in Figure 1. This diagram can be viewed as having 4 separate ground planes: input/output ground, where all the high-power components go; the power ground plane, where the GND pin and V_{DD} bypass capacitor go; the controller's analog ground plane where sensitive analog components, the controller's GND pin, and V_{CC} bypass capacitor go. The controller's ground plane must meet the power ground plane only at a single point directly beneath the IC (this si done automatically inside the MAX17024 through the back pad). These ground planes should connect to the high-power output ground with a short metal trace from GND (back pad) to the source of the low-side MOSFET (the middle of the star ground). This point must also be very close to the output capacitor ground terminal.
5) Connect the output power planes (V_{CORE} and system ground planes) directly to the output filter capacitor positive and negative terminals with multiple vias. Place the entire DC-DC converter circuit as close to the load as is practical.

Chip Information

TRANSISTOR COUNT: 7169

PROCESS: BiCMOS

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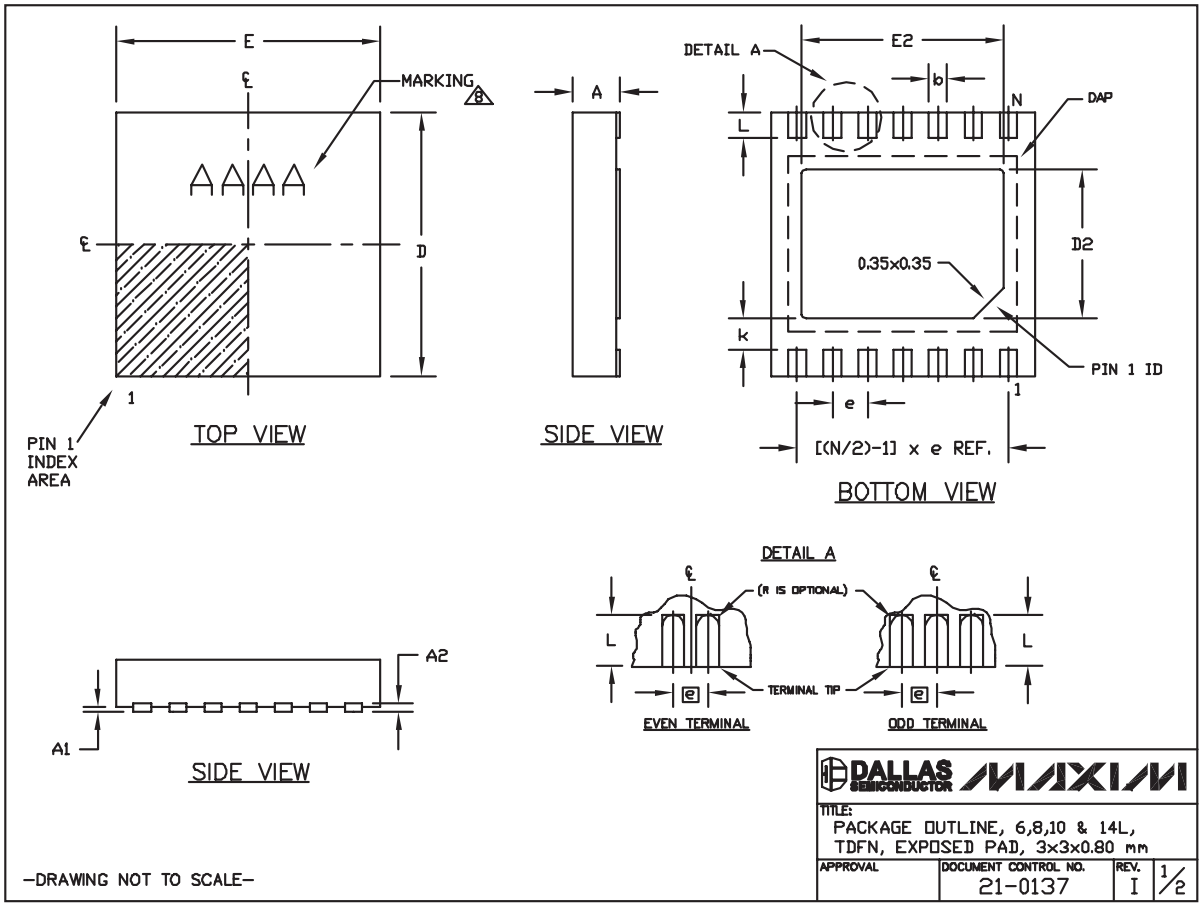
Single Quick-PWM Step-Down Controller with Dynamic REFIN

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	I	2/2

-DRAWING NOT TO SCALE-

Note: *MAX17024ETD+ Package Code = T1433-1*

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