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1 Description

The M27W512 is a low-voltage, 512 Kbit OTP (one-time programmable) EPROM. It is ideally suited to microprocessor systems and are organized as 65536 by 8 bits.

The M27W512 operates in the read mode with a supply voltage as low as 2.7 V at –40 to 85 °C temperature range. The decrease in operating power allows either a reduction of the size of the battery or an increase in the time between battery recharges.

For applications where the content is programmed only one time and erasure is not required, the M27W512 is offered in PLCC32 packages.

Figure 1. Logic diagram

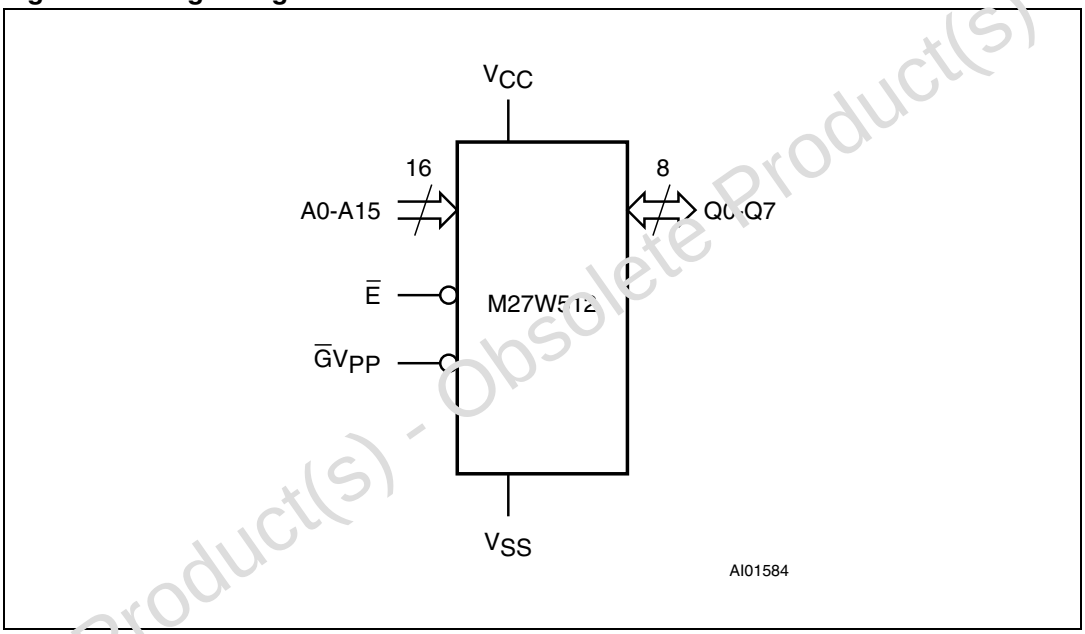
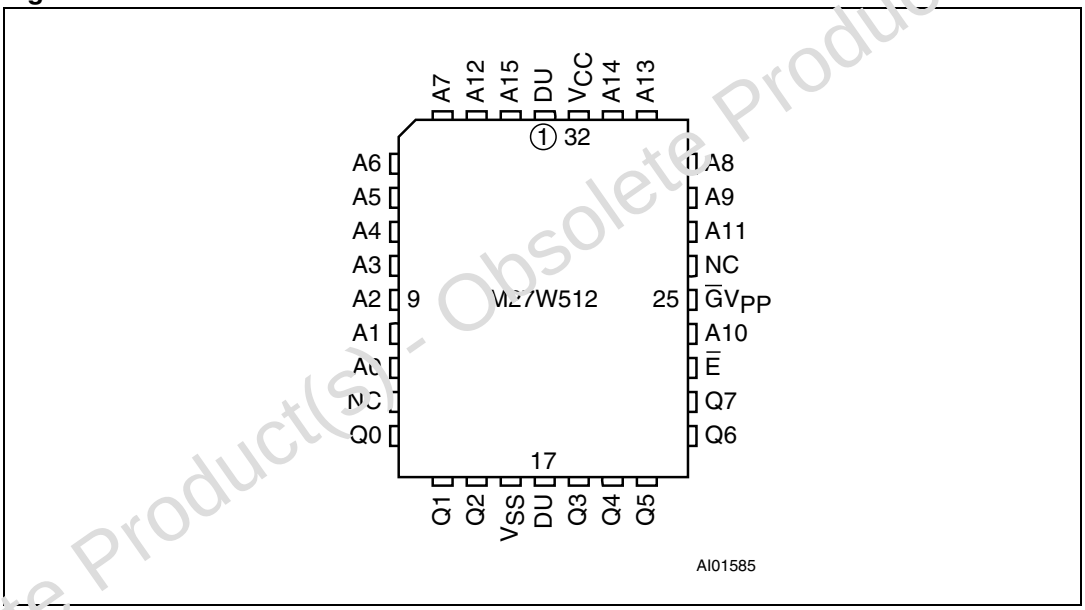


Table 1. Signal names

Signal names	Function
A0-A15	Address inputs
Q0-Q7	Data outputs
$\overline{E}$	Chip Enable
GV_{PP}	Output Enable / Program supply
V_{CC}	Supply voltage
V_{SS}	Ground
NC	Not connected internally
DU	Don't use

Figure 2. LCC connections



2 Device operation

The modes of operations of the M27W512 are listed in *Table 2: Operating modes*. A single power supply is required in the read mode. All inputs are TTL levels except for $\overline{G}V_{PP}$ and 12V on A9 for Electronic Signature.

2.1 Read mode

The M27W512 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{E}$) is the power control and should be used for device selection. Output Enable ($\overline{G}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that the addresses are stable, the address access time (t_{AVQV}) is equal to the delay from $\overline{E}$ to output (t_{ELQV}). Data is available at the output after a delay of t_{GLQV} from the falling edge of $\overline{G}$, assuming that $\overline{E}$ has been low and the addresses have been stable for at least t_{AVQV}-t_{GLQV}.

2.2 Standby mode

The M27W512 has a standby mode which reduces the supply current from 15mA to 15µA with low voltage operation $V_{CC} \leq 3.6V$, see *Table 7: Read mode DC characteristics*.

Characteristics table for details. The M27W512 is placed in the standby mode by applying a CMOS high signal to the $\overline{E}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{G}V_{PP}$ input.

Table 2. Operating modes(1)

Mode	$\overline{E}$	$\overline{G}V_{PP}$	A9	Q7-Q0
Read	V_{IL}	V_{IL}	X	Data Out
Output Disable	V_{IL}	V_{IH}	X	Hi-Z
Program	V_{IL} Pulse	V_{PP}	X	Data In
Program Inhibit	V_{IH}	V_{PP}	X	Hi-Z
Standby	V_{IH}	X	X	Hi-Z
Electronic Signature	V_{IL}	V_{IL}	V_{ID}	Codes

1. X = V_{IH} or V_{IL}, V_{ID} = 12V ± 0.5V.

Table 3. Electronic signature

Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex data
Manufacturer code	V_{IL}	0	0	1	0	0	0	0	0	20h
Device code	V_{IH}	0	0	1	1	1	1	0	1	3Dh

2.3 Two line output control

Because EPROMs are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- The lowest possible memory power dissipation
- Complete assurance that output bus contention will not occur.

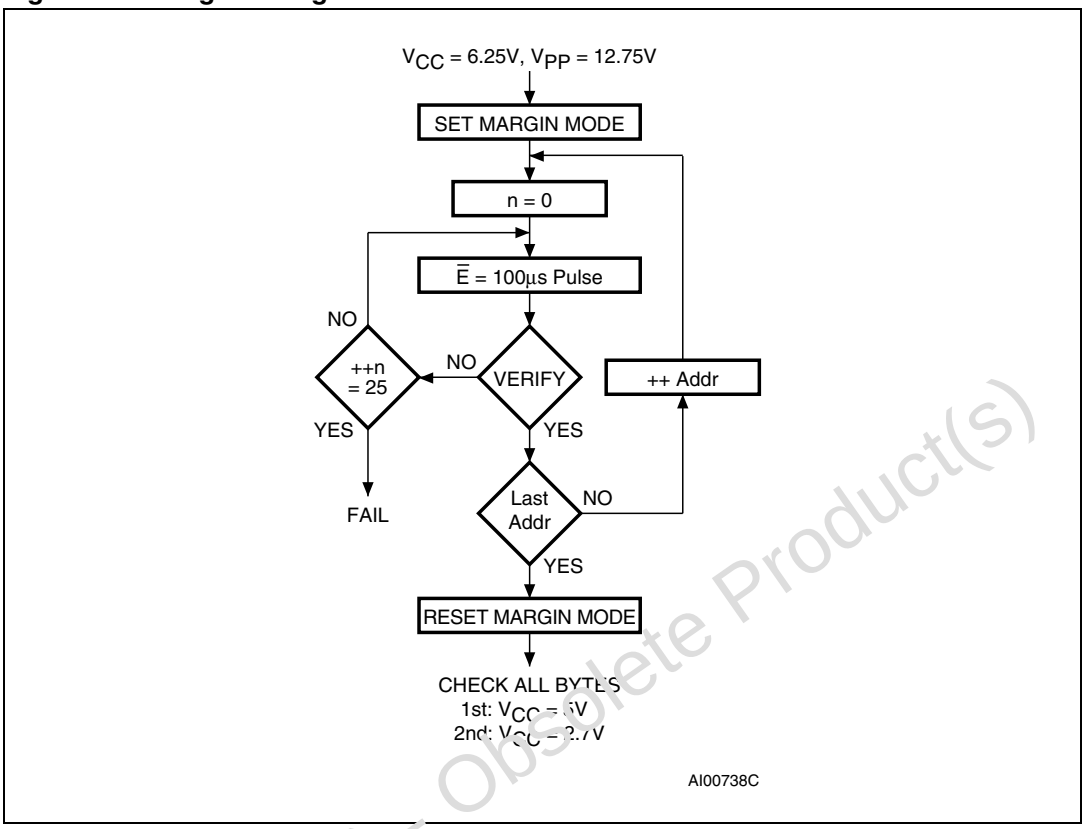
For the most efficient use of these two control lines, $\overline{E}$ should be decoded and used as the primary device selecting function, while $\overline{G}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

2.4 System considerations

The power switching characteristics of Advanced CMOS EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of $\overline{E}$. The magnitude of the transient current peaks is dependent on the capacitive and inductive loading of the device at the output.

The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a 0.1µF ceramic capacitor be used on every device between V_{CC} and V_{SS}. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for every eight devices. The bulk capacitor should be located near the power supply connection point.The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

Figure 3. Programming flowchart



2.5 Programming

The M27W512 has been designed to be fully compatible with the M27C512 and has the same electronic signature. As a result, the M27W512 can be programmed as the M27C512 on the same programming equipment applying 12.75V on V_{PP} and 6.25V on V_{CC}. The M27W512 can use PRESTO IIB Programming Algorithm that drastically reduces the programming time. Nevertheless to achieve compatibility with all programming equipment, PRESTO II Programming Algorithm can be used as well. When delivered, all bits of the M27W512 are in the '1' state. Data is introduced by selectively programming '0's into the desired bit locations. Although only '0's will be programmed, both '1's and '0's can be present in the data word. The M27W512 is in the programming mode when V_{PP} input is at 12.75V and $\overline{E}$ is pulsed to V_{IL}. The data to be programmed is applied to 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL. V_{CC} is specified to be 6.25V ± 0.25V.

2.6 PRESTO IIB programming algorithm

PRESTO IIB programming algorithm allows the whole array to be programmed with a guaranteed margin, in a typical time of 6.5 seconds. This can be achieved with STMicroelectronics M27W512 due to several design innovations described in the M27W512 datasheet to improve programming efficiency and to provide adequate margin for reliability. Before starting the programming the internal MARGIN MODE circuit must be set in order to guarantee that each cell is programmed with enough margin. Then a sequence of 100µs program pulses is applied to each byte until a correct verify occurs (see *Figure 3*). No overprogram pulses are applied since the verify in MARGIN MODE at V_{CC} much higher than 3.6V, provides the necessary margin.

2.7 Program inhibit

Programming of multiple devices in parallel with different data is also easily accomplished. Except for $\overline{E}$, all like inputs including $\overline{G}V_{PP}$ of the parallel M27W512 may be common. A TTL low level pulse applied to a M27W512 $\overline{E}$ input, with V_{PP} at 12.75V, will program this device. A high level $\overline{E}$ input inhibits the other M27W512 from being programmed.

2.8 Program verify

A verify (read) should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{G}$ at V_{IL}. Data should be verified with t_{ELQV} after the falling edge of $\overline{E}$.

2.9 Electronic signature

The Electronic Signature (ES) mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. The ES mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the M27W512. To activate the ES mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27W512. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during Electronic Signature mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the STMicroelectronics M27W512, these two identifier bytes are given in *Table 3* and can be read-out on outputs Q7 to Q0.

Note that the M27W512 and M27C512 have the same identifier byte.

3 Maximum rating

Stressing the device outside the ratings listed in *Table 4* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
T_A	Ambient operating temperature(1)	–40 to 125	°C
T_{BIAS}	Temperature under bias	–50 to 125	°C
T_{STG}	Storage temperature	–65 to 150	°C
V_{IO}(2)	Input or output voltage (except A9)	–2 to 7	V
V_{CC}	Supply voltage	–2 to 7	V
V_{A9}(2)	A9 voltage	–2 to 13.5	V
V_{PP}	Program supply voltage	–2 to 14	V

1. Depends on range.
2. Minimum DC voltage on input or output is –0.5V with possible undershoot to –2.0V for a period less than 20ns. Maximum DC voltage on Output is V_{CC} +0.5V with possible overshoot to V_{CC} +2V for a period less than 20ns.

4 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 5. AC measurement conditions

	High speed	Standard
Input rise and fall times	≤10ns	≤20ns
Input pulse voltages	0 to 3V	0.4V to 2.4V
Input and output timing ref. voltages	1.5V	0.8V and 2V

Figure 4. AC testing input output waveform

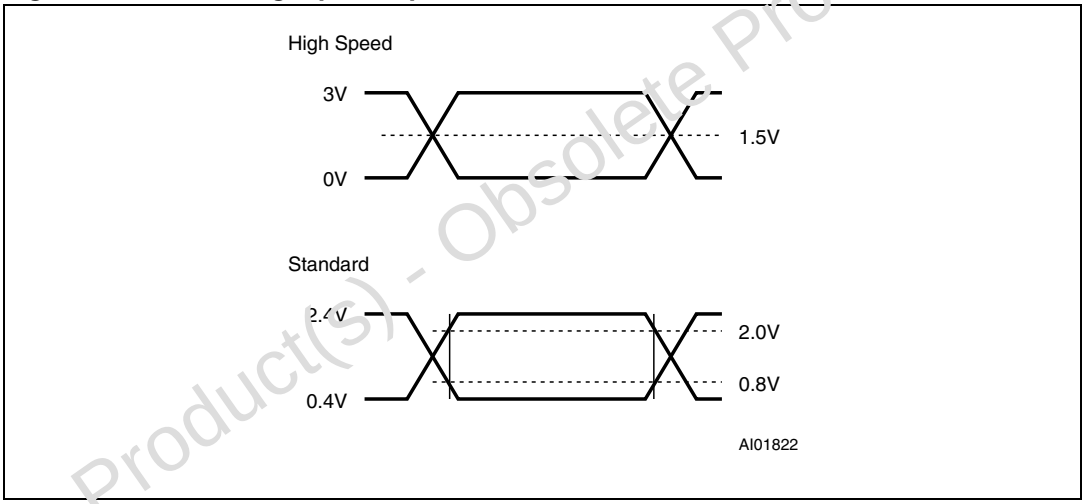


Figure 5. AC testing load circuit

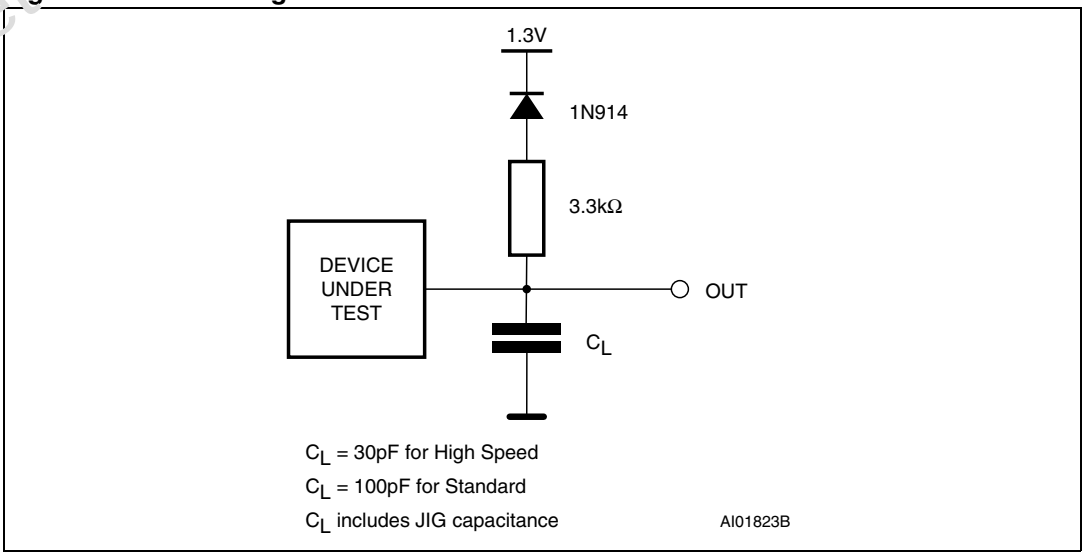


Table 6. Capacitance

Symbol	Parameter	Test condition(1)(2)	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0V		12	pF

1. T_A = 25°C, f = 1MHz
2. Sampled only, not 100% tested.

Table 7. Read mode DC characteristics

Symbol	Parameter	Test condition(1)	Min	Max	Unit
I_{LI}	Input leakage current	0V ≤V_{IN} ≤V_{CC}		±10	µA
I_{LO}	Output leakage current	0V ≤V_{OUT} ≤V_{CC}		±10	µA
I_{CC}	Supply current	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}, I_{OUT} = 0mA, f = 5MHz V_{CC} ≤3.6V		15	mA
I_{CC1}	Supply current (Standby) TTL	$\overline{E}$ = V_{IH}		1	mA
I_{CC2}	Supply current (Standby) CMOS	$\overline{E}$ > V_{CC} – 0.2V, V_{CC} ≤3.6V		15	µA
I_{PP}	Program current	V_{PP} = V_{CC}		10	µA
V_{IL}	Input low voltage		–0.6	0.2 V_{CC}	V
V_{IH}(2)	Input high voltage		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output high voltage TTL	I_{OH} = –1mA	2.4		V

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Maximum DC voltage on Output is V_{CC} +0.5V.

Table 8. Read mode AC characteristics

Symbol	Alt	Parameter	Test condition (1)	M27W512						Unit
				-70(2)		-80(2)		-100		
				V_{CC} = 3.0 to 3.6V		V_{CC} = 2.7 to 3.6V		V_{CC} = 2.7 to 3.6V		
				Min	Max	Min	Max	Min	Max	
t_{AVQV}	t_{ACC}	Address valid to output valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		80		100	ns
t_{ELQV}	t_{CE}	Chip Enable low to output valid	$\overline{G}$ = V_{IL}		70		80		100	ns
t_{GLQV}	t_{OE}	Output Enable low to output valid	$\overline{E}$ = V_{IL}		40		50		60	ns
t_{EHQZ}(3)	t_{DF}	Chip Enable high to output Hi-Z	$\overline{G}$ = V_{IL}	0	40	0	50		60	ns
t_{GHQZ}(3)	t_{DF}	Output Enable high to output Hi-Z	$\overline{E}$ = V_{IL}	0	40	0	50		60	ns
t_{AXQX}	t_{OH}	Address transition to output transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	0		0				ns

1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
2. Speed obtained with High Speed AC measurement conditions.
3. Sampled only, not 100% tested.

Figure 6. Read mode AC waveforms

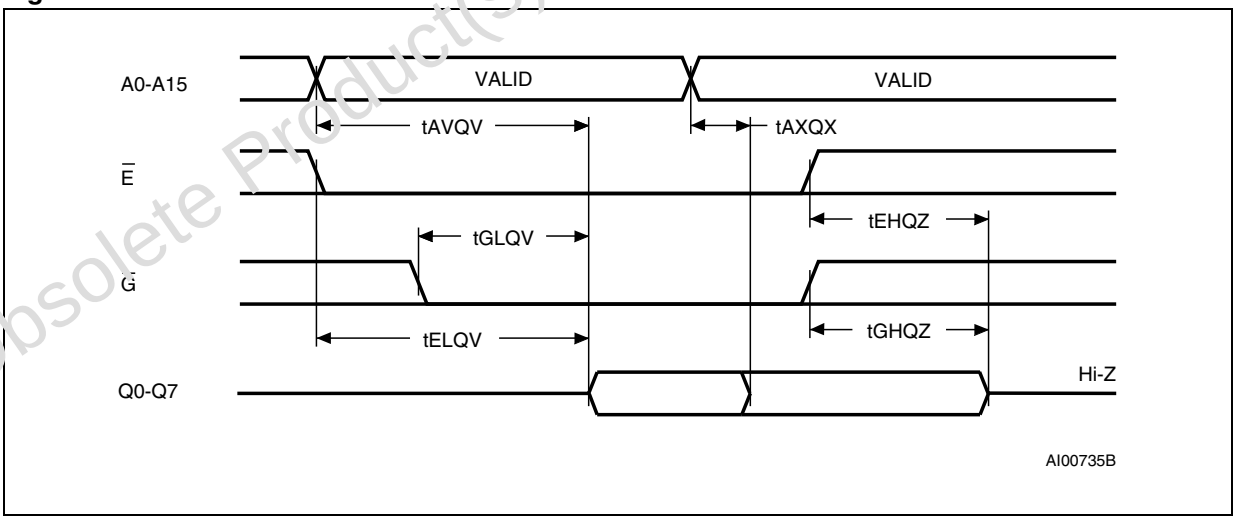


Table 9. Programming mode DC characteristics

Symbol	Parameter	Test condition(1)(2)	Min	Max	Unit
I_{LI}	Input leakage current	$V_{IL} \le V_{IN} \le V_{IH}$		±10	µA
I_{CC}	Supply current			50	mA
I_{PP}	Program current	$\overline{E} = V_{IL}$		50	mA
V_{IL}	Input low voltage		–0.3	0.8	V
V_{IH}	Input high voltage		2	V_{CC} + 0.5	V
V_{OL}	Output low voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output high voltage TTL	I_{OH} = –1mA	3.6		V
V_{ID}	A9 voltage		11.5	12.5	V

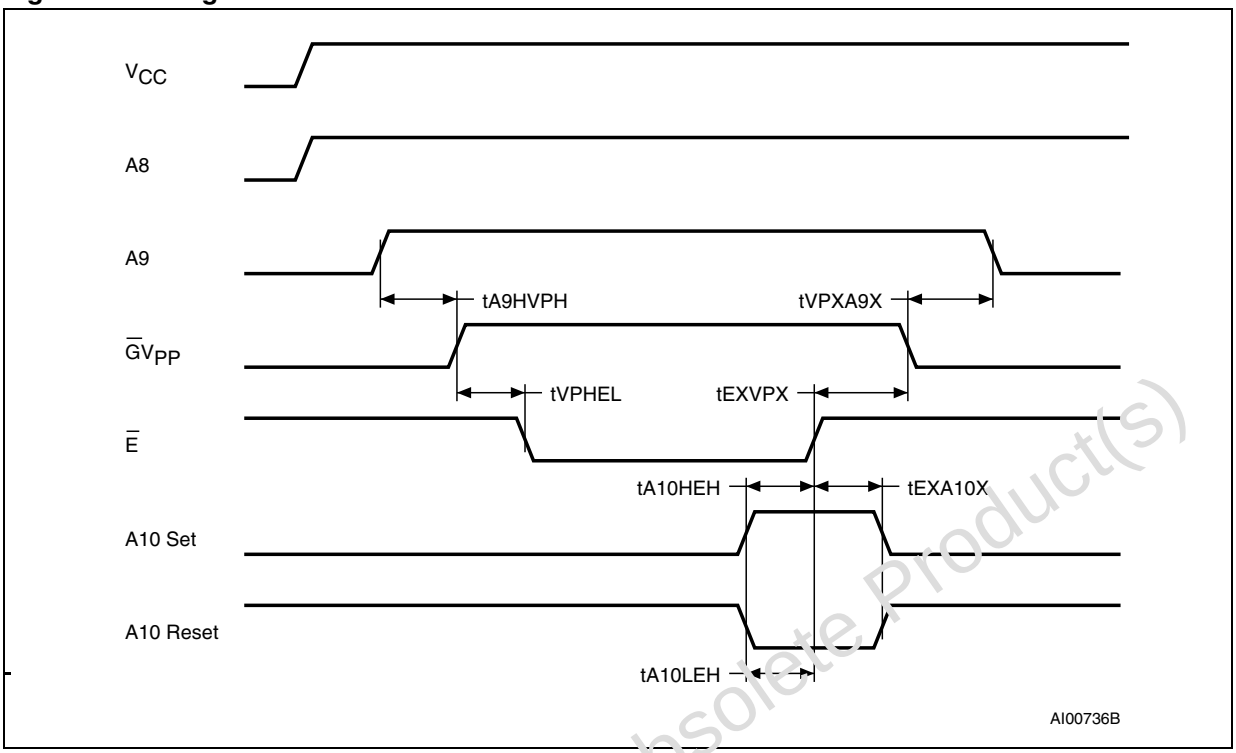
1. T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Table 10. Margin mode AC characteristics

Symbol	Alt	Parameter	Test condition(1)(2)	Min	Max	Unit
t_{A9HVPH}	t_{AS9}	V_{A9} high to V_{PP} high		2		µs
t_{VPHEL}	t_{VPS}	V_{PP} high to Chip Enable low		2		µs
t_{A10HEH}	t_{AS10}	V_{A10} high to Chip Enable high (set)		1		µs
t_{A10LEH}	t_{AS10}	V_{A10} low to Chip Enable high (reset)		1		µs
t_{EXA10X}	t_{AH10}	Chip Enable transition to V_{A10} transition		1		µs
t_{EXVPX}	t_{VPH}	Chip Enable transition to V_{PP} transition		2		µs
t_{VPXA9X}	t_{AH9}	V_{PP} transition to V_{A9} transition		2		µs

1. T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.

Figure 7. Margin mode AC waveforms



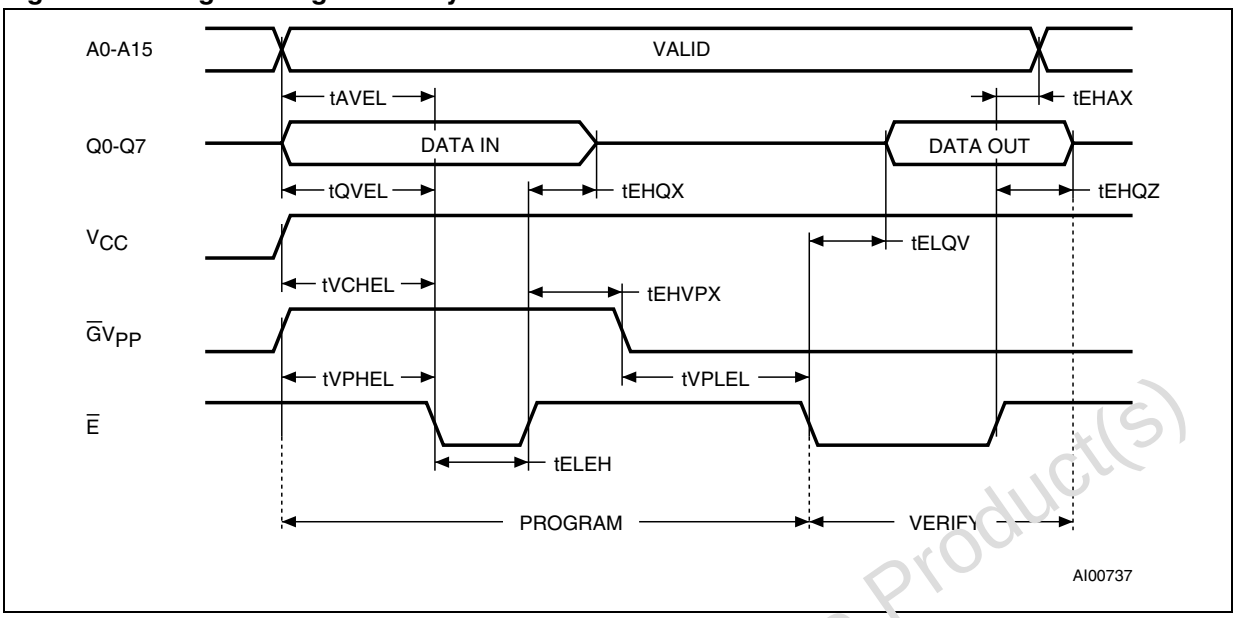
1. A8 High level = 5V; A9 High level = 12V.

Table 11. Programming mode AC characteristics

Symbol	Alt	Parameter	Test condition(1)(2)	Min	Max	Unit
t_{AVEL}	t_{AS}	Address valid to Chip Enable low		2		µs
t_{QVEL}	t_{DS}	Input Valid to Chip Enable low		2		µs
t_{VCHEL}	t_{VCS}	V_{CC} high to Chip Enable low		2		µs
t_{VPHEL}	t_{OES}	V_{PP} high to Chip Enable low		2		µs
t_{VPLVPH}	t_{PRT}	V_{PP} rise time		50		ns
t_{ELEH}	t_{PW}	Chip Enable program pulse width (Initial)		95	105	µs
t_{EHQX}	t_{DH}	Chip Enable high to input transition		2		µs
t_{EHVPX}	t_{OEH}	Chip Enable high to V_{PP} transition		2		µs
t_{VPLEL}	t_{VR}	V_{PP} low to Chip Enable low		2		µs
t_{ELQV}	t_{DV}	Chip Enable low to output valid			1	µs
t_{EHQZ}(3)	t_{DFP}	Chip Enable high to output Hi-Z		0	130	ns
t_{EHAX}	t_{AH}	Chip Enable high to address transition		0		ns

1. T_A = 25 °C; V_{CC} = 6.25V ± 0.25V; V_{PP} = 12.75V ± 0.25V
2. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously or after V_{PP}.
3. Sampled only, not 100% tested.

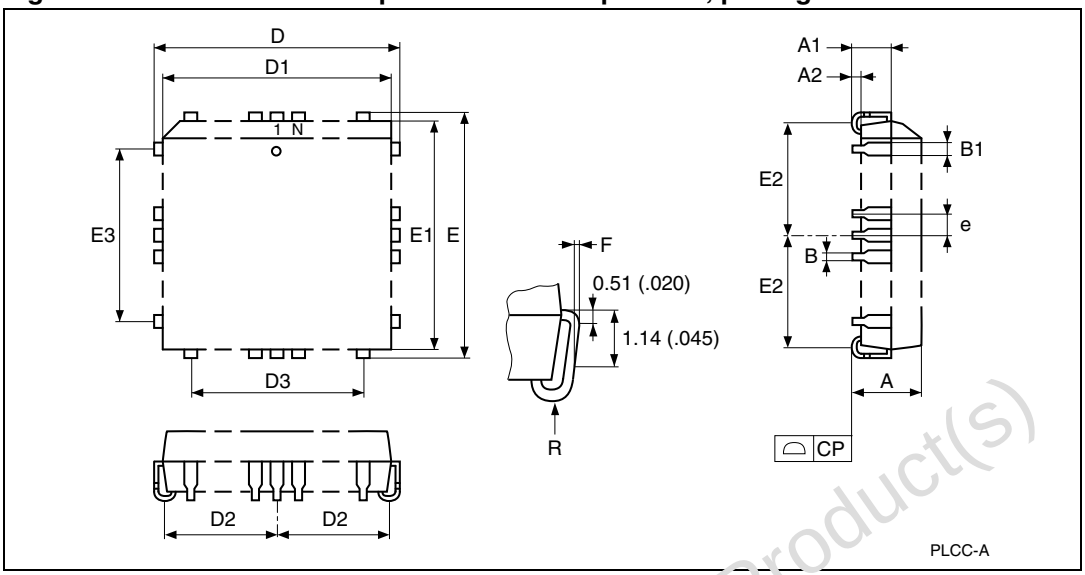
Figure 8. Programming and verify mode AC waveforms



5 Package mechanical data

In order to meet environmental requirements, ST offers the M27W512 in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

Figure 9. PLCC32 - 32 lead plastic leaded chip carrier, package outline



1. Drawing is not to scale.

Table 12. PLCC32 - 32 lead plastic leaded chip carrier, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A		3.175	3.556		0.1250	0.1400
A1		1.530	2.413		0.0602	0.0950
A2		0.381	-		0.0150	-
B		0.330	0.533		0.0130	0.0210
B1		0.660	0.813		0.0260	0.0320
CP			0.100			0.0039
D		12.319	12.573		0.4850	0.4950
D1		11.354	11.506		0.4470	0.4530
D2		4.780	5.660		0.1882	0.2228
D3	7.620	-	-	0.3000	-	-
E		14.859	15.113		0.5850	0.5950
E1		13.894	14.046		0.5470	0.5530
E2		6.050	6.930		0.2382	0.2728
E3	10.160	-	-	0.4000	-	-
e	1.270	-	-	0.0500	-	-
F		0.000	0.127		0.0000	0.0050
R	0.889	-	-	0.0350	-	-
N (number of pins)	32			32		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

6 Part numbering

Table 13. Ordering information scheme

Example: M27W512 -100 K 6 TR

Device type

M27

Supply voltage

W = 2.7 V to 3.6 V

Device function

512 = 512 Kbit (64 Kb x 8)

Speed

-100= 100 ns

Package

K = PLCC32

Temperature range

6 = –40 to 85 °C

Options

Blank = Standard packing

TR = Tape and reel packing

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

7 Revision history

Table 14. Document revision history

Date	Revision	Changes
20-Mar-2000	1.1	FDIP28W Package Dimension, L Max added (*Table 12*) TSOP32 Package Dimension changed (*Table 13*) 0 to 70°C Temperature Range deleted Speed Classes changed
15-Jun-2001	1.2	Typing error (*Table 8*)
30-Aug-2002	1.3	Package mechanical data clarified for FDIP28W (*Table 12*), PDIP28 (*Table 13*), PLCC32 (*Table 12*, *Figure 9*) and TSOP28 (*Table 13*, *Figure 11*)
08-Nov-2004	2.0	Details of ECOPACK lead-free package options added
27-Apr-2007	3	Document reformatted. FDIP28W and PDIP28 packages removed. 120, 150 and 200ns access times removed from *Table 13: Ordering information scheme*.
09-Jun-2008	4	Small text changes. UV range no longer offered (references to UV removed). TSOP28 package removed. Package mechanical data in inches calculated from millimeters and rounded to three decimals (see *Table 12: PLCC32 - 32 lead plastic leaded chip carrier, package mechanical data*). E and F options and 80 ns speed class removed from *Table 13: Ordering information scheme*.

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