# ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Supply Voltage (V1, V2)............................. –14V to 40V

Voltage from V1 or V2 to $V_S$ ....................... –40V to 40V

Input Voltage

   E1, $\overline{E2}$ ................................................ –0.3V to 40V

   $V_S$ ......................................................... –14V to 40V

Output Voltage

   G1 ....... –0.3V to the Higher of V1 + 0.3V or $V_S$ + 0.3V

   G2 ....... –0.3V to the Higher of V2 + 0.3V or $V_S$ + 0.3V

   H1, $\overline{H2}$ ...................................................... –0.3V to 7V

Operating Ambient Temperature Range (Note 2)

   LTC4416E ........................................... –40°C to 85°C

   LTC4416I .......................................... –40°C to 125°C

Operating Junction

Temperature Range................................ –40°C to 125°C

Storage Temperature Range.................... –65°C to 150°C

Lead Temperature (Soldering, 10 sec) .................. 300°C

# PACKAGE/ORDER INFORMATION

```
               TOP VIEW
     H1  1 ┌──────────┐ 10  G1
     E1  2 │          │  9  V1
    GND  3 │          │  8  VS
     E2  4 │          │  7  V2
     H2  5 └──────────┘  6  G2
```
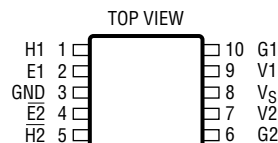
MS PACKAGE
10-LEAD PLASTIC MSOP

$T_{JMAX} = 130°C$, $\theta_{JA} = 120°C/W$

| ORDER PART NUMBER | MS PART MARKING* |
|---|---|
| LTC4416EMS | LTCFC |
| LTC4416IMS | LTCFC |
| LTC4416EMS-1 | LTCPS |
| LTC4416IMS-1 | LTCPS |

**Order Options** Tape and Reel: Add #TR
Lead Free: Add #PBF   Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

*The temperature grade is identified by a label on the shipping container.

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. V1 = V2 = 12V, E1 = 2V, $\overline{E2}$ = GND, GND = 0V. Current into a pin is positive and current out of a pin is negative. All voltages are referenced to GND, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{V1}$, $V_{V2}$, $V_{VS}$ | Operating Supply Range | V1, V2 and/or $V_S$ Must be in This Range for Proper Operation | ● | 3.6 | | 36 | V |
| $I_{QFL}$ | Quiescent Supply Current at Low Supply While in Forward Regulation | $V_{V1}$ = 3.6V, $V_{V2}$ = 3.6V. Measure Combined Current at V1, V2 and $V_S$ Pins Averaged with $V_{VS}$ = 3.560V and $V_{VS}$ = 3.6V (Note 3) | ● | | | 70 | µA |
| $I_{QFH}$ | Quiescent Supply Current at High Supply While in Forward Regulation | $V_{V1}$ = 36V, $V_{V2}$ = 36V. Measure Combined Current at V1, V2 and $V_S$ Pins Averaged with $V_{VS}$ = 35.960V and $V_{VS}$ = 36V (Note 3) | ● | | | 130 | µA |
| $I_{QRL}$ | Quiescent Supply Current at Low Supply While in Reverse Turn-Off | $V_{V1}$ = 3.6V, $V_{V2}$ = 3.6V. Measure Combined Current at V1, V2 and $V_S$ Pins with $V_{VS}$ = 3.7V | ● | | | 70 | µA |
| $I_{QRH}$ | Quiescent Supply Current at High Supply While in Reverse Turn-Off | $V_{V1}$ = 35.9V, $V_{V2}$ = 35.9V. Measure Combined Current at V1, V2 and $V_S$ Pins with $V_{VS}$ = 36V | ● | | | 130 | µA |
| $I_{QCL}$ | Quiescent Supply Current at Low Supply with E1 and $\overline{E2}$ Active | $V_{V1}$ = 3.6V, $V_{V2}$ = 3.6V, $V_{V1}$ – $V_{VS}$ = 0.9V, $V_{E1}$ = 0V, $V_{\overline{E2}}$ = 2V, V1 and V2 Measured Separately | ● | | | 30 | µA |
| $I_{QCH}$ | Quiescent Supply Current at High Supply with E1 and $\overline{E2}$ Active | $V_{V1}$ = 36V, $V_{V2}$ = 36V, $V_{V1}$ – $V_{VS}$ = 0.9V, $V_{E1}$ = 0V, $V_{\overline{E2}}$ = 2V, V1 and V2 Measured Separately | ● | | | 65 | µA |
| $I_{LEAK}$ | V1, V2 and $V_S$ Pin Leakage Currents When Other Pin Supplies Power (Note 4) | $V_{V1}$ = $V_{V2}$ = 28V, $V_{VS}$ = 0V. Measure $I_{VS}$ | | –10 | –1 | 1 | µA |
| | | $V_{V1}$ = $V_{V2}$ = 14V, $V_{VS}$ = –14V. Measure $I_{VS}$ | | –10 | –1 | 1 | µA |
| | | $V_{V1}$ = $V_{V2}$ = 36V, $V_{VS}$ = 8V. Measure $I_{VS}$ | | –10 | –1 | 1 | µA |
| **PowerPath Controller** | | | | | | | |
| $V_{FR}$ | PowerPath Switch Forward Regulation Voltage | $V_{V1}$, $V_{V2}$ – $V_{VS}$, 3.6V ≤ $V_{V1}$, $V_{V2}$ ≤ 36V, $C_{G1}$ = $C_{G2}$ = 3nF | ● | 10 | | 40 | mV |
| $V_{RTO}$ | PowerPath Switch Reverse Turn-Off Threshold Voltage | $V_{V1}$, $V_{V2}$ – $V_{VS}$, 3.6V ≤ $V_{V1}$, $V_{V2}$ ≤ 36V, $C_{G1}$ = $C_{G2}$ = 3nF | ● | –40 | | –10 | mV |
| $V_{FO}$ | PowerPath Switch Forward Fast-On Voltage Comparator Threshold | $V_{V1}$, $V_{V2}$ – $V_{VS}$, 6V ≤ $V_{V1}$, $V_{V2}$ ≤ 36V, $C_{G1}$ = $C_{G2}$ = 3nF, $I_{G1}$, $I_{G2}$ > 500µA | ● | 50 | | 125 | mV |

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**2**

# ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. V1 = V2 = 12V, E1 = 2V, $\overline{E2}$ = GND, GND = 0V. Current into a pin is positive and current out of a pin is negative. All voltages are referenced to GND, unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **G1, G2 Controller** | | | | | | | |
| $I_{G(SRC)}$ $I_{G(SNK)}$ $I_{G(FO)}$ $I_{G(OFF)}$ | GATE Active Forward Regulation  Source Current  Sink Current  Sink Current During Fast-On  Source Current During Fast-Off | (Note 5)  (Note 6)  (Note 7)  (Note 12) | | −9 15 500 | | −2 200  −500 | µA µA µA µA |
| $V_{G(ON)}$ | G1 and G2 Clamp Voltage | Apply $I_{G1}$ = $I_{G2}$ = 2µA, $V_{V1}$ = $V_{V2}$ = 12V, $V_{VS}$ = 11.8V, Measure $V_{V1} - V_{G1}$ or $V_{V2} - V_{G2}$ | ● | 7.4 | 8.25 | 9.1 | V |
| $V_{G(OFF)}$ | G1 and G2 Off Voltage | Apply $I_{G1}$ = $I_{G2}$ = −30µA, $V_{V1}$ = $V_{V2}$ = 12V, $V_{VS}$ = 12.2V, Measure $V_{V1} - V_{G1}$ or $V_{V2} - V_{G2}$ | ● | | 0.350 | 0.920 | V |
| $t_{G(ON)}$ | G1 and G2 Turn-On Time | $V_{GS}$ < −6V, $C_G$ = 17nF (Note 8) | ● | | | 60 | µs |
| $t_{G(OFF)}$ | G1 and G2 Turn-Off Time | $V_{GS}$ > −1.5V, $C_G$ = 17nF (Note 9) | ● | | | 30 | µs |
| $t_{E(OFF)}$ | Enable Comparator Turn-Off Delay | (Note 14) LTC4416-1 Only | ● | | | 6 | µs |
| **H1 and $\overline{H2}$ Open-Drain Drivers** | | | | | | | |
| $I_{H(OFF)}$ | H1 and $\overline{H2}$ Off Current | 3.6V ≤ $V_{V1}$, $V_{V2}$ ≤ 36V (Note 10) | ● | −1 | | 1 | µA |
| $V_{H(ON)}$ | H1 and $\overline{H2}$ On Voltage | 3.6V ≤ $V_{V1}$, $V_{V2}$ ≤ 36V (Note 10) | ● | | | 100 | mV |
| $t_{H(ON)}$ | H1 and $\overline{H2}$ Turn-On Time | (Note 11) | | | | 5 | µs |
| $t_{H(OFF)}$ | H1 and $\overline{H2}$ Turn-Off Time | (Note 11) | | | | 10 | µs |
| **E1 and $\overline{E2}$ Enable Input Comparators** | | | | | | | |
| $V_{REF}$ | E1 and $\overline{E2}$ Input Threshold Voltage | 3.6V ≤ $V_{V1}$, $V_{V2}$ ≤ 36V, −40°C to 85°C  4V ≤ $V_{V1}$, $V_{V2}$ ≤ 36V, −40°C to 125°C | | 1.180 1.180 | 1.215 1.215 | 1.240 1.240 | V V |
| $I_E$ | E1 and $\overline{E2}$ Input Leakage Current | 0V ≤ $V_{E1}$, $V_{E2}$ ≤ 1.5V | ● | −100 | | 100 | nA |
| $I_{G(ENOFF)}$ | Source Current When Other Channel Enabled (Note 13)  LTC4416  LTC4416-1 | | | −9 −500 | −3 | | µA µA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC4416E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the −40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4416I is guaranteed and tested over the −40°C to 125°C operating temperature range.

**Note 3:** This results in the same supply current as would be observed with an external P-channel MOSFET connected to the LTC4416 and operating in forward regulation.

**Note 4:** Only 3 of 9 permutations illustrated. This specification is the same when power is provided through $V_S$ or V2. This specification is only valid when V1, V2 and $V_S$ are within 28V of each other.

**Note 5:** V1 and V2 are held at 12V and G1 and G2 are forced to 9V. $V_S$ is set at 12V to measure the source current at either G1 or G2.

**Note 6:** V1 and V2 are held at 12V and G1 and G2 are forced to 9V. $V_S$ is set at 11.96V to measure the sink current at either G1 or G2.

**Note 7:** V1 and V2 are held at 12V and G1 and G2 are forced to 9V. $V_S$ is set at 11.875V to measure the sink current at either G1 or G2.

**Note 8:** V1 and V2 are held at 12V and $V_S$ is stepped from 12.2V to 11.8V to trigger the event. G1 and G2 voltages are initially $V_{G(OFF)}$.

**Note 9:** V1 and V2 are held at 12V and $V_S$ is stepped from 11.8V to 12.2V to trigger the event. G1 and G2 voltages are initially $V_{G(ON)}$.

**Note 10:** H1 and $\overline{H2}$ are forced to 2V. E1 and $\overline{E2}$ are forced to 1.5V to measure the off current of H1 and $\overline{H2}$. H1 and $\overline{H2}$ are forced with 1mA to measure the on voltage of H1 and $\overline{H2}$.
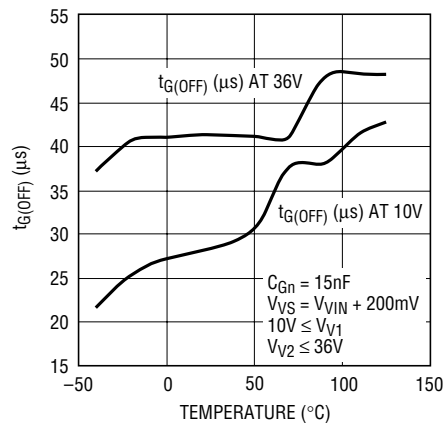
**Note 11:** H1 and H2 are forced to 2V. E1 and $\overline{E2}$ are stepped from 1.3V to 1.1V to measure $t_{S(ON)}$. E1 and E2 are stepped from 1.1V to 1.3V to measure $t_{S(OFF)}$.

**Note 12:** V1 and V2 are held at 12V and G1 and G2 are forced to 9V. $V_S$ is set to 12.05V to measure the source current at either G1 or G2.

**Note 13:** V1 and V2 are held at 12V and G1 and G2 are forced to 9V. $V_S$ is set to 12V to measure the source current at either G1 or G2 when the channel is deselected.

**Note 14:** V1 and V2 are held at 12V, $V_S$ = 11.96V and G1 and G2 have a 4k resistor each to 9V. Measure the delay after the channel is disabled until the gate signal begins to pull high.

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# TYPICAL PERFORMANCE CHARACTERISTICS

**V_FR vs Temperature and Supply Voltage**



4416 G01
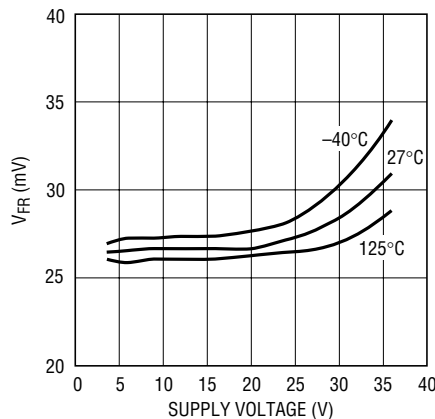
**V_RTO vs Temperature and Supply Voltage**



4416 G02
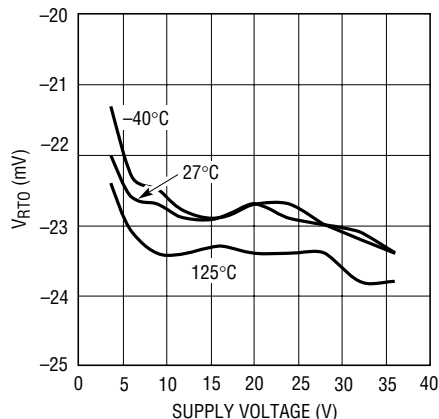
**Normalized Quiescent Supply Current vs Temperature**



4416 G03
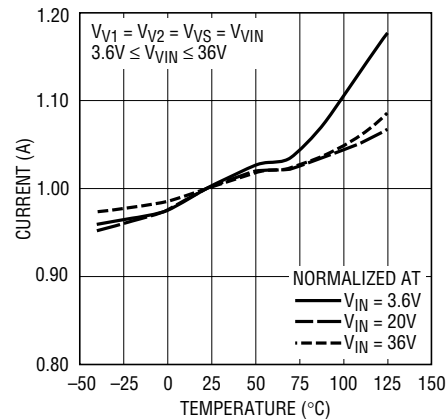
**V1, V2 and V_S Pin Leakage vs Temperature**



4416 G04
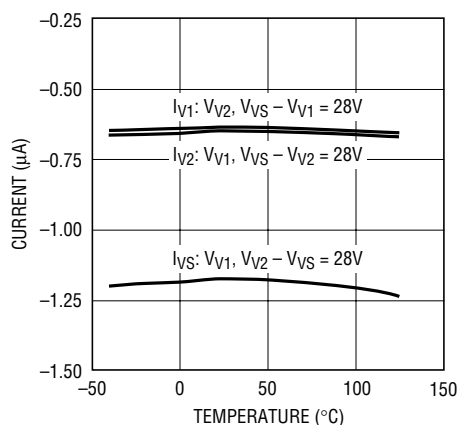
**V_Gn(ON) vs Temperature and V_IN**



4416 G05
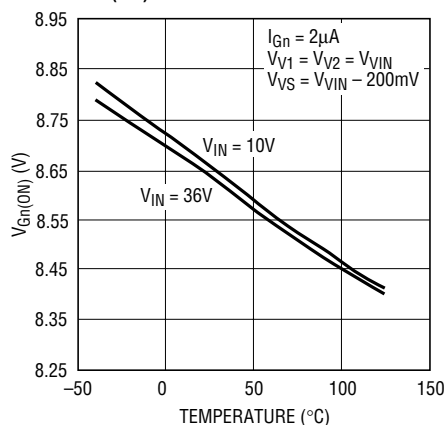
**V_Gn(OFF) vs Temperature and I_Gn**



4416 G06

**t_G(ON) vs Temperature**



4416 G07
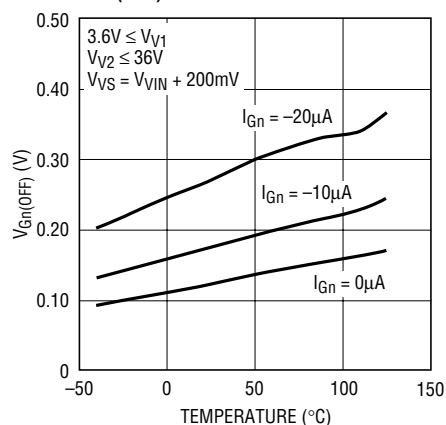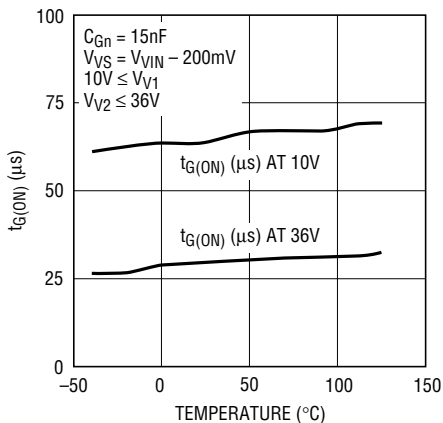
**t_G(OFF) vs Temperature**



4416 G08

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# PIN FUNCTIONS

**H1 (Pin 1):** Open-Drain Comparator Output of the E1 Pin. If E1 > $V_{REF}$, the H1 pin will go high impedance, otherwise the pin will be grounded. The maximum voltage permitted on this pin is 7V. This pin provides support for setting up hysterisis to an external resistor network.

**E1 (Pin 2):** LTC4416 Comparator Enable Input. A high signal greater than $V_{REF}$ will enable the V1 path. The ideal diode action will then determine if the V1 path should turn on by controlling any PFET(s) connected to the G1 pin. If the E1 signal is driven low, the V1 path will perform a "soft-off" provided the PFET(s) are properly configured for blocking DC current. An internal current sink will pull the E1 pin down when the E1 input exceeds 1.5V.

**E1 (Pin 2):** LTC4416-1 Comparator Enable Input. A high signal greater than $V_{REF}$ will enable the V1 path. The ideal diode action will then determine if the V1 path should turn on by controlling any PFET(s) connected to the G1 pin. If the E1 signal is driven low, the V1 path will be quickly disabled by enabling the "fast-off" feature, pulling the G1 gate high. An internal current sink will pull the E1 pin down when the E1 input exceeds 1.5V.

**GND (Pin 3):** Ground. This pin provides a power return path for all the internal circuits.

**$\overline{E2}$ (Pin 4):** LTC4416 Comparator Enable Input. A low signal less than $V_{REF}$ will enable the V2 path. The ideal diode action will then determine if the V2 path should turn on by controlling any PFET(s) connected to the G2 pin. If the $\overline{E2}$ signal is driven high, the V2 path will perform a "soft-off" provided the PFET(s) are properly configured for blocking DC current. An internal current sink will pull the $\overline{E2}$ pin down when the $\overline{E2}$ input exceeds 1.5V.

**$\overline{E2}$ (Pin 4):** LTC4416-1 Comparator Enable Input. A low signal less than $V_{REF}$ will enable the V2 path. The ideal diode action will then determine if the V2 path should turn on by controlling any PFET(s) connected to the G2 pin. If the $\overline{E2}$ signal is driven high, the V2 path will be quickly disabled by enabling the "fast-off" feature, pulling the G2 gate high. An internal current sink will pull the $\overline{E2}$ pin down when the $\overline{E2}$ input exceeds 1.5V.

**H2 (Pin 5):** Open-Drain Comparator Output of the $\overline{E2}$ Pin. If E2 > $V_{REF}$, the H2 pin will go high impedance, otherwise the pin will be grounded. The maximum voltage permitted on this pin is 7V. This pin provides support for setting up hysterisis to an external resistor network.

**G2 (Pin 6):** Second P-Channel MOSFET Power Switch Gate Drive Pin. This pin is directed by the second power controller to maintain a forward regulation voltage ($V_{FR}$) of 25mV between the V2 and $V_S$ pins when V2 is greater than $V_S$. When V2 is less than $V_S$, the G2 pin will pull up to the $V_S$ pin voltage, turning off the second P-channel power switch.
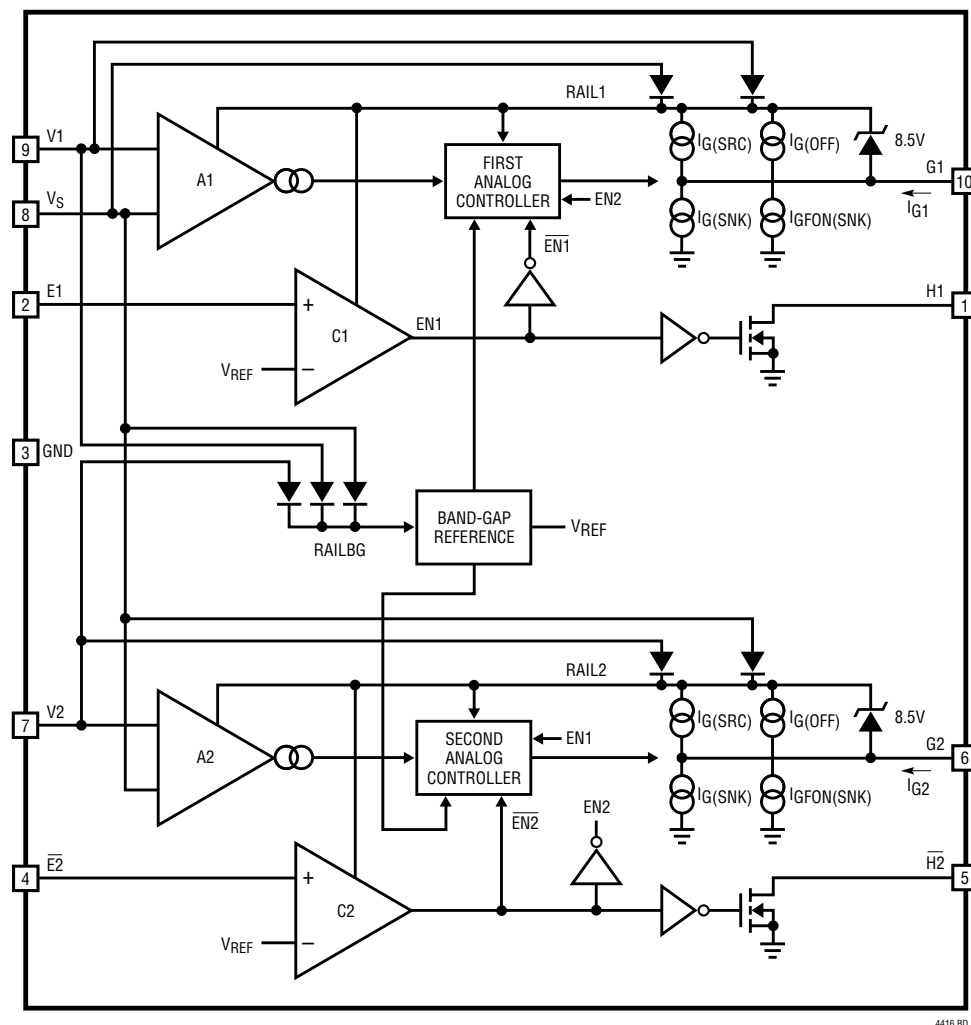
**V2 (Pin 7):** Second Input Supply Voltage. Supplies power to the second power controller and the band-gap reference. V2 is one of the two voltage sense inputs to the second internal power controller (the other input to the second internal power controller is the $V_S$ pin). This input is usually supplied power from the second, or backup, power source. This pin can be bypassed to ground with a capacitor in the range of 0.1µF to 10µF if needed to suppress load transients.

**$V_S$ (Pin 8):** Power Sense Input Pin. Supplies power to the internal circuitry of both the first and second power controller and the band-gap reference. This pin is also a voltage sense input to both internal analog controllers (the other input to the first controller is the V1 pin and the other input to the second controller is the V2 pin.) This input may also be supplied power from an auxiliary source which also supplies current to the load.

**V1 (Pin 9):** First Input Supply Voltage. Supplies power to the first power controller and the band-gap reference. V1 is one of the two voltage sense inputs to the first internal power controller (the other input to the first internal power controller is the $V_S$ pin). This input is usually supplied power from the first, or primary, power source. This pin can be bypassed to ground with a capacitor in the range of 0.1µF to 10µF if needed to suppress load transients.

**G1 (Pin 10):** First P-Channel MOSFET Power Switch Gate Drive Pin. This pin is directed by the first power controller to maintain a forward regulation voltage ($V_{FR}$) of 25mV between the V1 and $V_S$ pins when V1 is greater than $V_S$. When V1 is less than $V_S$, the G1 pin will pull up to the $V_S$ pin voltage, turning off the first P-channel power switch.

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# BLOCK DIAGRAM

V1  9

$V_S$  8

A1

FIRST ANALOG CONTROLLER — EN2

$\overline{EN1}$

RAIL1

$I_{G(SRC)}$  $I_{G(OFF)}$  8.5V  G1  10

$I_{G(SNK)}$  $I_{GFON(SNK)}$  $I_{G1}$

E1  2

+ C1 — EN1

$V_{REF}$  —

H1  1

GND  3

BAND-GAP REFERENCE  $V_{REF}$

RAILBG

V2  7

A2

SECOND ANALOG CONTROLLER — EN1

$\overline{EN2}$  EN2

RAIL2

$I_{G(SRC)}$  $I_{G(OFF)}$  8.5V  G2  6

$I_{G(SNK)}$  $I_{GFON(SNK)}$  $I_{G2}$

$\overline{E2}$  4

+ C2 —

$V_{REF}$  —

$\overline{H2}$  5

4416 BD

# OPERATION

Operation can best be understood by referring to the Block Diagram which illustrates the internal circuit blocks. The LTC4416/LTC4416-1 are divided into three sections, namely:

1. The channel 1 controller consisting of A1, C1, the "first analog contoller," the G1 drivers and the H1 output driver.

2. The band-gap reference

3. The channel 2 controller consisting of A2, C2, the "second analog controller," the G2 drivers and the $\overline{H2}$ output driver.

Each of the three sections has its own derived internal power supply referred to as a rail. RAIL1 provides power to the channel 1 controller. RAIL2 provides power to the channel 2 controller. The internal RAILBG provides power to the band-gap reference. The internal rail1 derives its power from the higher voltage of V1 and $V_S$. The internal rail2 derives its power from the higher voltage of V2 and $V_S$. RAILBG derives its power from the highest voltage of V1, V2, and $V_S$. All three sections share a common ground connected to the GND pin.

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# OPERATION

The band-gap reference provides internal bias currents used by the channel 1 and channel 2 controllers. It also provides a precision voltage reference, $V_{REF}$, used by comparators C1 and C2. The band-gap reference is powered as long as a minimum operational voltage is present on either V1, V2, or $V_S$.

The C1 and C2 comparators provide a fixed comparison between the E1 and $\overline{E2}$ inputs, respectively, and the internal $V_{REF}$ signal. The comparator outputs are directly represented by the H1 and $\overline{H2}$ open-drain outputs. The output states of H1 and $\overline{H2}$ are not dependent upon the relative voltage difference between $V_{V1} - V_{VS}$ and $V_{V2} - V_{VS}$, respectively. If $V_{E1}$ is less than $V_{REF}$, the H1 open-drain output will be low impedance to GND. If $V_{\overline{E2}}$ is less than $V_{REF}$, the $\overline{H2}$ open-drain output will be low impedance to GND.

The A1 and A2 circuits act both as a high side transconductance amplifiers and as comparators. Both A1 and A2 act identically when the analog controllers are fully enabled. The relationship of the G1 current is represented by Figure 1.

When $V_{V1} - V_{VS} < V_{RTO}$, the A1 activates the reverse turn-off condition and the $I_{G1}$ current is $I_{G(OFF)}$. When $V_{RTO} < V_{V1} - V_{VS} < V_{FR}$, the A1 acts as a class A output and the $I_{G1}$ current is fixed at $I_{G(SRC)}$. As the $V_{V1} - V_{VS}$ voltage
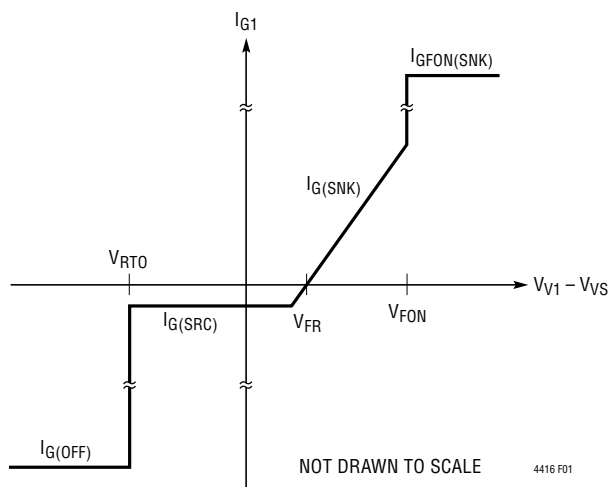
approaches the forward regulation voltage, $V_{FR}$, the $I_{G(SNK)}$ current will be proportional to $V_{V1} - V_{VS}$. When $V_{V1} - V_{VS} > V_{FON}$, the A1 activates the fast-on condition, $t_{G(ON)}$, and the $I_{G1}$ current is set to $I_{GFON(SNK)}$.

### LTC4416 OPERATION

The interaction of the LTC4416 analog controllers distinguish the operation of the LTC4416 from a simple circuit using two PowerPath controllers. Table 1 explains the different operation modes of the analog controllers.

**Table 1. LTC4416 Operational Modes**

| E1 | $\overline{E2}$ | Operation Mode | $I_{G(OFF)1}$ | $I_{G(OFF)2}$ |
|---|---|---|---|---|
| 1 | 0 | Load Sharing | Enabled | Enabled |
| 1 | Sense | V1 is Less Than V2 | Enabled | |
| Sense | 0 | V1 is Greater Than V2 | | Enabled |
| 0 | X | Channel 1 Disabled. Do Not Use | Disabled | |
| X | 1 | Channel 2 Disabled. Do Not Use | | Disabled |
| 0 | 1 | Both Channels Disabled | Disabled | Disabled |

The LTC4416 has six modes of operation. Each mode of operation is dependent upon the configuration of the E1 and $\overline{E2}$ input pins.

### Load Sharing Operation

The load sharing mode configures the LTC4416 into two independent PowerPath controllers. This is accomplished by fully enabling both the first analog controller and the second analog controller. Both channels will implement the gate drive outlined in Figure 1.

### V1 is Less Than V2 Operation

Channel 1 is fully enabled. If $V_{V1} - V_{VS} < V_{RTO}$, channel 1 will implement all of the $I_{G1}$ currents listed in Figure 1.

When $V_{\overline{E2}}$ is above the $V_{REF}$ threshold, channel 2 is in a "soft-off mode". This means that G2 will only provide an $I_{G(SRC)}$ current instead of either an $I_{G(SRC)}$ or an $I_{G(OFF)}$ current.

When $V_{\overline{E2}}$ is below the $V_{REF}$ threshold, channel 2 is fully enabled, and G2 will become active implementing the $I_G$ output current listed in Figure 1.



**Figure 1. $I_{G1}$ vs $V_{V1} - V_{VS}$**

# OPERATION

**V1 is Greater Than V2 Operation**

When $V_{E1}$ is below the $V_{REF}$ threshold, channel 1 is in a "soft-off mode". This means that G1 will only provide an $I_{G(SRC)}$ current instead of an $I_{G(SNK)}$ or an $I_{GFON(SNK)}$ current.

When $V_{E1}$ is above the $V_{REF}$ threshold, channel 1 is immediately fully enabled, and G1 will become active implementing the output current listed in Figure 1.

Channel 2 is fully enabled. If $V_{V1} - V_{VS} < V_{RTO}$, channel 2 will implement all of the $I_{G2}$ currents listed in Figure 1.

**Channel 1 is Disabled**

The LTC4416 is not designed to have channel 1 disabled by grounding E1 and leaving $\overline{E2}$ in an indeterminate state. If this happens, the channel 2 PowerPath controller will not have reverse turn-off capability. No electrical harm to the LTC4416 will occur.

**Channel 2 is Disabled**

The LTC4416 is not designed to have channel 2 disabled by connecting $\overline{E2}$ high and leaving E1 in an indeterminate state. If this happens, the channel 1 PowerPath controller will not have reverse turn-off capability. No electrical harm to the LTC4416 will occur.

**Both Channels Disabled**

When both channels of the LTC4416 are disabled, both G1 and G2 currents are set to $I_{G(SRC)}$.

**LTC4416-1 OPERATION**

The LTC4416-1 is designed for overvoltage/undervoltage protection or when either voltage path must be turned off rapidly, regardless of the status of the other voltage input. The LTC4416-1 does not implement the soft-off feature implemented in the LTC4416. The E1 and $\overline{E2}$ inactive will force the $I_G$ current of their respective channel to $I_{G(OFF)}$. Table 2 explains the operation of the E1 and $\overline{E2}$ inputs. The term "active" implies that $I_{G(OFF)}$ current is forced on the Gn pins regardless of the $V_{Vn} - V_{VS}$ value. The term "enabled" implies that $I_{G(OFF)}$ current is provide on the Gn pins if and only if $V_{Vn} - V_{VS} < V_{RTO}$.

**Table.2 LTC4416-1 Operational Modes**

| E1 | $\overline{E2}$ | Operation Mode | $I_{G(OFF)1}$ | $I_{G(OFF)2}$ |
|---|---|---|---|---|
| 0 | X | Undervoltage Protection | Active | |
| X | 1 | Overvoltage Protection | | Active |
| 1 | X | Channel 1 PowerPath | Enabled | |
| X | 0 | Channel 2 PowerPath | | Enabled |

# APPLICATIONS INFORMATION

**LTC4416**

The LTC4416 is designed to support three major applications. The first two applications assume that V1 is the primary power source and V2 is the backup power source. The first application is where the V1 power supply is normally less than V2. The second application is where the V1 power supply is normally greater than V2. The third application addresses the load sharing case where both V1 and V2 are relatively equal in value.

**V1 is Less Than V2**

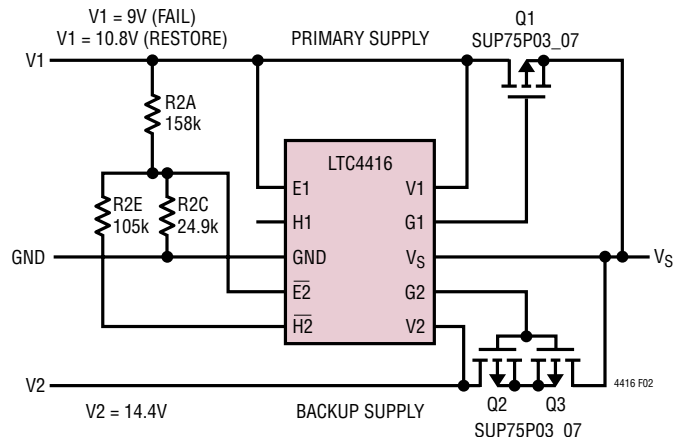Figure 2 illustrates the external resistor configuration for this case.



**Figure 2**

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# APPLICATIONS INFORMATION

This configuration would be used where V1 is a 12V power supply and the V2 power supply is a 4-cell Li-Ion battery pack. When V1 is 12V, $\overline{E2}$ disables the V2 source from being connected to $V_S$ through Q2A and Q2B by forcing G2 to V2, $\overline{H2}$ is open circuit. E1 is connected to a voltage greater than the $V_{REF}$ to keep the V1 to $V_S$ path active. The $V_S$ output can be shut completely off by grounding the E1 input. The LTC4416 takes its power from the higher of V1, V2 and $V_S$. This configuration will provide power from V1 to $V_S$ until the V1 supply drops below 9V.

When V1 drops below 9V, the $\overline{H2}$ pin closes to GND, G2 drops to a $V_{CLAMP}$ below V2 and G1 rises to the $V_S$ voltage level. V2 will supply current to $V_S$ until V1 rises above 10.8V. The H1 output will be open until the E1 input drops below the $V_{REF}$ voltage level.

The V1 $V_{FAIL}$ is determined by:

$$V_{FAIL} = V_{ETH} \bullet \frac{R2A+R2C}{R2C}$$

$$= 1.222V \bullet \frac{158k+24.9k}{24.9k} = 8.98V$$

The V1 $V_{RESTORE}$ is determined by:

$$V_{RESTORE} = V_{ETH} \bullet \frac{\left(R2A+\left(R2C\|R2E\right)\right)}{R2C\|R2E}$$

$$= 1.222V \bullet \frac{158k+\left(24.9k\|105k\right)}{24.9k\|105k} = 10.81V$$

**V1 is Greater Than V2**

Figure 3 illustrates the external resistor configuration for this case.

This configuration would be used where V1 is a 12V power supply and the V2 power supply is a 3-cell Li-Ion battery pack. When V1 is 16V, E1 enables the V1 source as being the primary supply, thus disabling the V2 supply since V1 > V2. When E1 > $V_{REF}$, the H1 output is open. The $V_S$ output can be shut completely off by grounding the H1 input and forcing $\overline{E2}$ > $V_{REF}$. The LTC4416 takes its power from the higher of V1, V2 and $V_S$. This configuration will provide power from V1 to $V_S$ until the V1 supply drops below 12V.
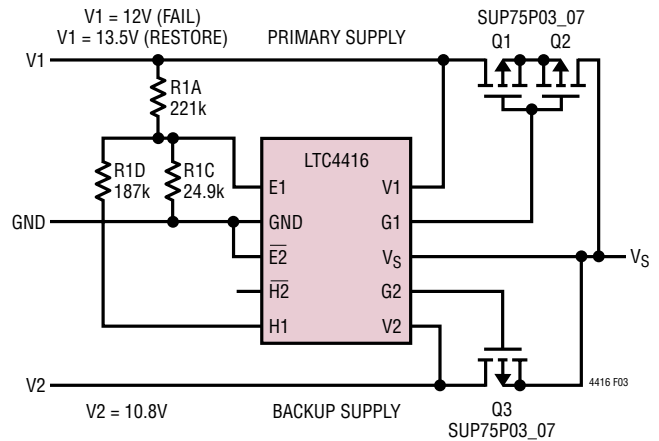


**Figure 3**

When V1 drops below 12V, the H1 pin closes to GND, G2 drops to a $V_{CLAMP}$ below V2 and G1 rises to the V1 voltage level. V2 will supply current to $V_S$ until V1 rises above 13.5V. The $\overline{H2}$ output will be shorted to GND until the $\overline{E2}$ input goes above the $V_{REF}$ voltage level.

The V1 $V_{FAIL}$ is determined by:

$$V_{FAIL} = V_{ETH} \bullet \frac{R1A+R1C}{R1C}$$

$$= 1.222V \bullet \frac{221k+24.9k}{24.9k} = 12.07V$$

The V1 $V_{RESTORE}$ is determined by:

$$V_{RESTORE} = V_{ETH} \bullet \frac{\left(R1A+\left(R1C\|R1D\right)\right)}{R1C\|R1D}$$

$$= 1.222V \bullet \frac{221k+\left(24.9k\|187k\right)}{24.9k\|187k} = 13.51V$$

**Load Sharing**

Figure 4 illustrates the configuration for this case.

This configuration would be used where V1 and V2 are relatively the same voltage. In this case the LTC4416 acts as two interconnected ideal diode controllers. $V_S$ will be supplied by the higher of the two supplies, V1 and V2. If V1 and V2 are exactly the same, then 50% of the current for $V_S$ will be supplied by each supply. As the two supplies

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# APPLICATIONS INFORMATION

differ by more than 100mV, 100% of the load will come from the higher of V1 or V2.

The user has the option of using E1 and $\overline{E2}$ to disable one of the two supplies by connecting them to a digital controller. If E1 is brought low, V1 will no longer supply current to $V_S$. If E2 is brought high, V2 will no longer supply current to $V_S$. If E1 is brought low and $\overline{E2}$ is brought high, $V_S$ will be disabled.

Figure 5 shows the same application without the shutdown option. It has one-half the losses of Figure 4 and is configured for 5V rails.
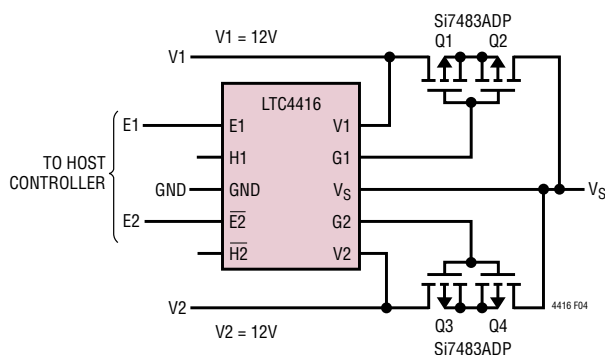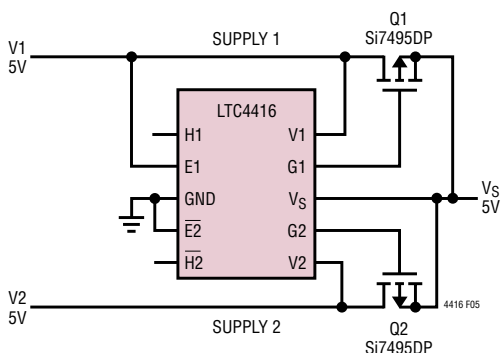


**Figure 4**



**Figure 5. Dual PowerPath for Current Sharing**

## LTC4416-1

The LTC4416-1 will support all three of the LTC4416 applications without the "soft-off" feature. The only difference in the two designs is the LTC4416-1 will rapidly switch off the load from a supply whenever a channel is disabled. This rapid turn-off feature is desirable when the supply cannot tolerate certain voltage excursions under load, or when the load is being protected from a rapidly changing input supply.

## Under and Overvoltage Shutdown

Refer to Figure 6 for an application circuit which disables the power to the load when the input voltage gets too low or too high. When $V_{IN}$ starts from zero volts, the load to the output is disabled until $V_{IN}$ reaches 5.5V. The V1 path is enabled and the load remains on the input until the supply exceeds 13.5V. At that voltage, the V2 path is disabled. As the input falls, the voltage source will be reconnected to the load when the input drops to 12V and the V2 path is enabled. Finally, the load will be removed from the input supply when the voltage drops below 5V.
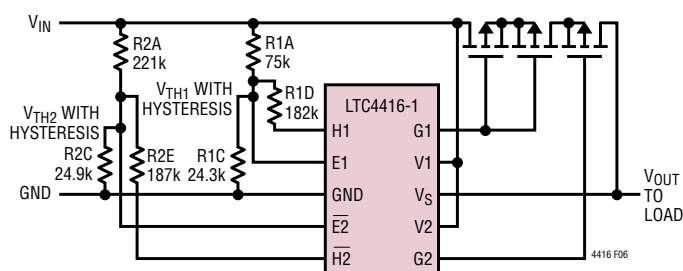


UV ENABLED AT 5V, $V_{IN}$ RESTORED TO LOAD WHEN $V_{IN}$ RISES TO 5.5V
OV ENABLED AT 13.5V, $V_{IN}$ RESTORED TO LOAD WHEN $V_{IN}$ FALLS TO 12V

**Figure 6**

### Undervoltage

$$V_{FAIL} = V_{ETH} \cdot \frac{R1A + R1C}{R1C}$$

$$= 1.222V \cdot \frac{75k + 24.3k}{24.3k} = 4.99V$$

$$V_{RESTORE} = V_{ETH} \cdot \frac{\left(R1A + \left(R1C\|R1D\right)\right)}{R1C\|R1D}$$

$$= 1.222V \cdot \frac{75k + \left(24.3k\|182k\right)}{24.3k\|182k} = 5.497V$$

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# APPLICATIONS INFORMATION

**Overvoltage**

$$V_{FAIL} = V_{ETH} \cdot \frac{R2A + R2C\|R2E}{R2C\|R2E}$$

$$= 1.222V \cdot \frac{221k + 24.9k\|187k}{24.9k\|187k} = 13.51V$$

$$V_{RESTORE} = V_{ETH} \cdot \frac{R2A + R2C}{R2C}$$

$$= 1.222V \cdot \frac{221k + 24.9k}{24.9k} = 12.07V$$

The over and undervoltage lockout circuits are shown here working in tandem. It is possible to configure the circuit for either over or undervoltage lockout by using only one of the voltage paths and eliminating the components from the other. Refer to Figure 7 for an LTC4416-1 configured for overvotlage protection. If the input does not go below ground, transistor Q1 can be eliminated.

The LTC4416-1 should be used in this configuration rather than the LTC4416 because the LTC4416-1 will turn-off rapidly if an over or undervoltage condition is detected. Refer to Figure 8 for a comparison of the transient response of the two ICs using the circuit configuration of Figure 6. The LTC4416 will not turn-off quickly in an overvoltage or undervoltage condition because the "fast-off" feature is not enabled. This will cause the output to travel beyond the desired range.
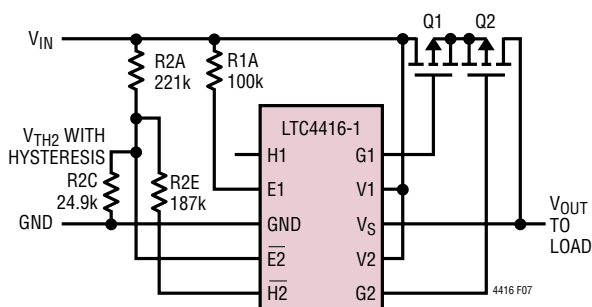
Figure 9 contains a rapidly changing input voltage on a much smaller time scale in comparison to Figure 8. The LTC4416 will require the $t_{E(OFF)}$ time prior to the rapid pull-up current being applied. The gate voltage will be pulled high with $I_{G(OFF)}$ which has a minimum current of 500μA. The discharge time of the gate will be dependent on the capacitance of the external FET and the initial gate-source voltage of the circuit. The total time delay will equal:

$$t_{DELAY} = t_{E(OFF)} + t_{DISCHARGE}$$

$$= t_{E(OFF)} + \frac{C_{GS} \cdot \Delta V}{I_{G(OFF)}}$$
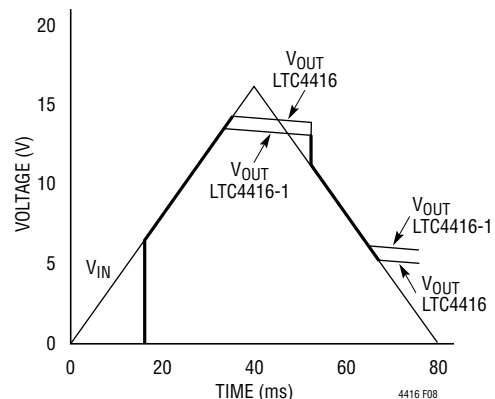


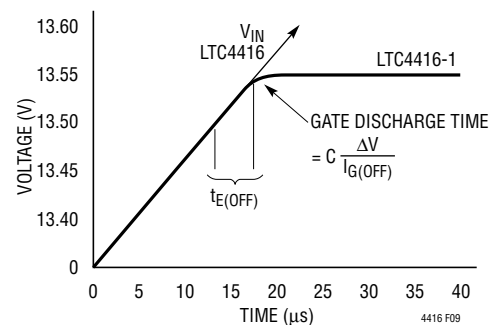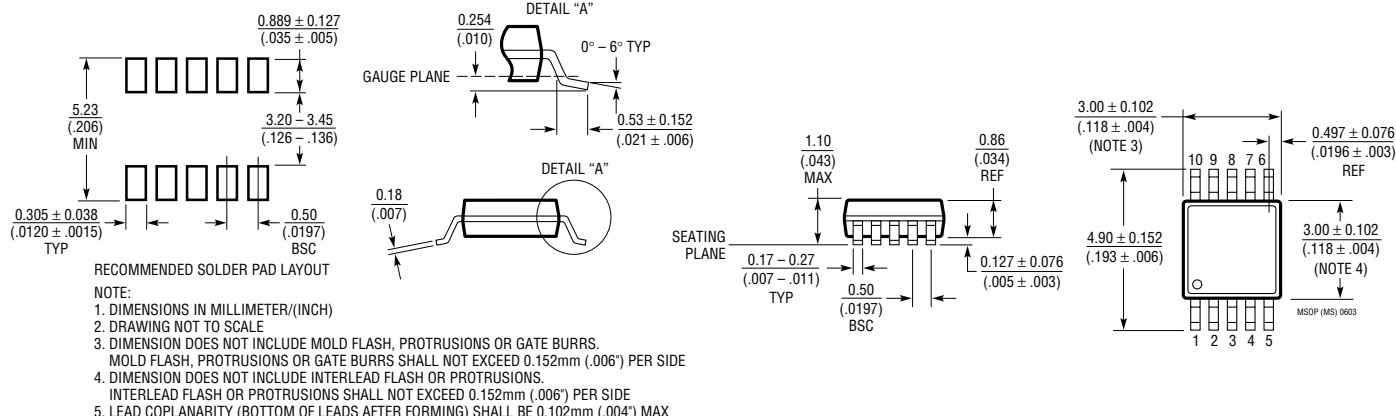**Figure 8. Transient Response of the LTC4416 vs the LTC4416-1 Light Load with a Large Capacitor on V$_{OUT}$**



**Figure 7. LTC4416-1 Configured for Overvoltage Protection**



**Figure 9. Close Up of the Transient Response of the LTC4416-1 to a Rapidly Rising Input**

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# LTC4416/LTC4416-1

# PACKAGE DESCRIPTION

**MS Package**
**10-Lead Plastic MSOP**
(Reference LTC DWG # 05-08-1661)

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

# RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1473 | Dual PowerPath Switch Driver | Switches and Isolates Sources Up to 30V |
| LTC1479 | PowerPath Controller for Dual Battery Systems | Complete PowerPath Management for Two Batteries; DC Power Source, Charger and Backup |
| LTC1558/LTC1559 | Back-Up Battery Controller with Programmable Output | Adjustable Backup Voltage from 1.2V NiCd Button Cell, Includes Boost Converter |
| LT®1579 | 300mA Dual Input Smart Battery Back-Up Regulator | Maintains Output Regulation with Dual Inputs, 0.4V Dropout at 300mA |
| LTC1733/LTC1734 | Monolithic Linear Li-Ion Chargers | Thermal Regulation, No External MOSFET/Sense Resistor |
| LTC1998 | 2.5µA, 1% Accurate Programmable Battery Detector | Adjustable Trip Voltage/Hysteresis, ThinSOT™ |
| LTC4055 | USB Power Controller and Li-Ion Linear Charger | Automatic Battery Switchover, Thermal Regulation, Accepts Wall Adapter and USB Power, 4mm × 4mm QFN |
| LTC4066 | USB Power Controller and Battery Charger | Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 50mΩ Ideal Diode, 4mm × 4mm QFN24 Package |
| LTC4085 | USB Power Manager with Ideal Diode Controller and Li-Ion Charger | Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode <50mΩ Option, 4mm × 3mm DFN14 Package |
| LTC4354 | Negative Voltage Diode-OR Controller and Monitor | Replaces Power Schottky Diodes; 80V Operation |
| LTC4410 | USB Power Manager in ThinSOT | Enables Simultaneous Battery Charging and Operation of USB Component Peripheral Devices |
| LTC4411 | SOT-23 Ideal Diode | 2.6A Forward Current, 28mV Regulated Forward Voltage |
| LTC4412HV | 36V, Low Loss PowerPath Controller in MSOP | –40°C to –125°C Operation; Automatic Switching Between DC Sources |
| LTC4413 | Dual 2.6A, 2.5V to 5.5V Ideal Diodes in 3mm × 3mm DFN | 100mΩ ON Resistance, 1µA Reverse Leakage Current, 28mV Regulated Forward Voltage |
| LTC4414 | 36V, Low Loss PowerPath Controller for Large PFETs | Drives Large $Q_G$ PFETs, Very Low Loss Replacement for Power Supply O'Ring Diodes, 3.5V to 36V AC/DC Adapter Voltage Range, MSOP-8 Package |

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