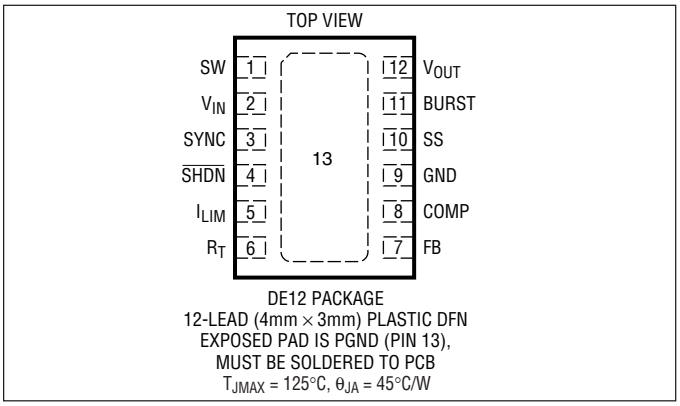
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, SS, SYNC Voltages ..... –0.3 to 7V
BURST, ~~SHDN~~, V_{OUT} Voltages ..... –0.3 to 8V
Operating Temperature Range
(Notes 2, 3) .....–40°C to 85°C
Storage Temperature Range .....–65°C to 125°C
SW Voltage
DC ..... –0.3V to 8V
Pulsed <100ns ..... –0.3V to 10V

PIN CONFIGURATION



DE12 PACKAGE
12-LEAD (4mm × 3mm) PLASTIC DFN
EXPOSED PAD IS PGND (PIN 13),
MUST BE SOLDERED TO PCB
T_{JMAX} = 125°C, θ_{JA} = 45°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3458EDE#PBF	LTC3458EDE#TRPBF	3458	12-Lead (4mm x 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V, V_{OUT} = 5V, R_T = 200k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum V_{IN} Operating Voltage	T_A = 0°C to 85°C T_A = –40°C to 0°C			1.4 1.4	1.5 1.7	V V
Output Voltage Adjust Range		●	2.0		7.5	V
Feedback Voltage	0°C to 85°C, V_{OUT} = 3.3V –40°C to 0°C		1.21 1.20	1.23	1.25 1.25	V V
Undervoltage (Exit Burst Mode Operation)	Below Feedback Voltage			–4%		V
Feedback Input Current	V_{FB} = 1.23V			1	50	nA
Quiescent Current - Burst Mode Operation	V_{IN} Current at 3.3V V_{OUT} Current at 5V			15 5	30 10	µA µA
Quiescent Current - Shutdown	V_{IN} Current at 3.3V V_{OUT} Current at 0V			0.5 1	1 3	µA µA
Quiescent Current - Active	V_{IN} Current Switching			1	3	mA
NMOS Switch Leakage		●		0.05	5	µA
PMOS Switch Leakage		●		0.05	5	µA
NMOS Switch On Resistance	V_{OUT} = 5V			0.3		Ω
PMOS Switch On Resistance	V_{OUT} = 5V			0.4		Ω
Fixed NMOS Current Limit	R_{ILIM} = 124k	●	1.4	1.6		A
Maximum Duty Cycle	V_{IN} = 3.3V, f_{OSC} = 1MHz	●	80	90		%
Minimum Duty Cycle		●			0	%
Frequency Accuracy	R_T = 200k	●	0.85	1	1.15	MHz
Error Amplifier Transconductance				100		µA/V
Error Amplifier Source Current				7		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.3V, V_{OUT} = 5V, R_T = 200k, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifier Sink Current				7		µA
SYNC Input High		●	1.5			V
SYNC Input Low		●			0.35	V
$\overline{SHDN}$ Input High		●	1.25			V
$\overline{SHDN}$ Input Low		●			0.3	V
BURST Mode Peak Current	R_{ILIM} = 124k			0.4		A
BURST Threshold Voltage				1.10		V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

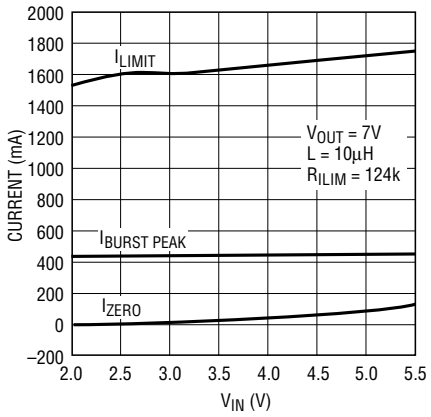
Note 2: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: The LTC3458 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

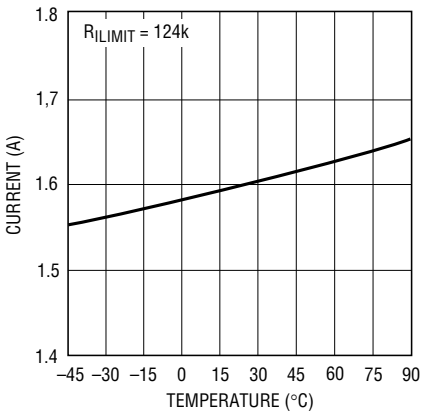
TYPICAL PERFORMANCE CHARACTERISTICS

(T_A = 25°C unless otherwise specified)

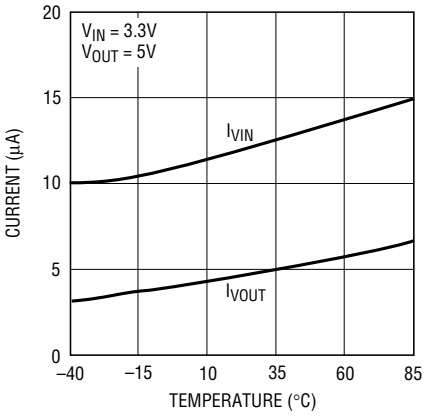
I_{LIMIT}, I_{BURST}, T_{ZERO} Currents



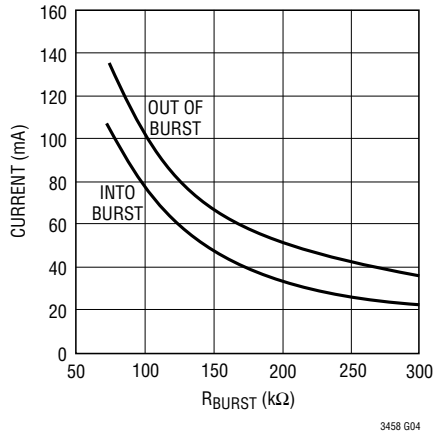
Current Limit Accuracy



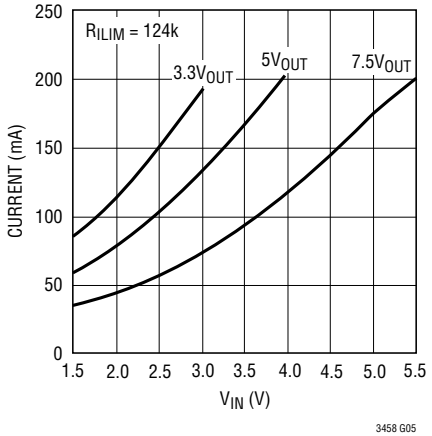
Burst Mode Quiescent Current



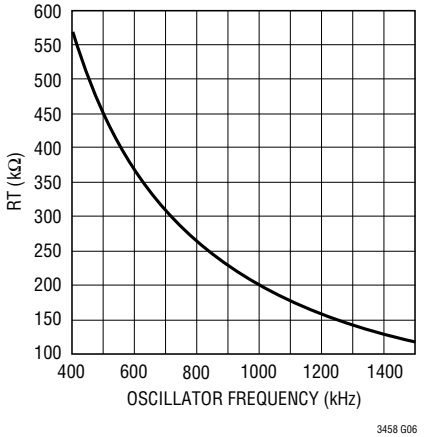
Typical Burst Mode Threshold and Hysteresis vs R_{BURST}



Maximum Load Current in Burst

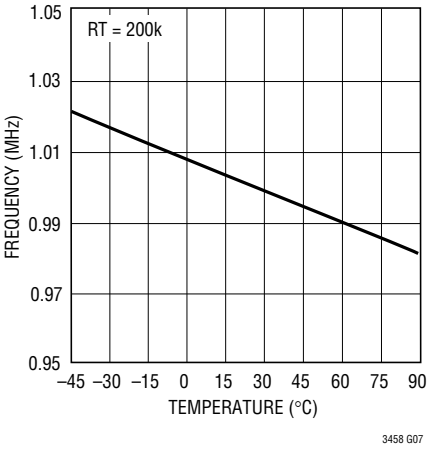


Oscillator Programming Resistor

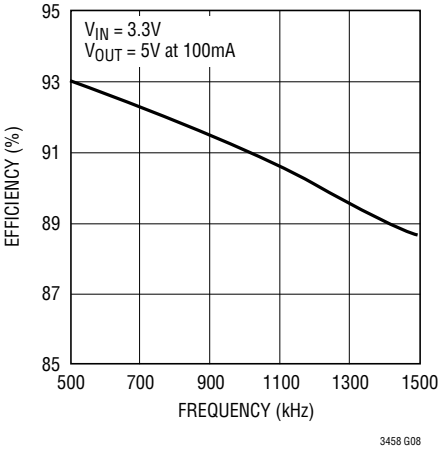


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

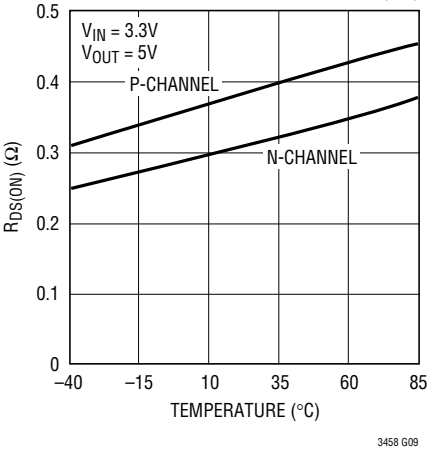
Frequency Accuracy



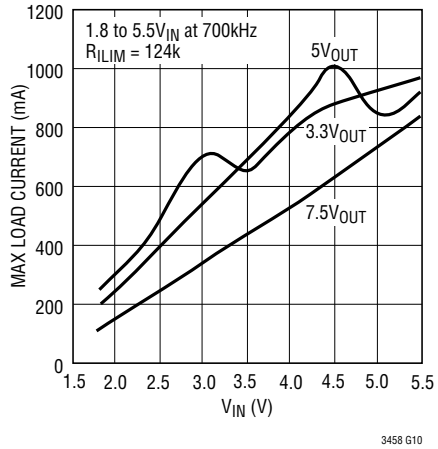
Efficiency vs Frequency



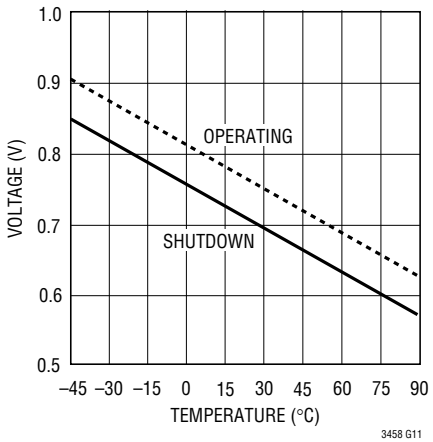
N-Channel and P-Channel $R_{DS(ON)}$



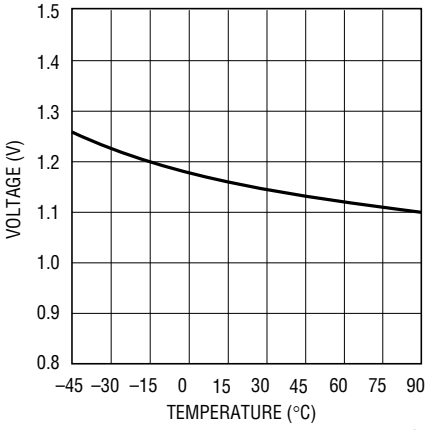
Maximum Load Current



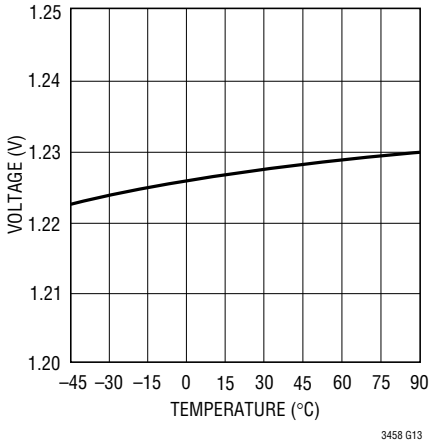
SHDN Pin Threshold and Hysteresis



SYNC Pin Threshold

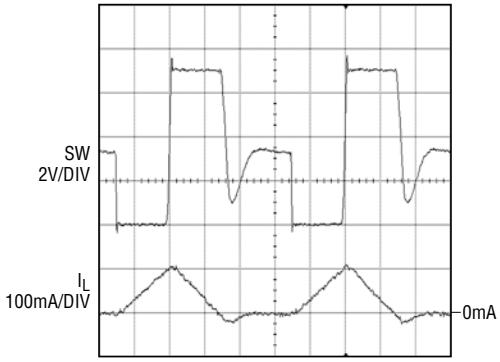


FB Voltage



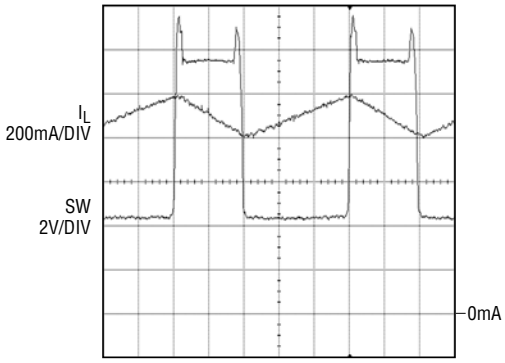
TYPICAL PERFORMANCE CHARACTERISTICS

Fixed Frequency (FF) Discontinuous Current



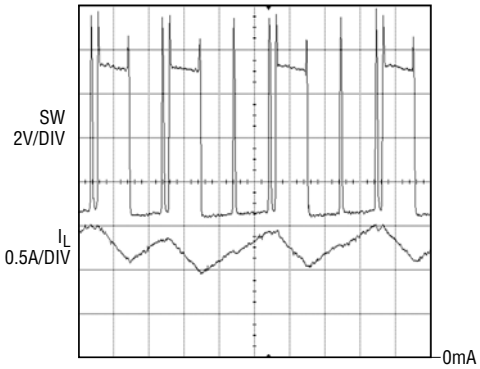
V_{IN} = 3.3V
V_{OUT} = 7V
L = 10µH
200ns/DIV

Fixed Frequency (FF) Continuous Current



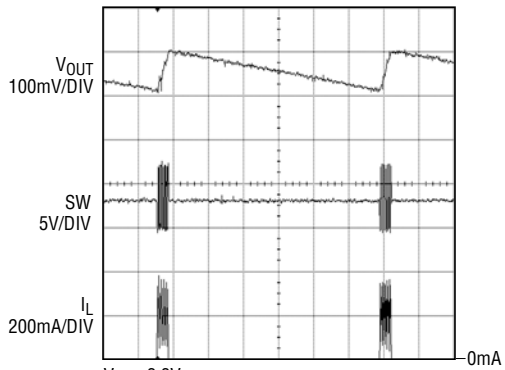
V_{IN} = 3.3V
V_{OUT} = 7V
L = 10µH
200ns/DIV

Over-Current with 1.5A I_{LIMIT}



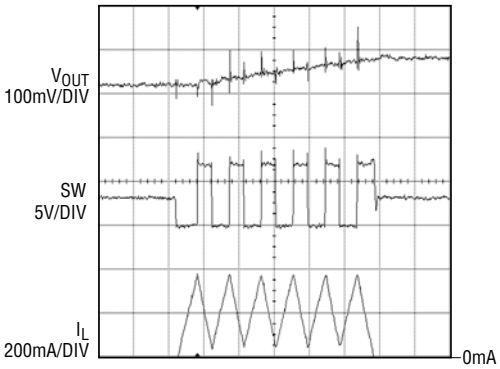
V_{IN} = 3.3V
V_{OUT} = 7V
L = 10µH
R_{ILIM} = 133k
1µs/DIV

Burst Mode Operation



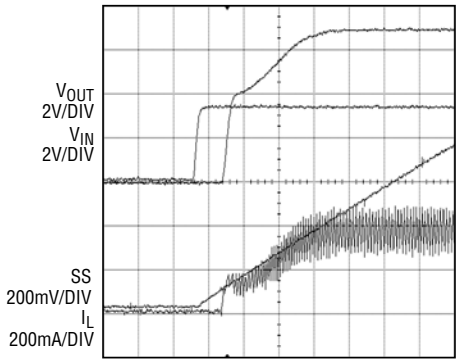
V_{IN} = 3.3V
V_{OUT} = 7V
L = 10µH
C_{OUT} = 22µF
C_{FF} = 22pF
50µs/DIV

Burst Mode Operation Close-Up



V_{IN} = 3.3V
V_{OUT} = 7V
L = 10µH
C_{OUT} = 22µF
C_{FF} = 22pF
2µs/DIV

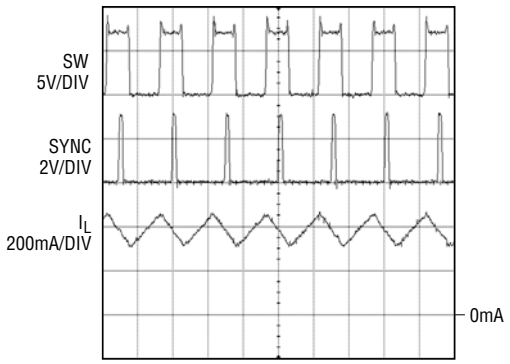
Soft-Start into 50Ω Load



V_{IN} = 3.3V
V_{OUT} = 7V
L = 10µH
5ms/DIV

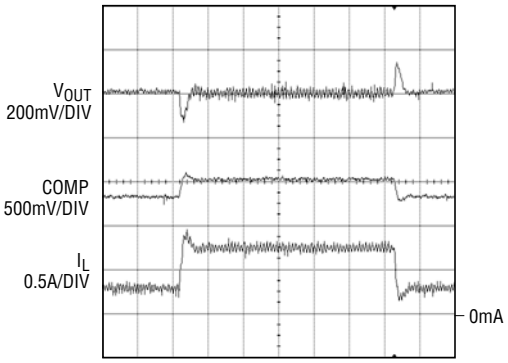
TYPICAL PERFORMANCE CHARACTERISTICS

Sync Operation at 1.33MHz



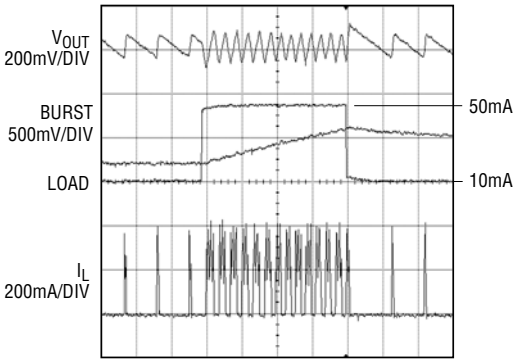
V_{IN} = 3.3V
V_{OUT} = 7V
R_{OSC} = 200k
500ns/DIV

FF Mode 100-300mA Load Step



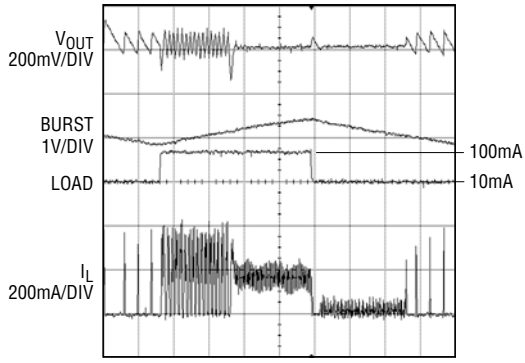
V_{IN} = 3.3V
V_{OUT} = 5V
R_Z = 33K
CC1 = 270pF
CC2 = 10pF
C_{OUT} = 22µF
200µs/DIV
L = 10µH
F = 1MHz

Burst Mode Operation 10mA to 50mA Load Step



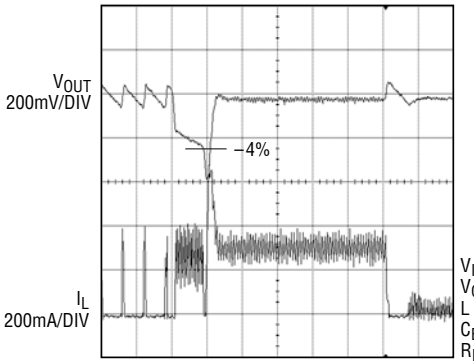
V_{IN} = 3.3V
V_{OUT} = 5V
L = 10µH
C_{OUT} = 22µF
200µs/DIV

Auto Mode 10mA to 100mA Load Step



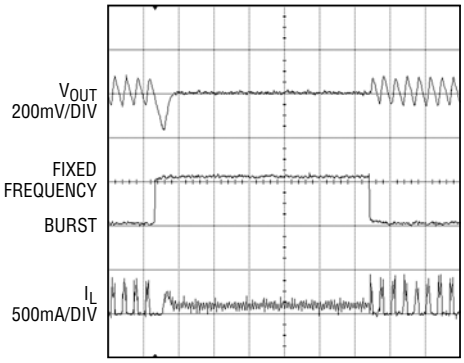
V_{IN} = 3.3V
V_{OUT} = 5V
L = 10µH
C_{BURST} = 0.015µF
R_{BURST} = 133k
500µs/DIV

10mA to 200mA Load Step Showing UV Trip



V_{IN} = 3.3V
V_{OUT} = 5V
L = 10µH
C_{BURST} = 0.015µF
R_{BURST} = 133k
200µs/DIV

Forced BURST to FF Mode Switch with 50mA Load



V_{IN} = 3.3V
V_{OUT} = 5V
L = 10µH
R_Z = 33k
CC1 = 270pF
CC2 = 10pF
C_{OUT} = 22µF
200µs/DIV

PIN FUNCTIONS

SW (Pin 1): Switch Pin for Inductor Connection. During discontinuous conduction mode an antiring resistor connects SW to V_{IN} to reduce noise.

V_{IN} (Pin 2): Input Supply Pin. Connect this to the input supply and decouple with 1µF minimum.

SYNC (Pin 3): Oscillator Synchronization Pin. A clock pulse width of 100ns to 2µs is required to synchronize the internal oscillator. This pin is disabled when grounded.

$\overline{SHDN}$ (Pin 4): Shutdown Pin. Grounding this pin shuts down the IC. Connect to >1.25V to enable.

I_{LIM} (Pin 5): Adjustable Peak Current Limit. Connect a resistor from I_{LIM} to GND to program the peak inductor current according to the following formula:

$$I_{LIMIT} = \frac{200}{R_{ILIM}}$$

where I_{LIMIT} is in amps and R_{ILIM} is in kΩ.

R_T (Pin 6): Connect a resistor to ground to program the oscillator frequency, according to the formula:

$$f_{OSC} = \frac{1}{0.2 + 0.004 \bullet R_T}$$

where f_{OSC} is in MHz and R_T is in kΩ.

FB (Pin 7): Connect Resistor Divider Tap Here. The output voltage can be adjusted from 2V to 7.5V. Feedback reference voltage is typically 1.23V.

COMP (Pin 8): g_m Error Amp Output. A frequency compensation network is connected from this pin to ground to compensate the loop. See the section "Compensating the Feedback Loop" for guidelines.

GND (Pin 9): Signal Ground Pin.

SS (Pin 10): Connect a capacitor between this pin and ground to set soft-start period. 5µA of current is sourced from SS during soft-start.

$$t(msec) = C_{SS}\ (\mu F) \bullet 200$$

BURST (Pin 11): Burst Mode Threshold Adjust Pin. A resistor/capacitor combination from this pin to ground programs the average load current at which automatic Burst Mode operation is entered, according to the formula:

$$R_{BURST} = \frac{10}{I_{BURST}}$$

where R_{BURST} is in kΩ and I_{BURST} is in amps.

$$C_{BURST} = \frac{C_{OUT} \bullet V_{OUT}}{10{,}000}$$

where $C_{BURST(MIN)}$ and C_{OUT} are in µF.

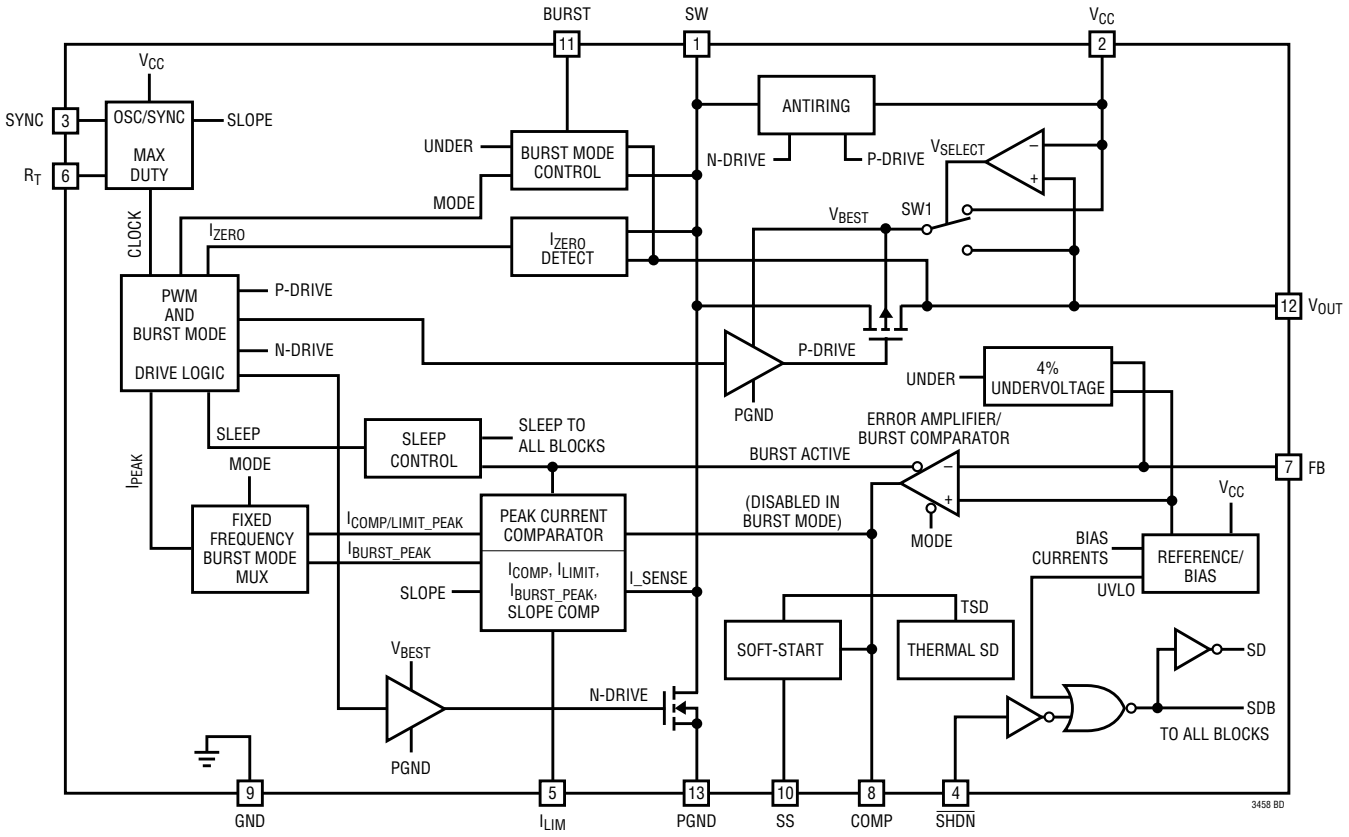
To force fixed frequency PWM mode, connect BURST to V_{OUT} through a 50k resistor.

V_{OUT} (Pin 12): Output of the Synchronous Rectifier and Internal Gate Drive Source for the Power Switches.

$$V_{OUT} = 1.23\left(1 + \frac{R2}{R1}\right)$$

Exposed Pad (PGND) (Pin 13): Must be soldered to PCB ground, for electrical contact and optimum thermal performance.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Detailed Description

The LTC3458 provides high efficiency, low noise power for boost applications with output voltages up to 7.5V. The true output disconnect feature eliminates inrush current, and allows V_{OUT} to go to zero during shutdown. The current mode architecture with adaptive slope compensation provides ease of loop compensation with excellent transient load response. The low $R_{DS(ON)}$, low gate charge synchronous switches eliminate the need for an external Schottky rectifier, and provide efficient high frequency pulse width modulation (PWM) control. High efficiency is achieved at light loads when Burst Mode operation is entered, where the IC's quiescent current is a low 15µA typical on V_{IN}. The LTC3458 is designed to provide custom performance in a variety of applications with programmable feedback, current limit, oscillator frequency, soft-start, and Burst Mode threshold.

LTC3458 Programmable Functions

Current Limit/Peak Burst Current. The programmable current limit circuit sets the maximum peak current in the internal N-channel MOSFET switch. This clamp level is programmed using a resistor to ground on I_{LIM}. In Burst Mode operation, the current limit is automatically set to ~1/4 of the programmed current limit for optimal efficiency. A 124k R_{ILIM} resistor is recommended in most applications unless a lower limit is needed to prevent the external inductor from saturating.

$$I_{LIM} = \frac{200}{R}$$

I is in amps and R is in kΩ.

$$I_{BURSTPEAK} \approx \frac{1}{4} \bullet I_{LIM}$$

APPLICATIONS INFORMATION

Error Amp. The error amplifier is a transconductance type, with its positive input internally connected to the 1.23V reference, and its negative input connected to FB. A simple compensation network is placed from COMP to ground. Internal clamps limit the minimum and maximum error amp output voltage for improved large signal transient response. During sleep (in Burst Mode), the compensation pin is high impedance, however clamps limit the voltage on the external compensation network, preventing the compensation capacitor from discharging to zero during the sleep time.

Oscillator. The frequency of operation is set through a resistor from R_T to ground. An internally trimmed timing capacitor resides inside the IC. The oscillator frequency is calculated using the following formula:

$$f_{OSC} = \frac{1}{0.2 + 0.004 \bullet R_T}$$

where f_{OSC} is in MHz and R_T is in kΩ

The oscillator can be synchronized with an external clock applied to the SYNC pin. When synchronizing the oscillator, the free running frequency must be set to approximately 30% lower than the desired synchronized frequency.

Soft-Start. The soft-start time is programmed with an external capacitor to ground on SS. An internal current source charges it with a nominal 5µA. The voltage on the SS pin (in conjunction with the external resistor on I_{LIM}) is used to control the peak current limit until the voltage on the capacitor exceeds ~1V, at which point the external resistor sets the peak current. In the event of a commanded shutdown, severe short-circuit, or a thermal shutdown, the capacitor is discharged automatically.

$$t_{(msec)} = C_{SS}\ (\mu F) \bullet 200$$

Other LTC3458 Features and Functions

Antiringing Control. The antiringing control places a resistor across the inductor to damp the ringing on SW pin discontinuous conduction mode. The LC ringing (L = inductor, C_{SW} = Capacitance on SW pin) is low energy, but can cause EMI radiation.

Current Sensing. Lossless current sensing converts the peak current signal to a voltage to sum in with the internal slope compensation. This summed signal is compared to the error amplifier output to provide a peak current control command for the PWM. The slope compensation in the IC is adaptive to the input and output voltage, therefore the converter provides the proper amount of slope compensation to ensure stability, but not an excess to cause a loss of phase margin in the converter.

Output Disconnect and Inrush Limiting. The LTC3458 is designed to allow true output disconnect by eliminating body diode conduction of the internal P-channel MOSFET rectifier. This allows V_{OUT} to go to zero volts during shutdown, drawing no current from the input source. It also allows for inrush current limiting at turn-on, minimizing surge currents seen by the input supply. Note that to obtain the advantages of output disconnect, there must be no external Schottky diodes connected between SW and V_{OUT}.

Shutdown. The part is shut down by pulling $\overline{SHDN}$ below 0.3V, and made active by pulling the pin above 1.25V. Note that $\overline{SHDN}$ can be driven above V_{IN} or V_{OUT}, as long as it is limited to less than 8V.

Synchronous Rectifier. To prevent the inductor current from running away, the P-channel MOSFET synchronous rectifier is only enabled when $V_{OUT} > (V_{IN} + 0.25V)$.

Thermal Shutdown. If the die temperature reaches approximately 150°C, the part will go into thermal shutdown and all switches will be turned off and the soft-start capacitor will be reset. The part will be enabled again when the die temperature has dropped by 10°C (nominal).

Zero Current Amplifier. The zero current amplifier monitors the inductor current to the output and shuts off the synchronous rectifier once the current is below 50mA typical, preventing negative inductor current.

Burst Mode Operation

Burst Mode operation can be automatic or user controlled. In automatic operation, the IC will automatically enter Burst Mode operation at light load and return to fixed frequency PWM mode for heavier loads. The user can program the average load current at which the mode

APPLICATIONS INFORMATION

transition occurs using a single resistor. During Burst Mode operation, the oscillator is shut down, since the on time is determined by the time it takes the inductor current to reach a fixed peak current, and the off time is determined by the time it takes for the inductor current to return to zero.

In Burst Mode operation, the IC delivers energy to the output until it is regulated and then goes into a sleep mode where the outputs are off and the IC is consuming only 15µA of quiescent current. In this mode the output ripple voltage has a variable frequency component with load current and will be typically 2% peak-to-peak. This maximizes efficiency at very light loads by minimizing switching and quiescent losses. Burst Mode ripple can be reduced slightly by using more output capacitance (22µF or greater). This capacitor does not need to be a low ESR type if low ESR ceramics are also used. Another method of reducing Burst Mode ripple is to place a small feedforward capacitor across the upper resistor in the V_{OUT} feedback divider network.

During Burst Mode operation, COMP is disconnected from the error amplifier in an effort to hold the voltage on the external compensation network where it was before entering Burst Mode operation. To minimize the effects of leakage current and stray resistance, voltage clamps limit the minimum and maximum voltage on COMP during Burst Mode operation. This minimizes the transient experienced when a heavy load is suddenly applied to the converter after being in Burst Mode operation for an extended period of time.

For automatic operation, an RC network should be connected from BURST to ground. The value of the resistor will control the average load current (I_{BURST}) at which Burst Mode operation will be entered and exited (there is hysteresis to prevent oscillation between modes). The equation given for the capacitor on BURST is for the minimum value, to prevent ripple on the BURST pin from causing the part to oscillate in and out of Burst Mode operation at the current where the mode transition occurs.

$$R_{BURST} = \frac{10}{I_{BURST}}$$

where R_{BURST} is in kΩ and I_{BURST} is in amps.

$$C_{BURST} = \frac{C_{OUT} \bullet V_{OUT}}{10{,}000}$$

where $C_{BURST(MIN)}$ and C_{OUT} are in µF.

Note: the BURST pin only sources current based on current delivered to V_{OUT} through the P-channel MOSFET. If current in the inductor is allowed to go negative (this can occur at very light loads and high step-up ratios), the burst threshold may become inaccurate, preventing the IC from entering Burst Mode operation. For R_{BURST} values greater than 200k, a larger than recommended inductor value may be needed to ensure positive inductor current and automatic Burst Mode operation.

In the event that a sudden load transient causes the voltage level on FB to drop by more than 4% from the regulation value, an internal pull-up is applied to BURST, forcing the part quickly out of Burst Mode operation. For optimum transient response when going between Burst Mode operation and PWM mode, Burst can be controlled manually by the host. This way PWM mode can be commanded before the load step occurs, minimizing output voltage drop. Note that Burst Mode operation is inhibited during start-up and soft-start.

Manual Control

For applications requiring fixed frequency operation at all load currents, connect the BURST pin to V_{OUT} through a 50kΩ resistor. To force Burst Mode operation, ground the BURST pin.

For applications where a large load step can be anticipated, the circuit below can be used to reduce the voltage transient on V_{OUT}. Automatic operation is achieved when the external PMOS is off and fixed frequency operation is commanded when the external PMOS is on. In shutdown, the PMOS should be off.

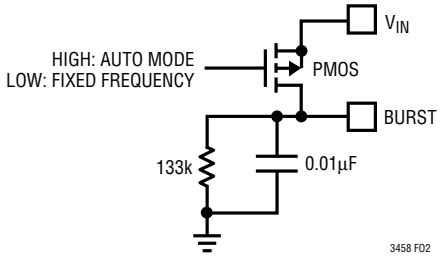


Figure 1

APPLICATIONS INFORMATION

COMPONENT SELECTION

Inductor Selection

The high frequency operation of the LTC3458 allows for the use of small surface mount inductors. Since the internal slope compensation circuit relies on the inductor's current slope and frequency, Table 1 should be used to select an inductor value for a given frequency of operation (±25%). The recommended value will yield optimal transient performance while maintaining stable operation. Inductor values larger than listed in Table 1 are permissible to reduce the current ripple.

Table 1. Recommended Inductor Values

Frequency	Inductor Value(μH)
1.5MHz	3.3 to 4.7
1.25MHz	4.7 to 6.8
1MHz	6.8 to 10
750Hz	10 to 15
500kHz	15 to 22

For high efficiency, choose an inductor with high frequency core material, such as ferrite, to reduce core losses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. Molded chokes or chip inductors usually do not have enough core to support peak inductor currents in the 1A to 3A region. To minimize radiated noise, use a toroidal or shielded inductor. (Note that the inductance of shielded types will drop more as current increases, and will saturate more easily). See Table 2 for a list of inductor manufacturers.

Table 2. Inductor Vendor Information

Supplier	Phone	Website
Coilcraft	(847) 639-6400	www.coilcraft.com
TDK	(847) 803-6100	www.component.tdk.com
Murata	USA: (814) 237-1431 (800) 831-9172	www.murata.com
Sumida	USA: (847) 956-0666 Japan: 81-3-3607-5111	www.japanlink.com/sumida
COEV	(800) 227-7040	www.coev.net
Toko	(847) 297-0070	www.tokoam.com
Würth	(202) 785-8800	www.we-online.com

Some example inductor part types are:

Coilcraft: DO1608 and MSS5131 Series
TDK: RLF5018T and SLF7045 Series
Murata: LQH4C and LQN6C Series
Sumida: CDRH4D28 and CDRH6D28 Series
COEV: DQ7545 Series
TOKO: D62CB and D63LCB Series
WÜRTH: WE-PD2 Series

Output Capacitor Selection

The output voltage ripple has three components to it. The bulk value of the capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The max ripple due to charge is given by:

$$V_{RBULK} = \frac{I_P \bullet V_{IN}}{C_{OUT} \bullet V_{OUT} \bullet f}$$

where I_P = peak inductor current and f = switching frequency.

The ESR (equivalent series resistance) is usually the most dominant factor for ripple in most power converters. The ripple due to capacitor ESR is given by:

$$V_{RCESR} = I_P \bullet C_{ESR}$$

where C_{ESR} = Capacitor Series Resistance.

The ESL (equivalent series inductance) is also an important factor for high frequency converters. Using small, surface mount ceramic capacitors, placed as close as possible to the V_{OUT} pins, will minimize ESL.

Low ESR/ESL capacitors should be used to minimize output voltage ripple. For surface mount applications, AVX TPS Series tantalum capacitors, Sanyo POSCAP, or Taiyo Yuden X5R type ceramic capacitors are recommended. For through-hole applications, Sanyo OS-CON capacitors offer low ESR in a small package size.

In all applications, a minimum of 4.7μF (generally 22μF is recommended), low ESR ceramic capacitor should be placed as close to the V_{OUT} pin as possible, and grounded to a local ground plane.

APPLICATIONS INFORMATION

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the input source and reduces input switching noise. In most applications >1µF per amp of peak input current is recommended. See Table 3 for a list of capacitor manufacturers for input and output capacitor selection.

Table 3. Capacitor Vendor Information

Supplier	Phone	Website
AVX	(803) 448 - 9411	www.avxcorp.com
Sanyo	(619) 661 - 6322	www.sanyovideo.com
TDK	(847) 803 - 6100	www.component.tdk.com
Murata	USA: (814) 237-1431 (800) 831-9172	www.murata.com
Taiyo Yuden	(408) 573 - 4150	www.t-yuden.com

Operating Frequency Selection

There are several considerations in selecting the operating frequency of the converter. The first is staying clear of sensitive frequency bands, which cannot tolerate any spectral noise. For example in products incorporating RF communications the 455kHz IF frequency is sensitive to any noise, therefore switching above 600kHz is desired. Some communications have sensitivity to 1.1MHz and in that case a 1.5MHz switching converter frequency may be employed. The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter capacitors go down in value and size. The trade off is in efficiency, since the switching losses due to gate charge increase proportional with frequency.

Thermal Considerations

For the LTC3458 to deliver its full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the large thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible. If the junction temperature rises above ~150°C, the part will go into thermal shutdown, and all switching will stop until the temperature drops.

Compensating the Feedback Loop

The LTC3458 uses current mode control, with internal adaptive slope compensation. Current mode control eliminates the 2nd order filter due to the inductor and output capacitor exhibited in voltage mode controllers, and simplifies the power loop to a single pole filter response. The product of the modulator control to output DC gain, and the error amp open-loop gain gives the DC gain of the system:

$$G_{DC} = G_{CONTROL} \bullet G_{EA} \bullet \frac{V_{REF}}{V_{OUT}} \bullet G_{CURRENT\_SENSE}$$

$$G_{CONTROL} = \frac{2 \bullet V_{IN}}{I_{OUT}},$$

$$G_{EA} \approx 1{,}000 \qquad G_{CURRENT\_SENSE} = \frac{1}{R_{DS(ON)}}$$

The output filter pole is given by:

$$f_{FILTER\_POLE} = \frac{I_{OUT}}{\pi \bullet V_{OUT} \bullet C_{OUT}},$$

where C_{OUT} is the output filter capacitor.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2\pi \bullet R_{ESR} \bullet C_{OUT}},$$

where R_{ESR} is the output capacitor equivalent series resistance.

A troublesome feature of the boost regulator topology is the right half plane zero (RHP), and is given by:

$$f_{RHPZ} = \frac{V_{IN}^{2}}{2\pi \bullet I_{OUT} \bullet V_{OUT} \bullet L}$$

At heavy loads this gain increase with phase lag can occur at a relatively low frequency. The loop gain is typically

APPLICATIONS INFORMATION

rolled off before the RHP zero frequency.

The typical error amp compensation is shown in Figure 2. The equations for the loop dynamics are as follows:

$$f_{POLE1} \approx \frac{1}{2\pi \bullet 10e^6 \bullet CC1} \text{ which is close to DC}$$

$$f_{ZERO1} = \frac{1}{2\pi \bullet R_Z \bullet CC1}$$

$$f_{POLE2} \approx \frac{1}{2\pi \bullet R_Z \bullet CC2}$$

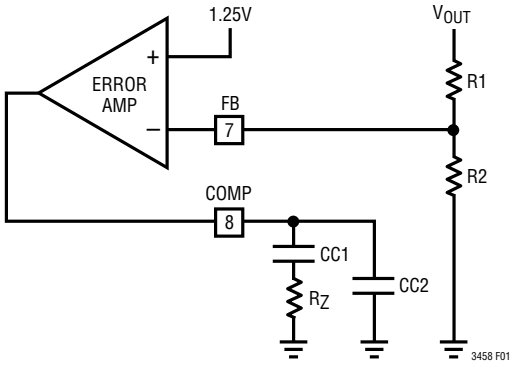
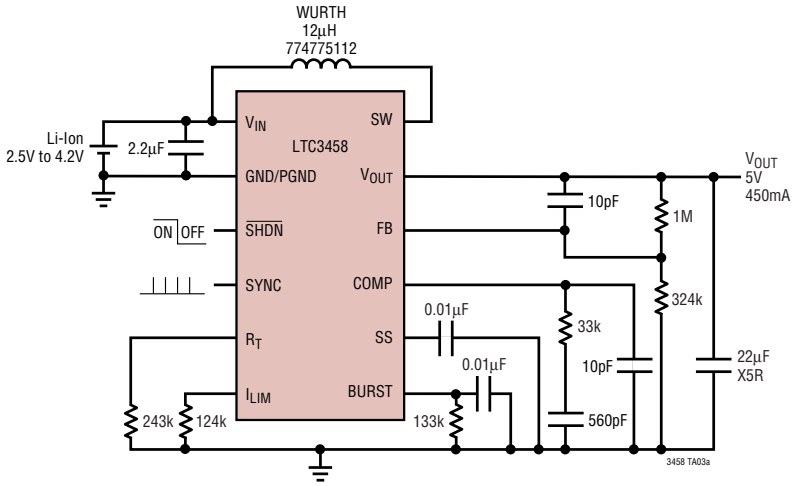


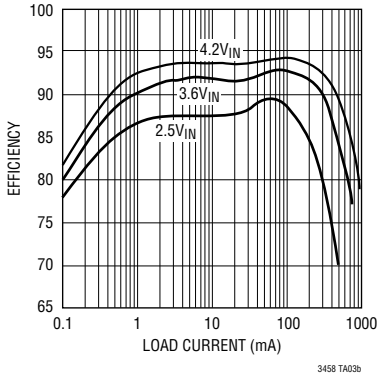
Figure 2

TYPICAL APPLICATIONS

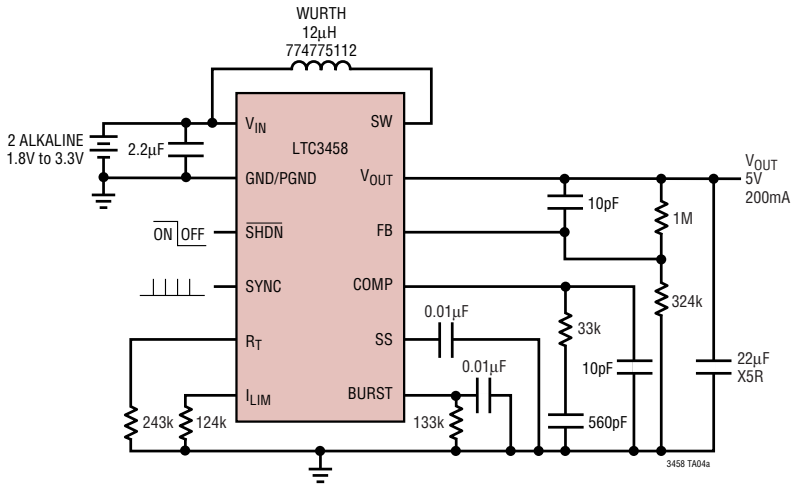
Lithium-Ion to 5V, 500mA at 850kHz



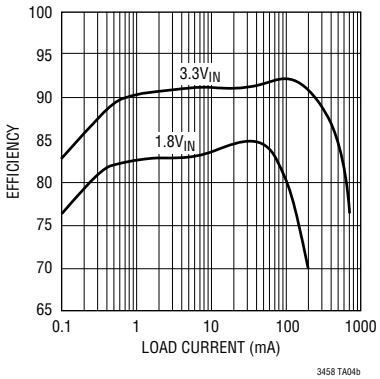
Li-Ion to $5V_{OUT}$



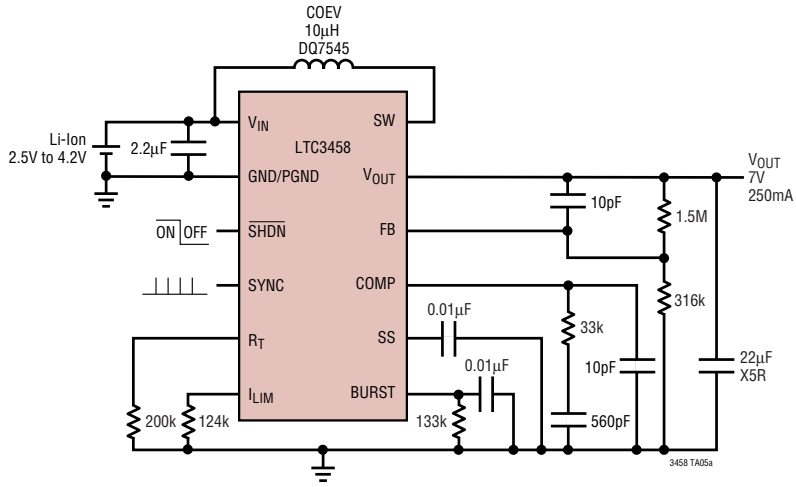
Two Cell to $5V_{OUT}$, 200mA at 850kHz



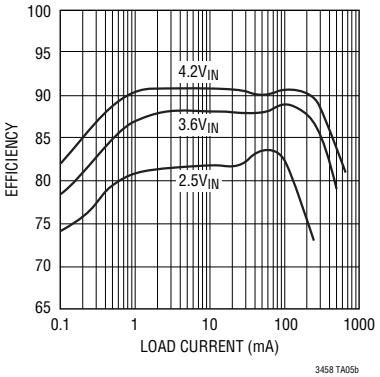
Two Alkaline to $5V_{OUT}$



Lithium-Ion Battery to $7V_{OUT}$, 250mA at 1MHz

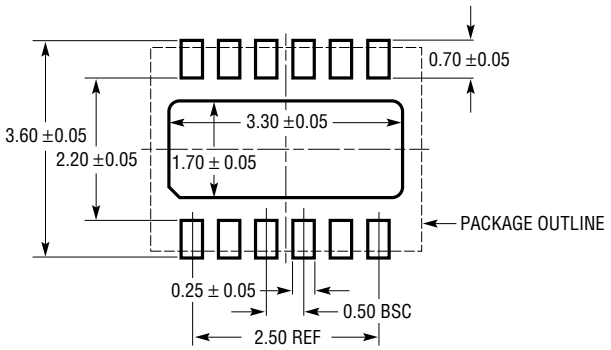


Li-Ion to $7V_{OUT}$

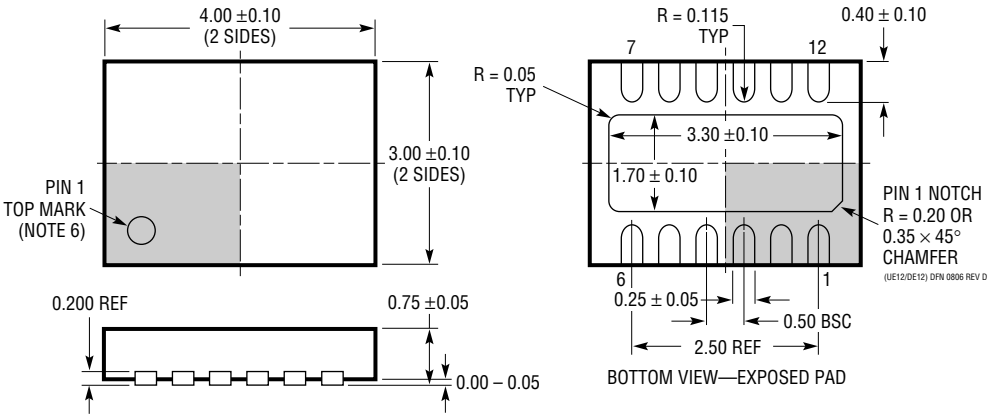


PACKAGE DESCRIPTION

DE/UE Package
12-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1695)



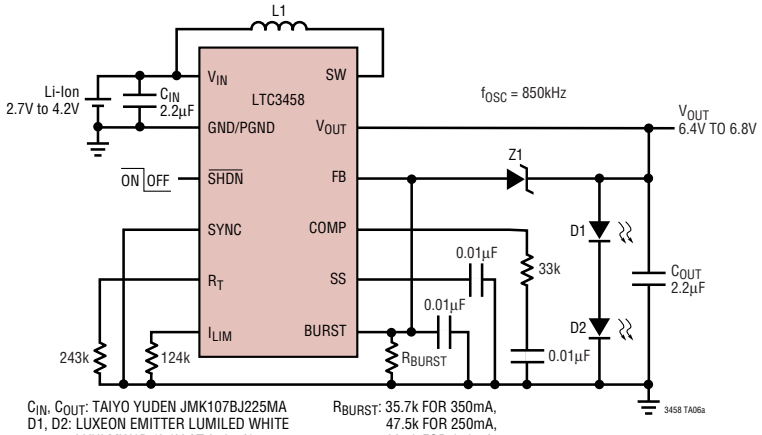
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



NOTE:
1. DRAWING PROPOSED TO BE A VARIATION OF VERSION
   (WGED) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

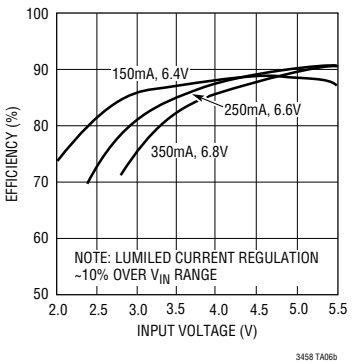
Dual Lumiled Application with BURST Pin Current Regulation



CIN, COUT: TAIYO YUDEN JMK107BJ225MA
D1, D2: LUXEON EMITTER LUMILED WHITE LXHLMW1D (2.9V AT 350mA)
L1: Wurth 12µH 774775112

RBURST: 35.7k FOR 350mA,
47.5k FOR 250mA,
82.5k FOR 150mA
Z1: CENTRAL SEMI 6.8V ZENER DIODE SOT-23 CMPZ5235B

2-Lumileds in Series



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1310	1.5A I_{SW}, 4.5MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.75V to 18V, $V_{OUT(MAX)}$ = 35V, I_Q = 12mA, I_{SD} < 1µA, MS10E
LT1613	550mA I_{SW}, 1.4MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 0.9V to 10V, $V_{OUT(MAX)}$ = 34V, I_Q = 3mA, I_{SD} < 1µA, ThinSOT
LT1615/ LT1615-1	300mA/80mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$ = 34V, I_Q = 20µA, I_{SD} < 1µA, ThinSOT
LT1618	1.5A I_{SW}, 1.4MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.6V to 18V, $V_{OUT(MAX)}$ = 35V, I_Q = 1.8mA, I_{SD} < 1µA, MS10
LT1944 (Dual)	Dual Output 350mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$ = 34V, I_Q = 20µA, I_{SD} < 1µA, MS10
LT1945 (Dual)	Dual Output Pos/Neg 350mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$ = ±34V, I_Q = 20µA, I_{SD} < 1µA, MS10
LT1946/LT1946A	1.5A I_{SW}, 1.2MHz/2.7MHZ, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.45V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 3.2mA, I_{SD} < 1µA, MS8
LT1949/ LT1949-1	550mA I_{SW}, 600kHz/1.1MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.5V to 12V, $V_{OUT(MAX)}$ = 28V, I_Q = 4.5mA, I_{SD} < 25µA, SO-8, MS8
LT1961	1.5A I_{SW}, 1.25MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MAX)}$ = 35V, I_Q = 0.9mA, I_{SD} < 6µA, MS8E
LTC3400/ LTC3400B	600mA I_{SW}, 1.2MHz, Synchronous Step-Up DC/DC Converter	V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$ = 5V, I_Q = 19µA/300µA I_{SD} < 1µA, ThinSOT
LTC3401	1A I_{SW}, 3MHz, Synchronous Step-Up DC/DC Converter	V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$ = 6V, I_Q = 38µA I_{SD} < 1µA, MS10
LTC3402	2A I_{SW}, 3MHz, Synchronous Step-Up DC/DC Converter	V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$ = 6V, I_Q = 38µA I_{SD} < 1µA, MS10
LTC3425	5A I_{SW}, 8MHz, 4-Phase Synchronous Step-Up DC/DC Converter QFN32	V_{IN}: 0.5V to 4.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 12µA, I_{SD} < 1µA,
LTC3429	600mA, 500kHz, Synchronous Step-Up DC/DC Converter with Output Disconnect and Soft-Start	V_{IN}: 0.5V to 5V, $V_{OUT(MAX)}$ = 5V, I_Q = 20µA/300µA I_{SD} < 1µA, ThinSOT
LTC3459	70mA I_{SW}, 10V Micropower Synchronous Boost/Output Disconnect	V_{IN}: 1.5V to 5.5V, $V_{OUT(MAX)}$ = 10V, I_Q = 10µA, ThinSOT
LT3460	320mA I_{SW}, 1.3MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 16V, $V_{OUT(MAX)}$ = 36V, I_Q = 2mA, I_{SD} < 1µA, SC70, ThinSOT
LT3464	85mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter with Integrated Schottky/Output Disconnect	V_{IN}: 2.3V to 10V, $V_{OUT(MAX)}$ = 34V, I_Q = 25µA, I_{SD} < 1µA, ThinSOT

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT0807 REV A • PRINTED IN USA