ABSOLUTE MAXIMUM RATINGS

(Note 1)

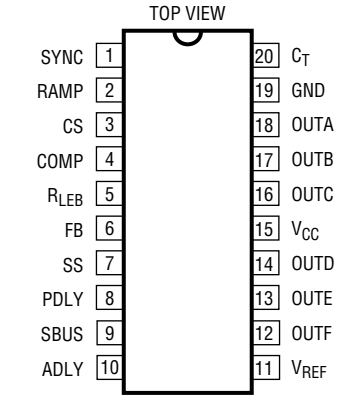
V_{CC} to GND
- Low Impedance Source ..... –0.3V to 10V
- (Chip Self Regulates at 10.3V)

All Other Pins to GND
- (Low Impedance Source) ..... –0.3V to 5.5V

V_{CC} (Current Fed) 25mA
V_{REF} Output Current ..... Self Regulated
Outputs (A, B, C, D, E, F) Current ..... ±100mA
Operating Temperature Range (Note 5)
- LTC1922E ..... –40°C to 85°C
- LTC1922I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
20-LEAD PLASTIC SSOP

N PACKAGE
20-LEAD PDIP

T_{JMAX} = 125°C, θ_{JA} = 110°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 62°C/W (N)

ORDER PART NUMBER
LTC1922EG-1
LTC1922IG-1
LTC1922EN-1
LTC1922IN-1

Consult factory for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at V_{CC} = 9.5V, C_T = 180pF, T_A = T_{MIN} to T_{MAX} unless other wise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
UVLO	Undervoltage Lockout	Measured on V_{CC}			10.25	10.7	V
UVHY	UVLO Hysteresis	Measured on V_{CC}		3.8	4.2		V
I_{CCST}	Start-Up Current	V_{CC} = V_{UVLO} – 0.3V	●		145	250	µA
I_{CCRN}	Operating Current				4	7	mA
V_{SHUNT}	Shunt Regulator Voltage	Current Into V_{CC} = 10mA			10.2	10.8	V
R_{SHUNT}	Shunt Resistance	Current Into V_{CC} = 7mA to 17mA			–1.5	2	Ω
Delay Blocks							
DTHR	Delay Pin Threshold ADLY and PDLY	SBUS = 1.5V SBUS = 2.25V		1.38 2.08	1.50 2.25	1.62 2.42	V V
DHYS	Delay Hysteresis Current ADLY and PDLY	SBUS = 1.5V, ADLY/PDLY = 1.6V		1.1	1.3	1.45	mA
DTMO	Delay Time-Out	SBUS = 1.5V SBUS = 2.25V			600 900		ns ns
DZRT	Zero Delay Threshold	Measured on SBUS		3	4.15	5	V
Phase Modulator							
ROS	RAMP Offset Voltage	Measured on COMP, RAMP = 0V			0.4		V
I_{RMP}	RAMP Discharge Current	RAMP = 1V, COMP = 0V		30	50		mA
I_{SLP}	Slope Compensation Current	Measured on CS, C_T = 1.5V C_T = 3V		35 70	55 110	75 150	µA µA
DCMX	Maximum Phase Shift	COMP = 4V	●	95	99.5		%
DCMN	Minimum Phase Shift	COMP = 0V	●		0.1	0.6	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at V_{CC} = 9.5V, C_T = 180pF, T_A = T_{MIN} to T_{MAX} unless other wise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator							
OSCT	Total Variation	V_{CC} = 6.5V to 9.5V	●	236	277	319	kHz
OSCV	C_T RAMP Amplitude	Measured on C_T		3.6	3.85	4.2	V
OSYT	SYNC Threshold	Measured on SYNC		1.6	1.8	2.2	V
OSYW	Minimum SYNC Pulse Width	Measured at Outputs (Note 2)			6		ns
OSYWX	Maximum SYNC Pulse Width	Measured on Outputs, C_T = 180pF				1.3	µs
OSOP	SYNC Output Pulse Width	Measured on SYNC, R_{SYNC} = 5.1k			170		ns
Error Amplifier							
V_{FB}	FB Input Voltage	COMP = 2.5V (Note 3)		1.179	1.204	1.229	V
FBI	FB Input Range	Measured on FB (Note 4)		–0.3		2.5	V
AVOL	Open-Loop Gain	COMP = 1V to 3V (Note 3)		70	90		dB
I_{IB}	Input Bias Current	COMP = 2.5V (Note 3)			5	50	nA
V_{OH}	Output High	Load on COMP = –100µA		4.7	4.92		V
V_{OL}	Output Low	Load on COMP = 100µA			0.18	0.4	V
I_{SOURCE}	Output Source Current	COMP = 2.5V		–400	–800		µA
I_{SINK}	Output Sink Current	COMP = 2.5V		3	7		mA
Reference							
V_{REF}	Initial Accuracy	T_A = 25°C, Measured on V_{REF}		4.925	5	5.075	V
REFTV	Total Variation	Line, Load and Temperature	●	4.9	5	5.1	V
REFLD	Load Regulation	Load on V_{REF} = 100µA to 5mA			2	15	mV
REFLN	Line Regulation	V_{CC} = 6.5V to 9.5V			0.1	10	mV
REFSC	Short-Circuit Current	V_{REF} Shorted to GND		18	30	45	mA
Outputs							
OUTH(X)	Output High Voltage	$I_{OUT(X)}$ = –50mA		7.9	8.4		V
OUTL(X)	Output Low Voltage	$I_{OUT(X)}$ = 50mA			0.6	1	V
$R_{HI(X)}$	Pull-Up Resistance	$I_{OUT(X)}$ = –50mA to –10mA			22	30	Ω
$R_{LO(X)}$	Pull-Down Resistance	$I_{OUT(X)}$ = –50mA to –10mA			12	20	Ω
$t_{r(X)}$	Rise Time	$C_{OUT(X)}$ = 50pF			5	15	ns
$t_{f(X)}$	Fall Time	$C_{OUT(X)}$ = 50pF			5	15	ns
Current Limit and Shutdown							
CLPP	Pulse-by-Pulse Current Limit Threshold	Measured on CS		0.34	0.415	0.48	V
CLSD	Shutdown Current Limit Threshold	Measured on CS		0.55	0.64	0.73	V
SSI	Soft-Start Current	SS = 2.5V		7	12	17	µA
SSR	Soft-Start Reset Threshold	Measured on SS		0.7	0.4	0.1	V
FLT	FAULT Reset Threshold	Measured on SS		4.4	4.1	3.8	V

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: SYNC pulse width is valid from >20ns and <0.4 • ($1/f_{OSC}$), V_{SYNC} = 0V to 5V.

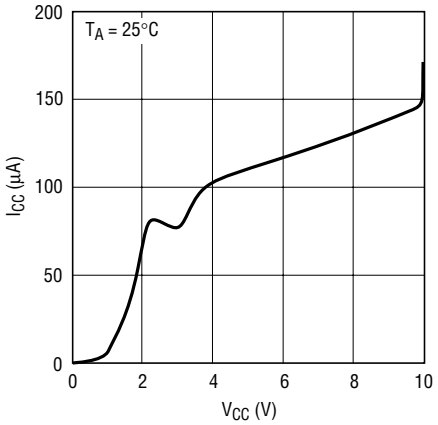
Note 3: FB is driven by a servo loop amplifier to control V_{COMP} for these tests.

Note 4: Set FB to –0.3V, 2.5 and insure that COMP does not phase invert.

Note 5: The LTC1922-1E is guaranteed to meet performance specifications from 0°C to 85°C. Specification over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC1922-1I is guaranteed and tested over the –40°C to 85°C operating temperature range.

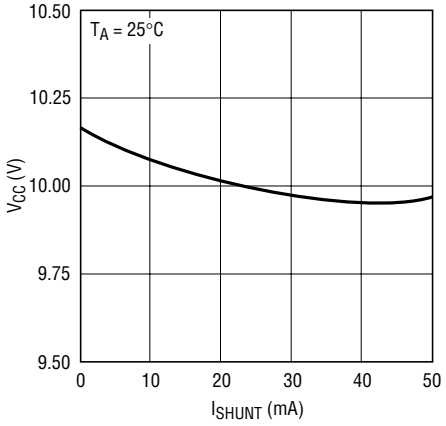
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up I_{CC} vs V_{CC}



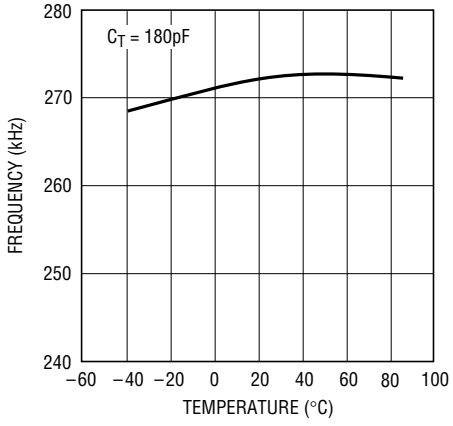
1922 • G01

V_{CC} vs I_{SHUNT}



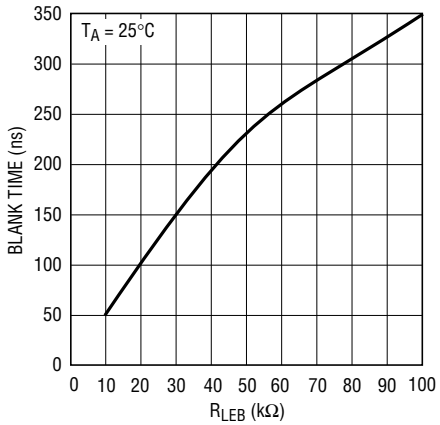
1922 • G02

Oscillator Frequency vs Temperature



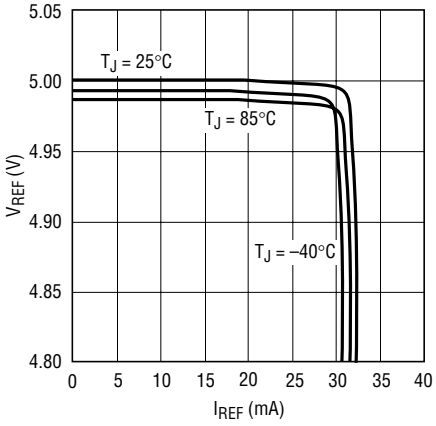
1922 • G03

Leading Edge Blanking Time vs R_{LEB}



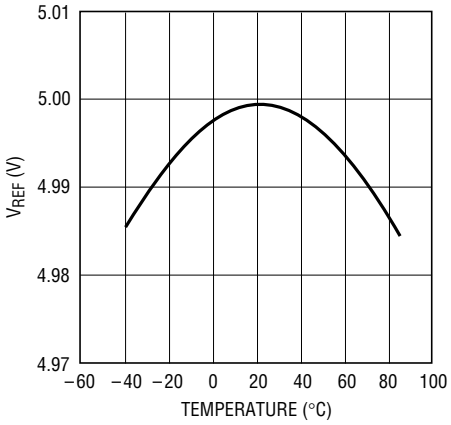
1922 • G04

V_{REF} vs I_{REF}



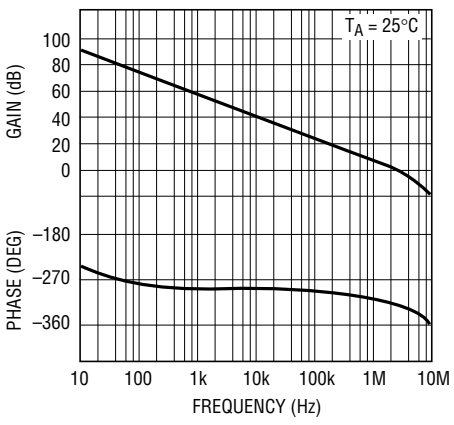
1922 • G05

V_{REF} vs Temperature



1922 • G03

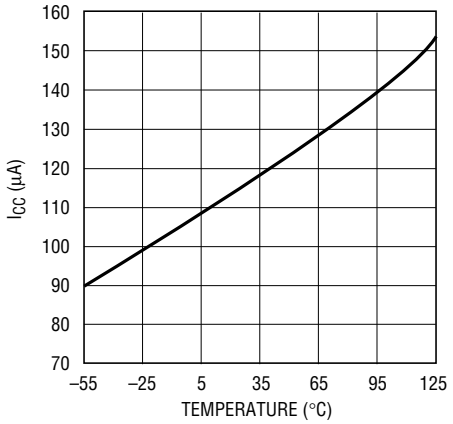
Error Amplifier Gain/Phase



1922 • G07

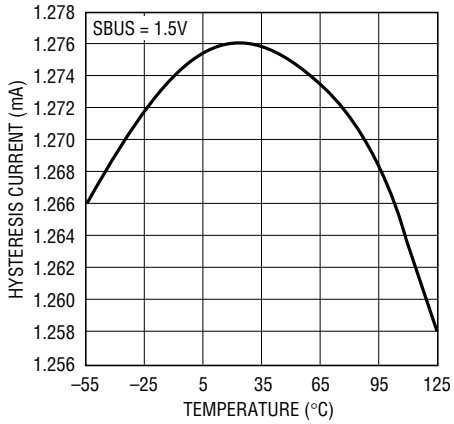
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up I_{CC} vs Temperature



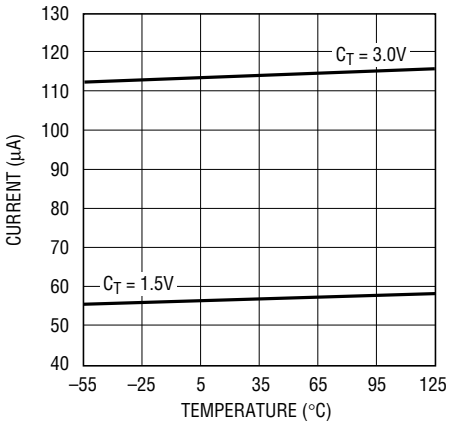
1922 • G10

Delay Hyseresis Current vs Temperature



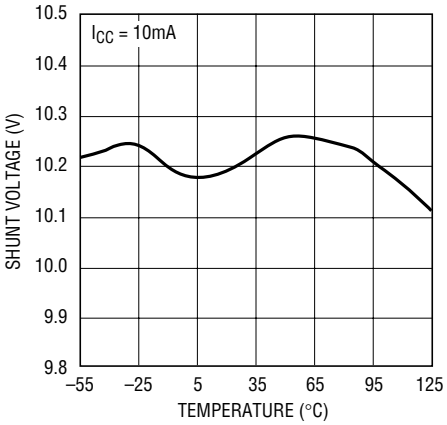
1922 • G11

Slope Current vs Temperature



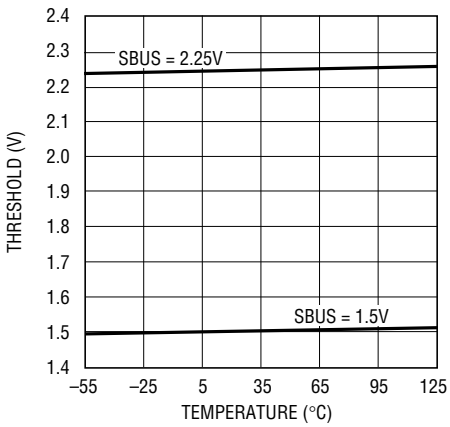
1922 • G12

V_{CC} Shunt Voltage vs Temperature



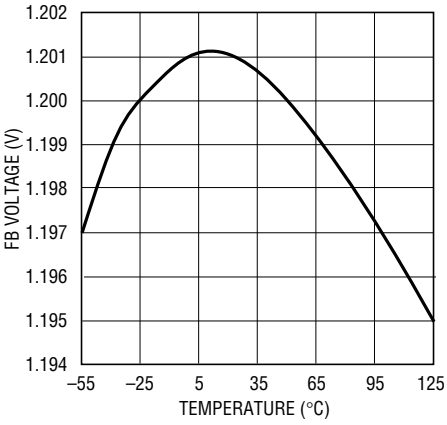
1922 • G13

Delay Pin Threshold vs Temperature



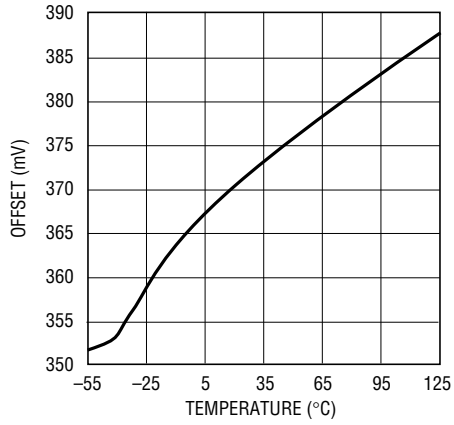
1922 • G14

FB Input Voltage vs Temperature



1922 • G15

Ramp Offset Voltage vs Temperature



1922 • G16

PIN FUNCTIONS

SYNC (Pin 1): Synchronization Input/Output for the Oscillator. Terminate SYNC with a 5.1k resistor to GND.

RAMP (Pin 2): Input to Phase Modulator Comparator. The voltage on RAMP is internally level shifted by 400mV.

CS (Pin 3): Input to Current Limit Comparators, Output of Slope Compensation Circuitry.

COMP (Pin 4): Error Amplifier Output, Input to Phase Modulator.

R_{LEB} (Pin 5): Timing Resistor for Leading Edge Blanking. Use a 10k to 100k resistor to program from 40ns to 310ns of leading edge blanking. A ±1% tolerance resistor is recommended. Leading edge blanking may be defeated by connecting R_{LEB} to V_{REF}.

FB (Pin 6): Error Amplifier Inverting Input. This is the voltage feedback input for the LTC1922-1.

SS (Pin 7): Soft-Start/Restart Delay Circuitry Timing Capacitor.

PDLY (Pin 8): Passive Leg Delay Circuit Input.

SBUS (Pin 9): Input (Bus) Voltage Sensing Input.

ADLY (Pin 10): Active Leg Delay Circuit Input.

V_{REF} (Pin 11): 5V Reference Output. V_{REF} is capable of supplying up to 15mA to external circuitry. Bypass V_{REF} with a 1µF (minimum) ceramic capacitor to GND.

OUTF (Pin 12): 50mA Driver Output for Secondary Side Current Doubler Synchronous Rectifier.

OUTE (Pin 13): 50mA Driver Output for Secondary Side Current Doubler Synchronous Rectifier.

OUTD (Pin 14): 50mA Driver Output for Active Leg Low Side.

V_{CC} (Pin 15): Chip Power Supply Input, 10.3V Shunt Regulator. Bypass V_{CC} with a 0.1µF or larger ceramic capacitor to GND.

OUTC (Pin 16): 50mA Driver Output for Active Leg High Side.

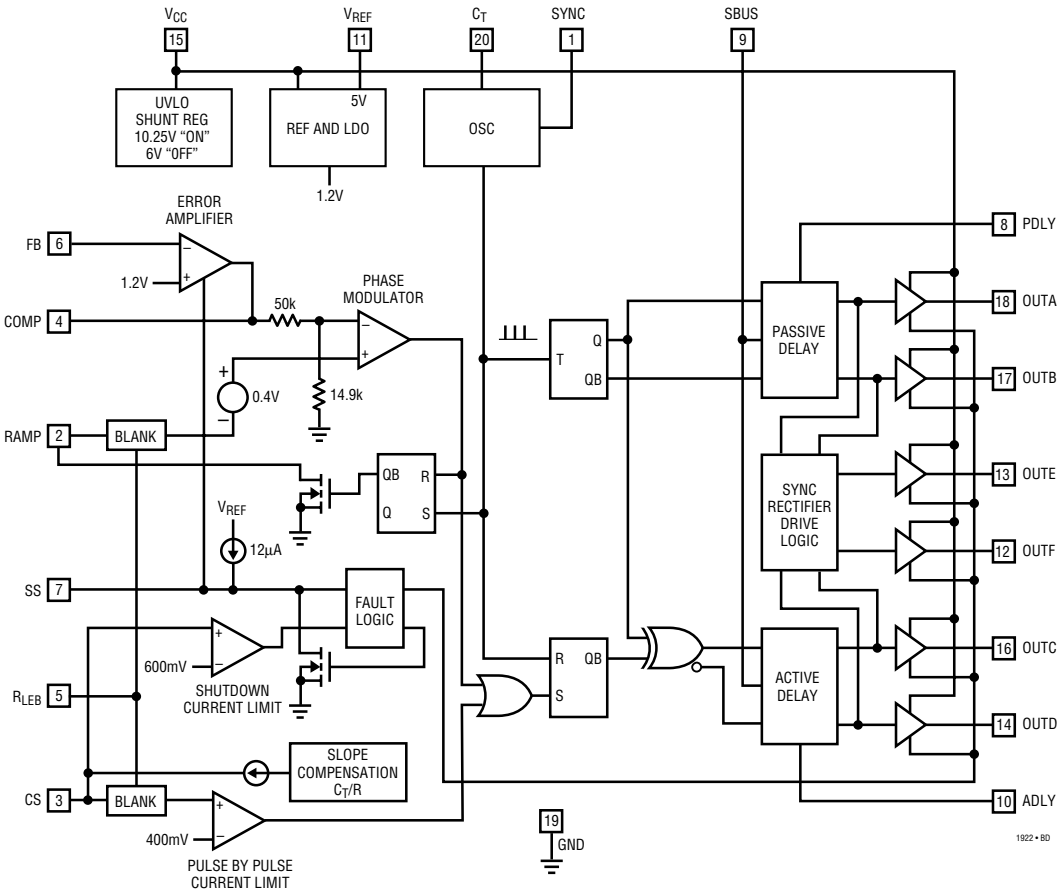
OUTB (Pin 17): 50mA Driver Output for Passive Leg Low Side.

OUTA (Pin 18): 50mA Driver Output for Passive Leg High Side.

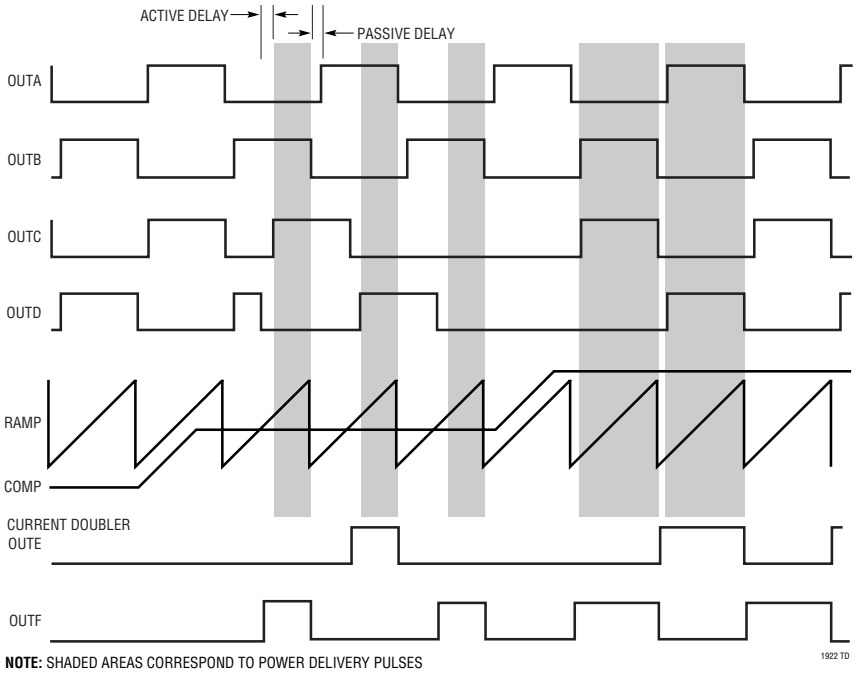
GND (Pin 19): All Voltages on the LTC1922-1 Are Referred to GND.

C_T (Pin 20): Timing Capacitor for Oscillator. Use ±5% or better multilayer NPO ceramic for best results.

BLOCK DIAGRAM



TIMING DIAGRAM



NOTE: SHADED AREAS CORRESPOND TO POWER DELIVERY PULSES

OPERATION

Phase Shift Full-Bridge PWM

Conventional full-bridge switching power supply topologies are often employed for high power, isolated DC/DC and off-line converters. Although they require two additional switching elements, substantially greater power and higher efficiency can be attained for a given transformer size compared to the more common single-ended forward and flyback converters. These improvements are realized since the full-bridge converter delivers power during both parts of the switching cycle, reducing transformer core loss and lowering voltage and current stresses. The full-bridge converter also provides inherent automatic transformer flux reset and balancing due to its bidirectional drive configuration. As a result, the maximum duty cycle range is extended, further improving efficiency. Soft switching variations on the full-bridge topology have been proposed to improve and extend its performance and application. These zero voltage switching (ZVS) techniques exploit the generally undesirable parasitic elements present within the power stage. The parasitic elements are utilized to drive near lossless switching transitions for all of the external power MOSFETs.

LTC1922-1 phase shift PWM controller provides enhanced performance and simplifies the design task required for a ZVS phase shifted full-bridge converter. The primary attributes of the LTC1922-1 as compared to currently available solutions include:

1) Truly adaptive and accurate (DirectSense technology) ZVS switching delays.

Benefit: higher efficiency, higher duty cycle capability, eliminates external trim.

2) Internally generated drive signals for current doubler synchronous rectifiers.

Benefit: eliminates external glue logic, drivers, optimal timing for highest efficiency.

3) Programmable (single resistor) leading edge blanking.

Benefit: prevents spurious operation, reduces external filtering required on CS.

4) Programmable (single resistor) slope compensation.

Benefit: eliminates external glue circuitry.

5) Optimized current mode control architecture.

Benefit: eliminates glue circuitry, less overshoot at start-up, faster recovery from system faults.

6) Proven reference circuits and design tools.

Benefit: substantially reduced learning curve, more time for optimization.

As a result, the LTC1922-1 makes the ZVS topology feasible for a wider variety of applications, including those at lower power levels.

The LTC1922-1 controls four external power switches in a full-bridge arrangement. The load on the bridge is the primary winding of a power transformer. The diagonal switches in the bridge connect the primary winding between the input voltage and ground every oscillator cycle. The pair of switches that conduct are alternated by an internal flip-flop in the LTC1922-1. Thus, the voltage applied to the primary is reversed in polarity on every switching cycle and each output drive signal is 1/2 the frequency of the oscillator. The on-time of each driver signal is slightly less that 50%. The actual percentage is adaptively modulated by the LTC1922-1. The on-time overlap of the diagonal switch pairs is controlled by the LTC1922-1 phase modulation circuitry. (Refer to Block and Timing Diagrams) This overlap sets the approximate duty cycle of the converter. The LTC1922-1 driver output signals (OUTA to OUTF) are optimized for interface with an external gate driver IC or buffer. External power MOSFETs A and C require high side driver circuitry, while B and D are ground referenced and E and F are ground referenced but on the secondary side of the isolation barrier. Methods for providing drive to these elements are detailed in the data sheet. The secondary voltage of the transformer is the primary voltage divided by the transformer turns ratio. Similar to a buck converter, the secondary square wave is applied to an output filter inductor and capacitor to produce a well regulated DC output voltage.

Switching Transitions

The phase shifted full-bridge can be described by four primary operating states. The key to understanding how ZVS occurs is revealed by examining the states in detail.

OPERATION

Each full cycle of the transformer has two distinct periods in which power is delivered to the output, and two "freewheeling" periods. The two sides of the external bridge have fundamentally different operating characteristics that become important when designing for ZVS over a wide load current range. The left bridge leg is referred to as the "passive" leg, while the right leg is referred to as the "active" leg. The following descriptions provide insight as to why these differences exist.

State 1 (Power Pulse 1)

Referring to Figure 1, State 1 begins with MA, MD and MF "ON" and MB, MC and ME "OFF." During the simultaneous conduction of MA and MD, the full input voltage is applied across the transformer primary winding and following the dot convention, V_{IN}/N is applied to the left side of LO1 allowing current to increase in LO1. The primary current during this period is approximately equal to the output inductor current (LO1) divided by the transformer turns ratio plus the transformer magnetizing current ($V_{IN} \bullet t_{ON}/L_{MAG}$). MD turns off and ME turns on at the end of State 1.

State 2 (Active Transition and Freewheel Interval)

MD turns off when the phase modulator comparator transitions. At this instant, the voltage on the MD/MC junction begins to rise towards the applied input voltage (V_{IN}). The transformer's magnetizing current and the reflected output inductor current propels this action. The slew rate is limited by MOSFET MC and MD's output capacitance (C_{OSS}), snubbing capacitance and the transformer interwinding capacitance. The voltage transition on the active leg from the ground reference point to V_{IN} will always occur, independent of load current as long as energy in the transformer's magnetizing and leakage inductance is greater than the capacitive energy. That is, $1/2 \bullet (L_M + L_I) \bullet I_M^2 > 1/2 \bullet 2 \bullet C_{OSS} \bullet V_{IN}^2$ — the worst case occurs when the load current is zero. This condition is usually easy to meet. The magnetizing current is virtually constant during this transition because the magnetizing inductance has positive voltage applied across it throughout the low to high transition. Since the leg is actively driven by this "current source," it is called the active or linear transition. When the voltage on the active leg has risen to V_{IN}, MOSFET MC is switched on by the LTC1922-1 DirectSense circuitry. The primary current now flows through the two high side MOSFETs (MA and MC). The transformer's secondary windings are electrically shorted at this time since both ME and MF are "ON". As long as positive current flows in LO1 and LO2, the transformer primary (magnetizing) inductance is also shorted through normal transformer action. MA and MF turn off at the end of State 2.

State 3 (Passive Transition)

MA turns off when the oscillator timing period ends, i.e., the clock pulse toggles the internal flip-flop. At the instant MA turns off, the voltage on the MA/MB junction begins to decay towards the lower supply (GND). The energy available to drive this transition is limited to the primary leakage inductance and added commutating inductance which have ($I_{MAG} + I_{OUT}/2N$) flowing through them initially. The magnetizing and output inductors don't contribute any energy because they are effectively shorted as mentioned previously, significantly reducing the available energy. This is the major difference between the active and passive transitions. If the energy stored in the leakage and commutating inductance is greater than the capacitive energy, the transition will be completed successfully. During the transition, an increasing reverse voltage is applied to the leakage and commutating inductances, helping the overall primary current to decay. The inductive energy is thus resonantly transferred to the capacitive elements, hence, the term passive or resonant transition. Assuming there is sufficient inductive energy to propel the bridge leg to GND, the time required will be approximately equal to $\pi \bullet \sqrt{LC}/2$. When the voltage on the passive leg nears GND, MOSFET MB is commanded "ON" by the LTC1922-1 DirectSense circuitry. Current continues to increase in the leakage and external series inductance which is opposite in polarity to the reflected output inductor current. When this current is equal in magnitude to the reflected output current, the primary current reverses direction, the opposite secondary winding becomes forward biased and a new power pulse is initiated. The time required for the current reversal reduces the effective maximum duty cycle

OPERATION

and must be considered when specifying the power transformer. If ZVS is required over the entire range of loads, a small commutating inductor is added in series with the primary to aid with the passive leg transition, since the leakage inductance alone is usually not sufficient and predictable enough to guarantee ZVS over the full load range.

State 4 (Power Pulse 2)

During power pulse 2, current builds up in the primary winding in the opposite direction as power pulse 1. The primary current consists of reflected output inductor current and current due to the primary magnetizing inductance. At the end of State 4, MOSFET MC turns off and an active transition, essentially similar to State 2, but opposite in direction (high to low) takes place.

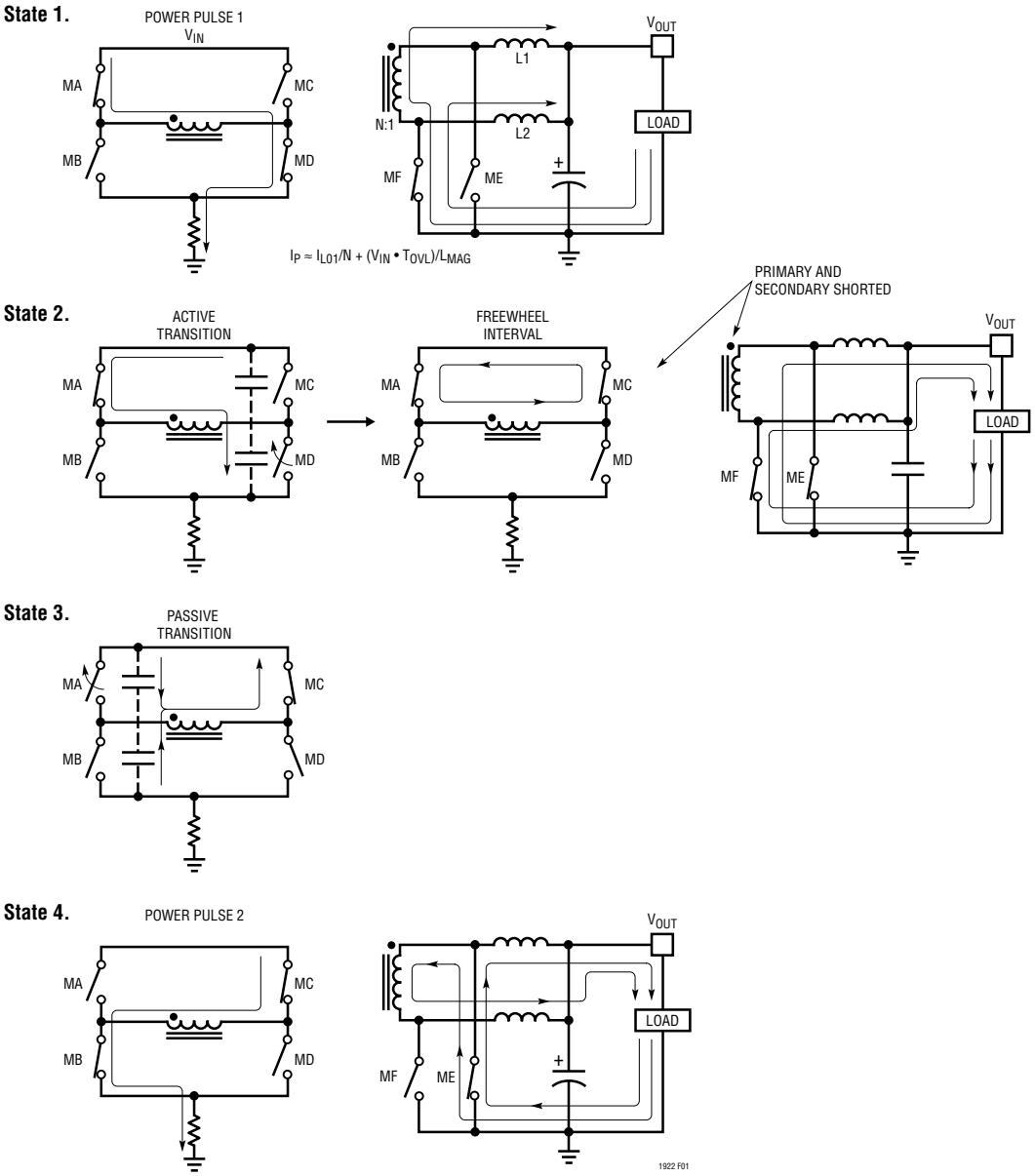


Figure 1. ZVS Operation

OPERATION

Zero Voltage Switching (ZVS)

A lossless switching transition requires that the respective full-bridge MOSFETs be switched to the "ON" state at the exact instant their drain to source voltage is zero. Delaying the turn-on results in lower efficiency due to circulating current flowing in the body diode of the primary side MOSFET rather than its low resistance channel. Premature turn-on produces hard switching of the MOSFETs, increasing noise and power dissipation. Previous solutions have attempted to meet these requirements with fixed or first order (linear) variable open-loop time delays. Open-loop methods typically set the turn-on delay to the worst case longest bridge transition time expected plus the tolerances of all the internal and external delay timing circuitry. These error tolerances can be quite significant, while the optimal transition times over the load current range vary nonlinearly. In a volume production environment, these factors can necessitate an external trim to guarantee ZVS operation, adding cost to the final product. An additional side effect of longer than required delays is a decrease in the effective maximum duty cycle. Reduced duty cycle range can mandate a lower transformer turns ratio, impacting efficiency or requiring a lower switching frequency, impacting size.

LTC1922-1 Adaptive Delay Circuitry

The LTC1922-1 addresses the issue of nonideal switching delays with novel DirectSense circuitry that intelligently monitors both the input supply and instantaneous bridge leg voltages, and commands a switching transition when the expected zero voltage condition is reached. In effect, the LTC1922-1 "closes the loop" on the ZVS turn-on delay requirements. DirectSense technology provides optimal turn-on delay timing, regardless of input voltage, output load, or component tolerances and greatly simplifies the power supply design process. The DirectSense technique requires only a simple voltage divider sense network to implement. If there is not enough energy to fully commutate the bridge leg to a ZVS condition, the LTC1922-1 automatically overrides the DirectSense circuitry and forces a transition. The LTC1922-1 delay circuitry can also be overridden, by tying SBUS to V_{REF}.

Adaptive Mode

The LTC1922-1 is configured for adaptive delay sensing with three pins, ADLY, PDLY and SBUS. ADLY and PDLY sense the active and passive delay legs respectively via a voltage divider network as shown in Figure 2.

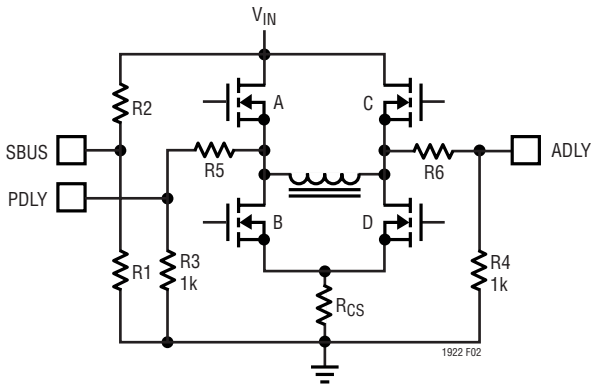


Figure 2. Adaptive Mode

The threshold voltage on PDLY and ADLY for both the rising and falling transitions is set by the voltage on SBUS. A buffered version of this voltage is used as the threshold level for the internal DirectSense circuitry. At nominal V_{IN}, the voltage on SBUS is set to 1.5V by an external voltage divider between V_{IN} and GND, making this voltage directly proportional to V_{IN}. The LTC1922-1 DirectSense circuitry uses this characteristic to zero voltage switch all of the external power MOSFETs, independent of input voltage.

ADLY and PDLY are connected through voltage dividers to the active and passive bridge legs respectively. The lower resistor in the divider is set to 1k. The upper resistor in the divider is divided into one, two or three equal value resistors to reduce its overall capacitance. In off-line applications, this is usually required anyway to stay within the maximum voltage ratings of the resistors. One or two resistor segments will work for most nominal 48V or lower V_{IN} applications.

To set up the ADLY and PDLY resistors, first determine at what drain to source voltage to turn-on the MOSFETs. Finite delays exist between the time at which the LTC1922-1 controller output transitions, to the time at which the power MOSFET switches on due to MOSFET turn on delay and external driver circuit delay. Ideally, we want the power MOSFET to switch at the instant there is zero volts across it. By setting a threshold voltage for ADLY and

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PDLY corresponding to several volts across the MOSFET, the LTC1922-1 can "anticipate" a zero voltage VDS and signal the external driver and switch to turn-on. The amount of anticipation can be tailored for any application by modifying the upper divider resistor(s). The LTC1922-1 DirectSense circuitry sources a trimmed current out of PDLY and ADLY after a low to high level transition occurs. This provides hysteresis and noise immunity for the PDLY and ADLY circuitry, and sets the high to low threshold on ADLY or PDLY to nearly the same level as the low to high threshold, thereby making the upper and lower MOSFET VDS switch points virtually identical, independent of V_{IN}.

Example: V_{IN} = 48V nominal (36V to 72V)

1. Set up SBUS: 1.5V is desired on SBUS with V_{IN} = 48V. Set divider current to 100µA.

   R1 = 1.5V/100µA = 15k.

   R2 = (48V – 1.5V)/100µA = 465k.

   An optional small capacitor (0.001µF) can be added across R1 to decouple noise from this input.

2. Set up ADLY and PDLY: 7V of "anticipation" are required in this circuit to account for the delays of the external MOSFET driver and gate drive components.

   R3, R4 = 1k, sets a nominal 1.5mA in the divider chain at the threshold.

   R5, R6 = (48V – 7V – 1.5V)/1.5mA = 26.3k, use (2) equal 13k segments.

Zero Delay Mode

The LTC1922-1 provides the flexibility through the SBUS pin to disable the DirectSense delay circuitry. See Figure 3 for details.

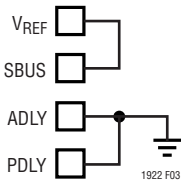

Figure 3. Zero Delays

Powering the LTC1922-1

The LTC1922-1 utilizes an integrated V_{CC} shunt regulator to serve the dual purposes of limiting the voltage applied to V_{CC} as well as signaling that the chip's bias voltage is sufficient to begin switching operation (under voltage lockout). With its typical 10.2V turn-on voltage and 4.2V UVLO hysteresis, the LTC1922-1 is tolerant of loosely regulated input sources such as an auxiliary transformer winding. The V_{CC} shunt is capable of sinking up to 25mA of externally applied current. The UVLO turn-on and turn-off thresholds are derived from an internally trimmed reference making them extremely accurate. In addition, the LTC1922-1 exhibits very low (145µA typ) start-up current that allows the use of 1/8W to 1/4W trickle charge start-up resistors.

The trickle charge resistor should be selected as follows:

$$R_{START(MAX)} = V_{IN(MIN)} – 10.7V/250µA$$

Adding a small safety margin and choosing standard values yields:

APPLICATION	V_{IN} RANGE	R_{START}
DC/DC	36V to 72V	100k
Off-Line	85V to 270V_{RMS}	430k
PFC Preregulator	390V_{DC}	1.4M

V_{CC} should be bypassed with a 0.1µF to 1µF multilayer ceramic capacitor to decouple the fast transient currents demanded by the output drivers and a bulk tantalum or electrolytic capacitor to hold up the V_{CC} supply before the bootstrap winding, or an auxiliary regulator circuit takes over.

$$C_{HOLDUP} = (I_{CC} + I_{DRIVE}) \bullet t_{DELAY}/3.8V$$
(minimum UVLO hysteresis)

Regulated bias supplies as low as 7V can be utilized to provide bias to the LTC1922-1. Refer to Figure 4 for various bias supply configurations.

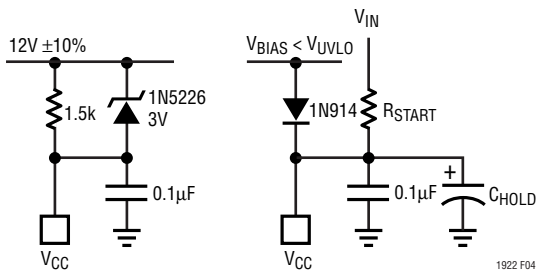

Figure 4. Bias Configurations

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Off-Line Bias Supply Generation

If a regulated bias supply is not available to provide V_{CC} voltage to the LTC1922-1 and supporting circuitry, one must be generated. Since the power requirement is small, approximately 1W, and the regulation is not critical, a simple open-loop method is usually the easiest and lowest cost approach. One method that works well is to add a winding to the main power transformer, and post regulate the resultant square wave with an L-C filter (see Figure 5a). The advantage of this approach is that it maintains decent regulation as the supply voltage varies, and it does not require full safety isolation from the input winding of the transformer. Some manufacturers include a primary winding for this purpose in their standard product offerings as well. A different approach is to add a winding to the output inductor and peak detect and filter the square wave signal (see Figure 5b). The polarity of this winding is designed so that the positive voltage square wave is produced while the output inductor is freewheeling. An advantage of this technique over the previous is that it does not require a separate filter inductor and since the voltage is derived from the well-regulated output voltage, it is also well controlled. One disadvantage is that this winding will require the same safety isolation that is required for the main transformer. Another disadvantage is that a much larger V_{CC} filter capacitor is needed, since it does not generate a voltage as the output is first starting up, or during short-circuit conditions.

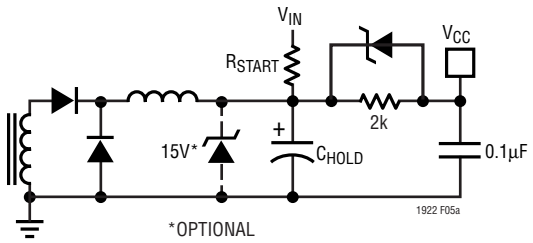

Figure 5a. Auxiliary Winding Bias Supply

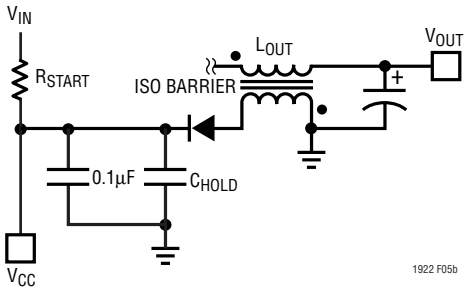

Figure 5b. Output Inductor Bias Supply

Programming the LTC1922-1 Oscillator

The high accuracy LTC1922-1 oscillator circuit provides flexibility to program the switching frequency, slope compensation, and synchronization with minimal external components. The LTC1922-1 oscillator circuitry produces a 3.8V peak-to-peak amplitude ramp waveform on C_T and a narrow pulse on SYNC that can be used to synchronize other PWM chips. Typical maximum duty cycles of 99% are obtained at 300kHz and 97% at 1MHz. The large amplitude ramp provides a high degree of noise margin. A compensating slope current is derived from the oscillator ramp waveform and sourced out of CS.

The desired amount of slope compensation is selected with single external resistor (or no resistor), if not required. A capacitor to GND on C_T programs the switching frequency. The C_T ramp discharge current is internally set to a high value (>10mA). The dedicated SYNC I/O pin easily achieves synchronization. The LTC1922-1 can be set up to either synchronize other PWM chips or be synchronized by another chip or external clock source. The 1.8V SYNC threshold allows the LTC1922-1 to be synchronized directly from all standard 3V and 5V logic families.

Design Procedure:

1. Choose C_T for the desired oscillator frequency. The switching frequency selected must be consistent with the power magnetics and output power level. This is detailed in the Transformer Design section. In general, increasing the switching frequency will decrease the maximum achievable output power, due to limitations of maximum duty cycle imposed by transformer core reset and ZVS. Remember that the output frequency is 1/2 that of the oscillator.

$$C_T = 1/(20k \bullet f_{OSC})$$

Example: Desired f_{OSC} = 330kHz

C_T = 1/(20k • 330kHz) = 152pF, choose closest standard value of 150pF. A 5% or better tolerance multilayer NPO or X7R ceramic capacitor is recommended for best performance.

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2. The LTC1922-1 can either synchronize other PWMs, or be synchronized to an external frequency source or PWM chip. See Figure 6 for details.

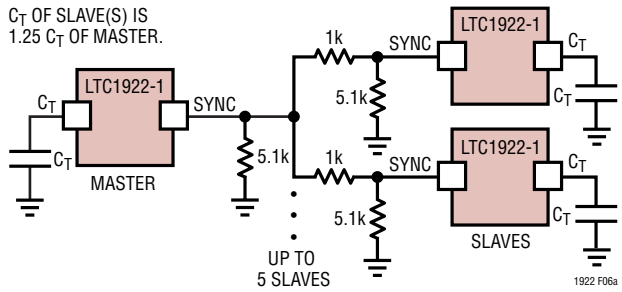

Figure 6a. SYNC Output (Master Mode)

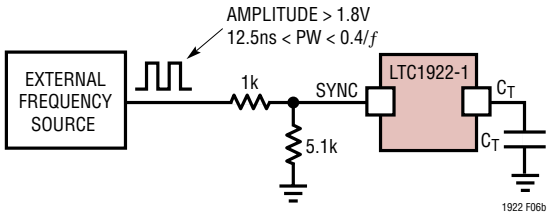

Figure 6b. SYNC Input from an External Source

3. Slope compensation is required for most peak current mode controllers in order to prevent subharmonic oscillation of the current control loop. In general, if the system duty cycle exceeds 50% in a fixed frequency, continuous current mode converter, an unstable condition exists within the current control loop. Any perturbation in the current signal is amplified by the PWM modulator resulting in an unstable condition. Some common manifestations of this include alternate pulse nonuniformity and pulse width jitter. Fortunately, this can be addressed by adding a corrective slope to the current sense signal or by subtracting the same slope from the current command signal (error amplifier output). In theory, the current doubler output configuration does not require slope compensation since the output inductor duty cycles only approach 50%. However, transient conditions can momentarily cause higher duty cycles and therefore, the possibility for unstable operation. The exact amount of required slope compensation is easily programmed by the LTC1922-1 with the addition of a single external resistor (see Figure 7). The LTC1922-1 generates a current that is proportional to the instantaneous voltage on C_T, ($33\mu A/V_{(CT)}$). Thus, at the peak of C_T, this current is approximately 125µA and is output from the CS pin. A resistor connected between CS and the external current sense resistor sums in the required amount of slope compensation. The value of this resistor is dependent on several factors including minimum V_{IN}, V_{OUT}, switching frequency, current sense resistor value and output inductor value. An illustrative example with the design equation is provided below.

Example: V_{IN} = 36V to 72V

V_{OUT} = 3.3V

I_{OUT} = 40A

L = 2.2µH

Transformer turns ratio (N) = $V_{IN(MIN)} \bullet D_{MAX}/V_{OUT}$ = 3

R_{CS} = 0.025Ω

f_{SW} = 300kHz, i.e., transformer f = $f_{SW}/2$ = 150kHz

$R_{SLOPE} = V_O \bullet R_{CS}/(2 \bullet L \bullet f_T \bullet 125\mu A \bullet N) = 3.3V \bullet 0.025/(2 \bullet 2.2\mu A \bullet 100k \bullet 125\mu A \bullet 3)$

R_{SLOPE} = 500Ω, choose the next higher standard value to account for tolerances in I_{SLOPE}, R_{CS}, N and L.

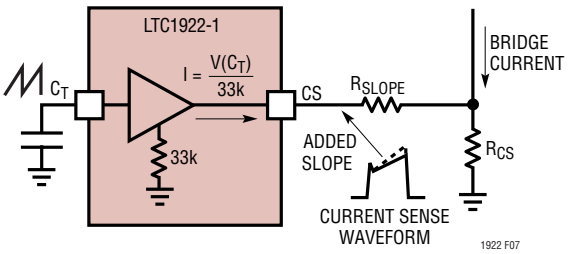

Figure 7. Slope Compensation Circuitry

Current Sensing and Overcurrent Protection

Current sensing provides feedback for the current mode control loop and protection from overload conditions. The LTC1922-1 is compatible with either resistive sensing or current transformer methods. Internally connected to the LTC1922-1 CS pin are two comparators that provide pulse-by-pulse and overcurrent shutdown functions respectively. (See Figure 8)

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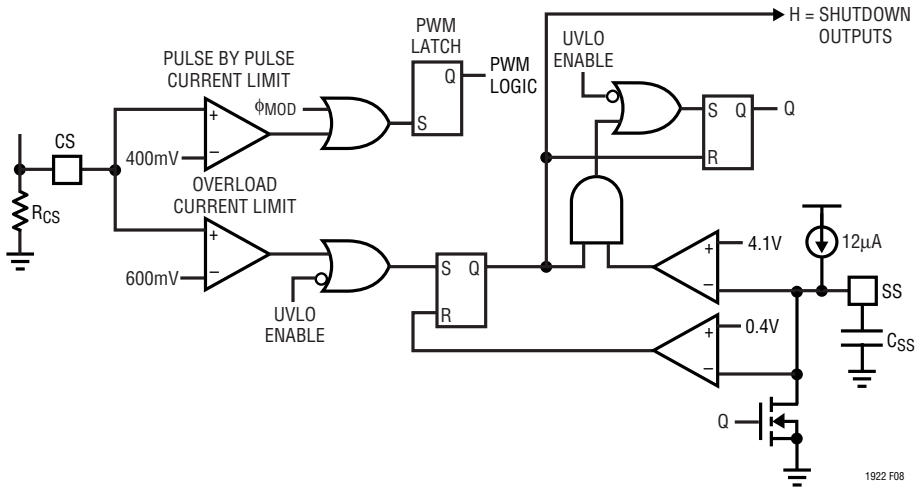

Figure 8. Current Sense/Fault Circuitry Detail

The pulse-by-pulse comparator has a 400mV nominal threshold, which can reduce sense resistor losses by 67% compared to previous solutions. This corresponds to 3W in a 200W, 48V to 3.3V converter. If the 400mV threshold is exceeded, the PWM cycle is terminated. The overcurrent comparator is set approximately 50% higher than the pulse-by-pulse level. If the current signal exceeds this level, the PWM cycle is terminated, the soft-start capacitor is quickly discharged and a soft-start cycle is initiated. If the overcurrent condition persists, the LTC1922-1 halts PWM operation and waits for the soft-start capacitor to charge up to approximately 4V before a retry is allowed. The soft-start capacitor is charged by an internal 12µA current source. If the fault condition has not cleared when soft-start reaches 4V, the soft-start pin is again discharged and a new cycle is initiated. This is referred to as hiccup mode operation. In normal operation and under most abnormal conditions, the pulse-by-pulse comparator is fast enough to prevent hiccup mode operation. In severe cases, however, with high input voltage, very low $RDS_{(ON)}$ MOSFETs and a shorted output, or with saturating magnetics, the overcurrent comparator provides a means of protecting the power converter.

Leading Edge Blanking

The LTC1922-1 provides programmable leading edge blanking to prevent nuisance tripping of the current sense circuitry. Although the ZVS full-bridge topology is somewhat more immune to leading edge noise spikes than other types of converters, they are not totally eliminated. Leading edge blanking relieves the filtering requirements for the CS pin, greatly improving the response to real overcurrent conditions. It also allows the use of a ground referenced current sense resistor or transformer(s), further simplifying the design. With a single 10k to 100k resistor from R_{LEB} to GND, blanking times of approximately 40ns to 320ns are programmed. If not required, connecting R_{LEB} to V_{REF} can disable leading edge blanking. Keep in mind that the use of leading edge blanking will set a minimum linear control range for the phase modulation circuitry.

Resistive Sensing

A resistor connected between input common and the sources of MB and MD is the simplest, fastest and most accurate method of current sensing for the full-bridge converter. This is the preferred method for low to moderate power levels. A graph of resistive sense power losses vs output power is shown Figure 9. The sense resistor should be chosen such that the maximum rated output current for the converter can be delivered at the lowest expected V_{IN}. Use the following formula to calculate the optimal value for R_{CS}.

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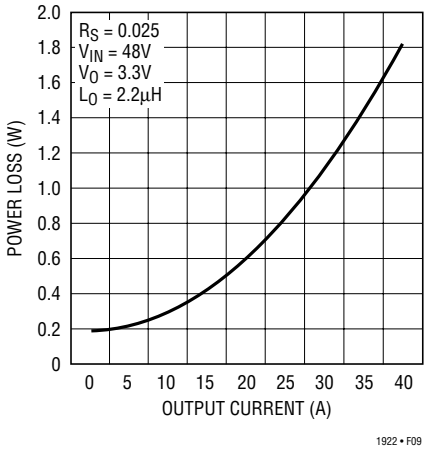

Figure 9. R_{SENSE} Power Loss vs I_{OUT}

If RAMP and CS are connected together:

$$R_{CS} = \frac{0.4V - (125\mu A \bullet R_{SLOPE})}{I_P(PEAK)}$$

$$I_P(PEAK) = \frac{I_{O(MAX)}}{2 \bullet N \bullet EFF} + \frac{V_{IN(MAX)} \bullet 2 \bullet D_{MIN}}{L_{MAG} \bullet f_{CLK}} + \frac{V_O(1 - D_{MIN})}{L_{OUT} \bullet f_{CLK} \bullet N}$$

where: N = Transformer turns ratio

If RAMP and CS are separated

$$R_{CS} = \frac{0.4V}{I_P(PEAK)}$$

Current Transformer Sensing

A current sense transformer can be used in lieu of resistive sensing with the LTC1922-1. Current sense transformers are available in many styles from several manufacturers. A typical sense transformer for this application will use a 1:50 turns ratio (N), so that the sense resistor value is N times larger, and the secondary current N times smaller than in the resistive sense case. Therefore, the sense resistor power loss is about N times less with the transformer method, neglecting the transformers core and copper losses. The disadvantages of this approach include, higher cost and complexity, lower accuracy, core reset/max duty cycle limitations and lower speed. Nevertheless, for very high power applications, this method is preferred. The sense transformer primary is placed in the same location as the ground referenced sense resistor, or between the upper MOSFET drains in the (MA, MC) and V_{IN}. The advantage of the high side location is a greater immunity to leading edge noise spikes, since gate charge current and reflected rectifier recovery current are largely eliminated. Figure 10 illustrates a typical current sense transformer based sensing scheme. R_S in this case is calculated the same as in the resistive case, only its value is increased by the sense transformer turns ratio. At high duty cycles, it may become difficult or impossible to reset the current transformer. This is because the required transformer reset voltage increases as the available time for reset decreases to equalize the (volt • seconds) applied. The interwinding capacitance and secondary inductance of the current sense transformer form a resonant circuit that limits the dV/dT on the secondary of the CS transformer. This in turn limits the maximum achievable duty cycle for the CS transformer. Attempts to operate beyond this limit will cause the transformer core to "walk" and eventually saturate, opening up the current feedback loop.

Common methods to address this limitation include:

1. Reducing the maximum duty cycle by lowering the power transformer turns ratio.
2. Reducing the switching frequency of the converter.
3. Employ external active reset circuitry.
4. Using two CS transformers summed together.
5. Choose a CS transformer optimized for high frequency applications.

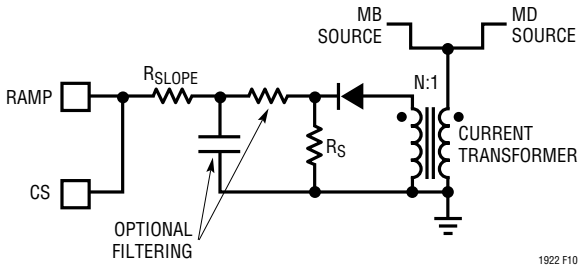

Figure 10. Current Transformer Sense Circuitry

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Phase Modulator

The LTC1922-1 phase modulation control circuitry is comprised of the phase modulation comparator and logic, the error amplifier, and the soft-start amplifier (see Figure 11). Together, these elements develop the required phase overlap (duty cycle) required to keep the output voltage in regulation. In isolated applications, the sensed output voltage error signal is fed back to COMP across the input to output isolation boundary by an optical coupler and shunt reference/error amplifier (LT®1431) combination. The FB pin is connected to GND, forcing COMP high. The collector of the optoisolator is connected to COMP directly. The voltage COMP is internally attenuated by the LTC1922-1. The attenuated COMP voltage provides one input to the phase modulation comparator. This is the current command. The other input to the phase modulation comparator is the RAMP voltage, level shifted by approximately 400mV. This is the current loop feedback. During every switching cycle, alternate diagonal switches (MA-MD or MB-MC) conduct and cause current in an output inductor to increase. This current is seen on the primary of the power transformer divided by the turns ratio. Since the current sense resistor is connected between GND and the two bottom bridge transistors, a voltage proportional to the output inductor current will be seen across R_{SENSE}. The high side of R_{SENSE} is also connected to RAMP and CS, usually through a small resistor (R_{SLOPE}). When the voltage on RAMP/CS exceeds either COMP/5.2 – 400mV, or 400mv, the overlap conduction period will terminate. During normal operation, the attenuated COMP voltage will determine the RAMP/CS trip point. During start-up, or slewing conditions following a large load step, the 400mV CS threshold will terminate the cycle, as COMP will be driven high, such that the attenuated version exceeds the 400mV threshold. In extreme conditions, the 600mV threshold on CS will be exceeded, invoking a soft-start/restart cycle.

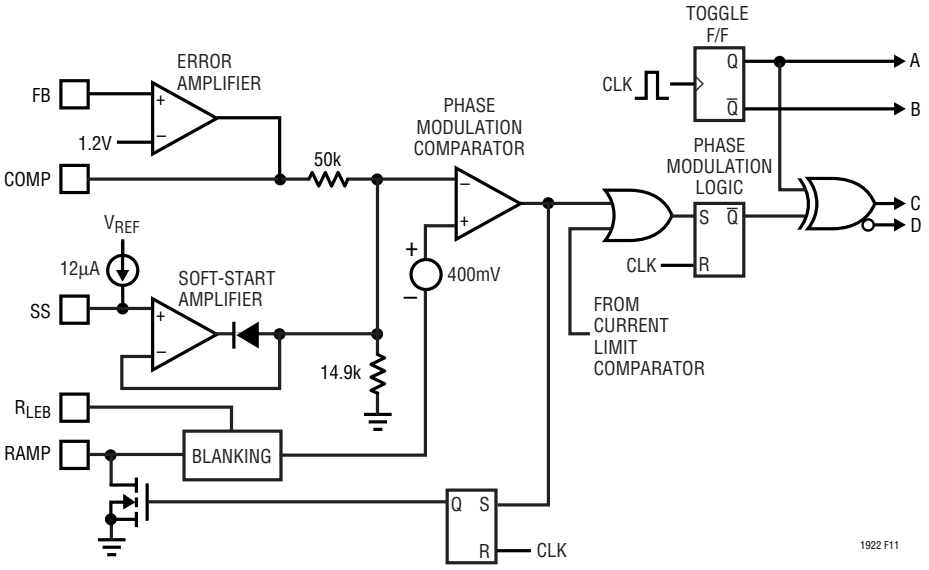

Figure 11. Phase Modulation Circuitry

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Selecting the Power Stage Components

Perhaps the most critical part of the overall design of the converter is selecting the power MOSFETs, transformer, inductors and filter capacitors. Tremendous gains in efficiency, transient performance and overall operation can be obtained as long as a few simple guidelines are followed with the phase shifted full-bridge topology.

Power Transformer

This guide is aimed at selecting readily available standard "off the shelf" transformers. The basic requirements, however, apply to custom transformer designs as well. Switching frequency, core material characteristics, series resistance and input/output voltages all play an important role in transformer selection. Close attention also needs to be paid to leakage and magnetizing inductances as they play an important role in how well the converter will achieve ZVS. Planar magnetics are very well suited to these applications because of their excellent control of these parameters.

Turns Ratio

The required turns ratio for a current doubler secondary is given below. Depending on the magnetics selected, this value may need to be reduced slightly.

Turns ratio formula:

$$N = 2 \bullet \frac{V_{IN(MIN)} \bullet D_{MAX}}{V_{OUT}}$$

where:

$V_{IN(MIN)}$ = Minimum V_{IN} for operation

D_{MAX} = Maximum duty cycle of controller

Magnetizing, Output, and Leakage Inductors

A lower value of magnetizing and output inductance will improve the ability of the converter to achieve ZVS over the full range of loads and reduce the size of the external commutating inductor. One of the trade-offs is increased primary referred ripple current which has a small negative impact on efficiency. Other factors to consider are switching frequency and required maximum duty cycle. A lower value of magnetizing inductance will require a longer time to reset the core, cutting into the available duty cycle range. As switching frequencies increase, this becomes more significant. In general, the magnetizing inductance value should be the lowest value required in order to achieve the necessary maximum duty cycle at the chosen switching frequency. Output inductor value determines the magnitude of output ripple current and therefore the ripple voltage along with the output capacitors. Generally speaking, the output inductance should be minimized as much as possible in order to improve transient response. In addition, output capacitance ESR should be minimized as much as possible. Using the equations below, plug in the manufacturers magnetizing inductance value and a "starting value" of commutating inductance (1% of L_{MAG}) to verify that a sufficient max duty cycle can be achieved at the desired switching frequency. Next, use equation (2) to determine what the absolute minimum required L_{COM} is to guarantee ZVT over the entire load range. One or two iterations may be required in order to arrive at the final selections.

MAX DC vs L_{COM} at f_{SW}

$$MAX\,DC \geq \frac{2 - f_{SW} \bullet T_R}{2}; \quad (1)$$

where:

T_R = transformer reset time (worst case)

$$= \frac{I_{O(MAX)} \bullet f_{SW} \bullet L_{MAG} + V_{IN} \bullet 2 \bullet D \bullet N}{f_{SW} \bullet L_{MAG} \bullet N} \left(\frac{L_{COM} + L_L}{V_{IN}} \right)$$

L_{COM} vs ZVS vs Load

$$L_{COM} + L_L = \frac{4/3\ C_{OSS} \bullet L_{MAG}^2 \bullet f_{SW}^2}{2 \bullet D^2} \quad (2)$$

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where:

C_{OSS} = MOSFET D-S capacitance
I_{MAG} = magnetizing inductance
f_{SW} = switching frequency
D = duty cycle
L_L = leakage inductance

For a 48V to 3.3V/5V, 200W converter, the following values were derived:

f_{SW} : 300kHz
L_{MAG} : 100µH
L_{COM} : 0.9µH
L_{OUT} : 2.2µH

Turns Ratio (N) = 2.5

Output Capacitors

Output capacitor selection has a dramatic impact on ripple voltage, dynamic response to transients and stability. Capacitor ESR along with output inductor ripple current will determine the peak-to-peak voltage ripple on the output. The current doubler configuration is advantageous because it has inherent ripple current reduction. The dual output inductors deliver current to the output capacitor 180 degrees out of phase, in effect, partially canceling each other's ripple current. This reduction is maximized at high duty cycle and decreases as the duty cycle reduces. This means that a current doubler converter requires less output capacitance for the same performance as a conventional converter. By determining the minimum duty cycle for the converter, worse-case V_{OUT} ripple can be derived by the formula given below.

$$V_{ORIPPLE} = I_{RIPPLE} \bullet ESR = \frac{V_O \bullet ESR}{L_O \bullet 2 \bullet f_{SW}} (1-D)(1-2D)$$

where:

D = minimum duty cycle

f_{SW} = oscillator frequency

L_O = output inductance

ESR = output capacitor series resistance

The amount of bulk capacitance required is usually system dependent, but has some relationship to output inductance value, switching frequency, load power and dynamic load characteristics. Polymer electrolytic capacitors are the preferred choice for their combination of low ESR, small size and high reliability. For less demanding applications, or those not constrained by size, aluminum electrolytic capacitors are commonly applied. Most DC/DC converters in the 100kHz to 300kHz range use 20µF to 25µF of bulk capacitance per watt of output power. Converters switching at higher frequencies can usually use less bulk capacitance. In systems where dynamic response is critical, additional high frequency capacitors, such as ceramics, can substantially reduce voltage transients,

Power converter stability is, to a large extent, determined by the choice of output capacitor. A zero in the converter's transfer function is given by $1/(2\pi \bullet ESR \bullet C_O)$. Aluminum electrolytic ESR is highly variable with temperature, increasing by about 4× at cold temperatures, making the ESR zero frequency highly variable. Polymer electrolytic ESR is essentially flat with temperature. This characteristic simplifies loop compensation and allows for a much faster responding power supply compared to one with aluminum electrolytic capacitors. Specific details on loop compensation are given in the Compensation section of the data sheet.

Power MOSFETs

The full-bridge power MOSFETs should be selected for their $R_{DS(ON)}$ and BV_{DSS} ratings. Select the lowest BV_{DSS} rated MOSFET available for a given input voltage range leaving at least a 20% voltage margin. Conduction losses are directly proportional to $R_{DS(ON)}$. Since the full-bridge has two MOSFETs in the power path most of the time, conduction losses are approximately equal to:

$2 \bullet R_{DS(ON)} \bullet I^2$, where $I = I_O/2N$

Switching losses in the MOSFETs are dominated by the power required to charge their gates, and turn-on and turn-off losses. At higher power levels, gate charge power is seldom a significant contributor to efficiency loss. ZVS operation virtually eliminates turn-on losses. Turn-off losses are reduced by the use of an external drain to source

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snubber capacitor and/or a very low resistance turn-off driver. If synchronous rectifier MOSFETs are used on the secondary, the same general guidelines apply. Keep in mind, however, that the BV_{DSS} rating needed for these can be greater than $V_{IN(MAX)}/N$, depending on how well the secondary is snubbed. Without snubbing, the secondary voltage can ring to levels far beyond what is expected due to the resonant tank circuit formed between the secondary leakage inductance and the C_{OSS} (output capacitance) of the synchronous rectifier MOSFETs.

Switching Frequency Selection

Unless constrained by other system requirements, the power converter's switching frequency is usually set as high as possible while staying within the desired efficiency target. The benefits of higher switching frequencies are many including smaller size, weight and reduced bulk capacitance. In the full-bridge phase shift converter, these principles are generally the same with the added complication of maintaining zero voltage transitions, and therefore, higher efficiency. ZVS is achieved in a finite time during the switching cycle. During the ZVS time, power is not delivered to the output; the act of ZVS reduces the maximum available duty cycle. This reduction is proportional to maximum output power since the parasitic capacitive element (MOSFETs) that increase ZVS time get larger as power levels increase. This implies an inverse relationship between output power level and switching frequency. Table 1 displays recommended maximum switching frequency vs power level for a 30V/75V in to 3.3V/5V out converter. Higher switching frequencies can be used if the input voltage range is limited, the output voltage is lower and/or lower efficiency can be tolerated.

Table 1.Switching Frequency vs Power Level

<50W	600kHz
<100W	450kHz
<200W	300kHz
<500W	200kHz
<1kW	150kHz
<2kW	100kHz

Closing the Feedback Loop

Closing the feedback loop with the full-bridge converter involves identifying where the power stage and other system poles/zeroes are located and then designing a compensation network around the converters error amplifier to shape the frequency response to insure adequate phase margin and transient response. Additional modifications will sometimes be required in order to deal with parasitic elements within the converter that can alter the feedback response. The compensation network will vary depending on the load current range and the type of output capacitors used. In isolated applications, the compensation network is generally located on the secondary side of the power supply, around the error amplifier of the optocoupler driver, usually an LT1431or equivalent. In nonisolated systems, the compensation network is located around the LTC1922-1's error amplifier.

In current mode control, the dominant system pole is determined by the load resistance (V_O/I_O) and the output capacitor $1/(2\pi \bullet R_O \bullet C_O)$. The output capacitors ESR $1/(2\pi \bullet ESR \bullet C_O)$ introduces a zero. Excellent DC line and load regulation can be obtained if there is high loop gain at DC. This requires an integrator type of compensator around the error amplifier. A procedure is provided for deriving the required compensation components. More complex types of compensation networks can be used to obtain higher bandwidth if necessary.

Step 1. Calculate location of minimum and maximum output pole:

$$F_{P1(MIN)} = 1/(2\pi \bullet R_{O(MAX)} \bullet C_O)$$

$$F_{P1(MAX)} = 1/(2\pi \bullet R_{O(MIN)} \bullet C_O)$$

Step 2. Calculate ESR zero location:

$$F_{Z1} = 1/(2\pi \bullet R_{ESR} \bullet C_O)$$

Step 3. Calculate the feedback divider gain:

$$R_B/(R_B + R_T) \text{ or } V_{REF}/V_{OUT}$$

If Polymer electrolytic output capacitors are used, the ESR zero can be employed in the overall loop compensation and optimum bandwidth can be achieved. If aluminum electrolytics are used, the loop will need to be rolled off prior to the ESR zero frequency, making the loop response

OPERATION

slower. A linearized SPICE macromodel of the control loop is very helpful tool to quickly evaluate the frequency response of various compensation networks.

Polymer Electrolytic (see Figure 12) $1/(2\pi C_C R_I)$ sets a low frequency pole. $1/(2\pi C_C R_F)$ sets the low frequency zero. The zero frequency should coincide with the worst-case lowest output pole frequency. The pole frequency and mid frequency gain (R_F/R_I) should be set such so that the loop crosses over zero dB with a –1 slope at a frequency lower than ($f_{SW}/8$). Use a bode plot to graphically display the frequency response. An optional higher frequency pole set by CP2 and R_f is used to attenuate switching frequency noise.

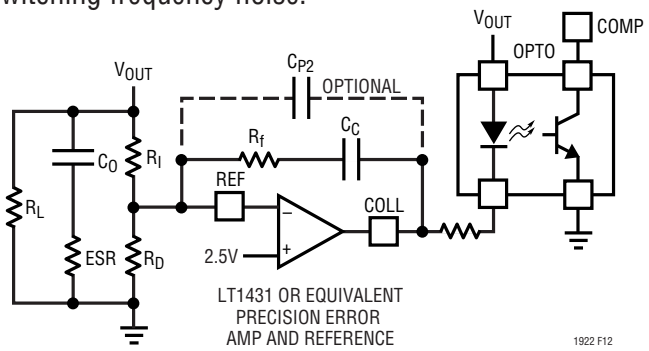

Figure 12. Compensation for Polymer Electrolytic

Aluminum Electrolytic (see Figure 12) the goal of this compensator will be to cross over the output minimum pole frequency. Set a low frequency pole with C_C and R_{IN} at a frequency that will cross over the loop at the output pole minimum F, place the zero formed by C_C and R_f at the output pole F.

Synchronous Rectification

The LTC1922-1 produces the precise timing signals necessary to control current doubler secondary side synchronous MOSFETs on OUTE and OUTF. Synchronous rectifiers are used in place of Schottky or Silicon diodes on the secondary side of the power supply. As MOSFET $R_{DS(ON)}$ levels continue to drop, significant efficiency improvements can be realized with synchronous rectification, provided that the MOSFET switch timing is optimized. An additional benefit realized with synchronous rectifiers is bipolar output current capability. These characteristics improve transient response, particularly overshoot, and improve ZVS ability at light loads.

Current Doubler

The current doubler secondary employs two output inductors that equally share the output load current. The transformer secondary is not center-tapped. This configuration provides 2× higher output current capability compared to similarly sized single output inductor modules, hence the name. Each output inductor is twice the inductance value as the equivalent single inductor configuration and the transformer turns ratio is 1/2 that of a single inductor secondary. The drive to the inductors is 180 degrees out of phase which provides partial ripple current cancellation in the output capacitor(s). Reduced capacitor ripple current lowers output voltage ripple and enhances the capacitors's reliability. The amount of ripple cancellation is related to duty cycle (see Figure 13). Although the current doubler requires an additional inductor, the inductor core volume is proportional to LI^2, thus the size penalty is small. The transformer construction is simplified without a center-tap winding and the turns ratio is reduced by 1/2 compared to a conventional full wave rectifier configuration.

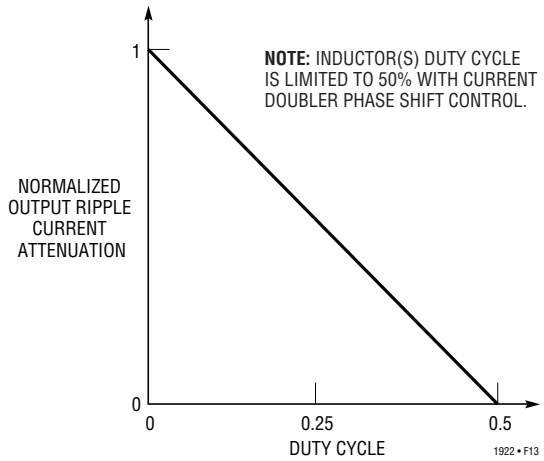

Figure 13. Ripple Current Cancellation vs Duty Cycle

Synchronous rectification of the current doubler secondary requires two ground referenced N-channel MOSFETs. The timing of the LTC1922-1 drive signals is shown in the Timing Diagram. Synchronous rectifier turn-on is internally delayed by the LTC1922-1 after OUT (C or D) turn-off—just after the end of a power cycle. Synchronous rectifier turn-off occurs coincident with OUT (A or B) turn-off. This gives a passive transition time margin before

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the start of a new power cycle. A noninverting MOSFET driver such as the LTC1693-1 (Figure 14) is used so that a single signal transformer with secondary center tap can be employed to translate the drive signals from the primary to the secondary side. In the event of overcurrent shutdown, or UVLO condition, both synchronous rectification MOSFETs are driven on in order to protect the load circuitry.

Full-Bridge Gate Drive

The full-bridge converter requires high current MOSFET gate driver circuitry for two ground referenced switches and two high side referred switches. Providing drive to the ground referenced switches is not too difficult as long as the traces from the gate driver chip or buffer to the gate and source leads are short and direct. Drive requirements are further eased since all of the switches turn on with zero VDS, eliminating the "Miller" effect. Low turn-off resistance is critical, however, in order to prevent excessive turn-off losses resulting from the same Miller effects that were not an issue for turn on. The LTC1922-1 does not require the propagation delays of the high and low side drive circuits to be precisely matched as the DirectSense ZVS circuitry will adapt accordingly, unlike previous solutions. As a result, LTC1922-1 can drive a simple NPN-PNP buffer or a gate driver chip like the LTC1693-1 to provide the low side gate drive. Providing drive to the high side presents additional challenges since the MOSFET gate must be driven above the input supply. A simple circuit (Figure 15) using a single LTC1693-1, an inexpensive signal transformer, and a few discrete components provides both high side gate drives (A and C) reliably.

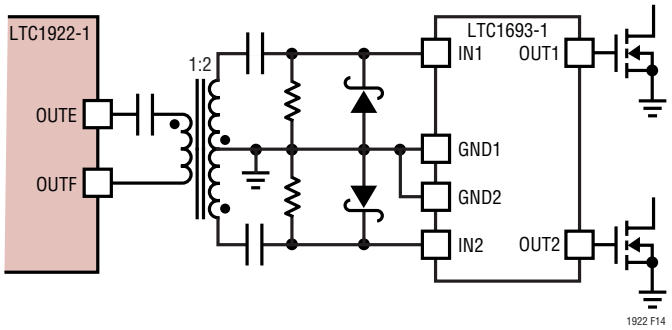


Figure 14. Isolated Drive Circuitry

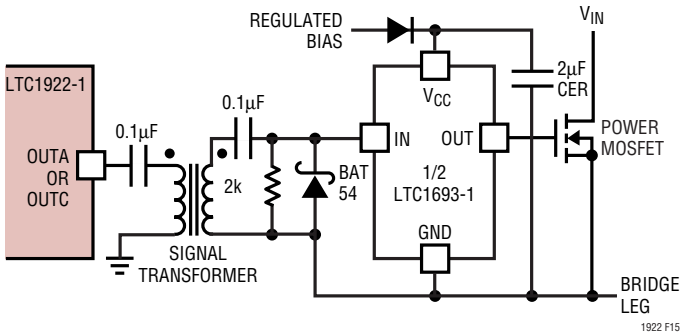
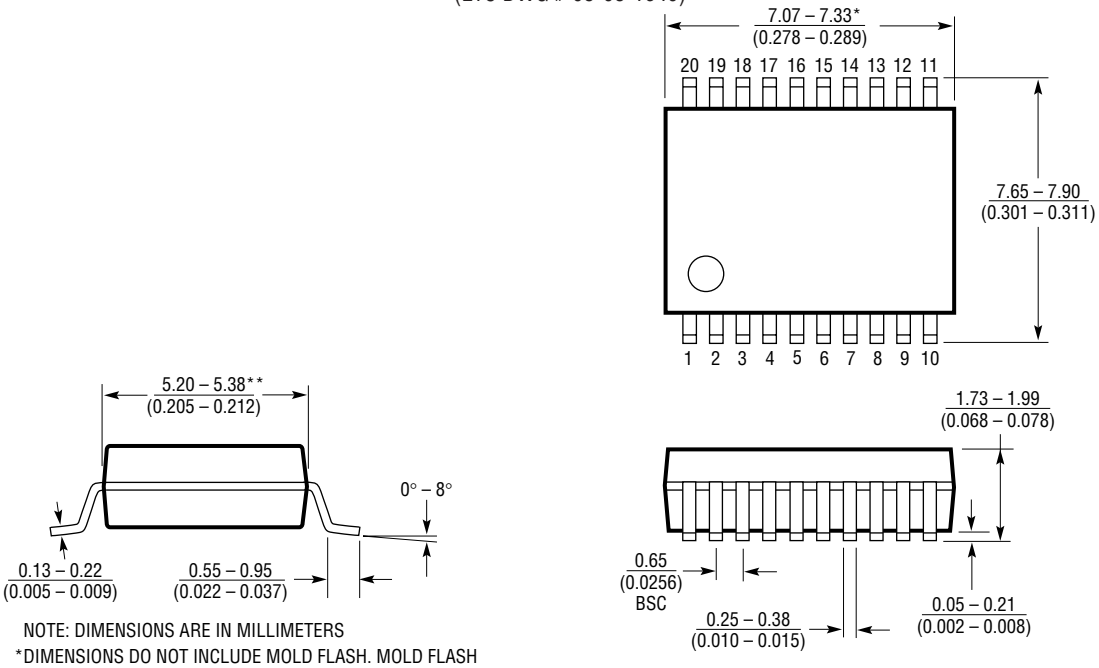


Figure 15. High Side Gate Driver Circuitry

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
20-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



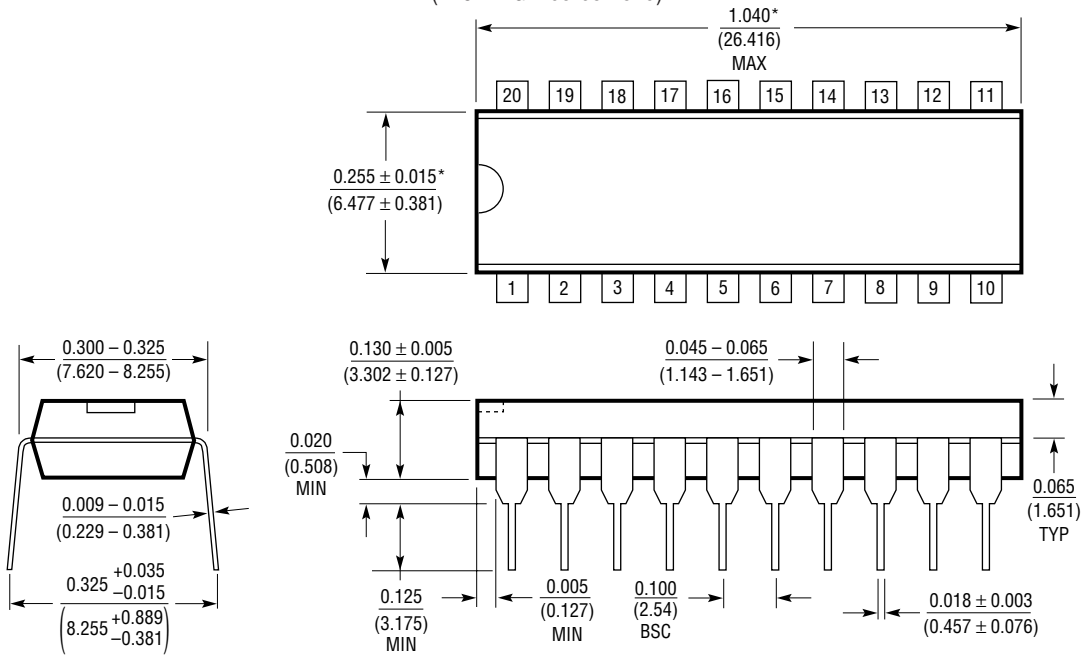
NOTE: DIMENSIONS ARE IN MILLIMETERS

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.152mm (0.006") PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.254mm (0.010") PER SIDE

G20 SSOP 1098

N Package
20-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)

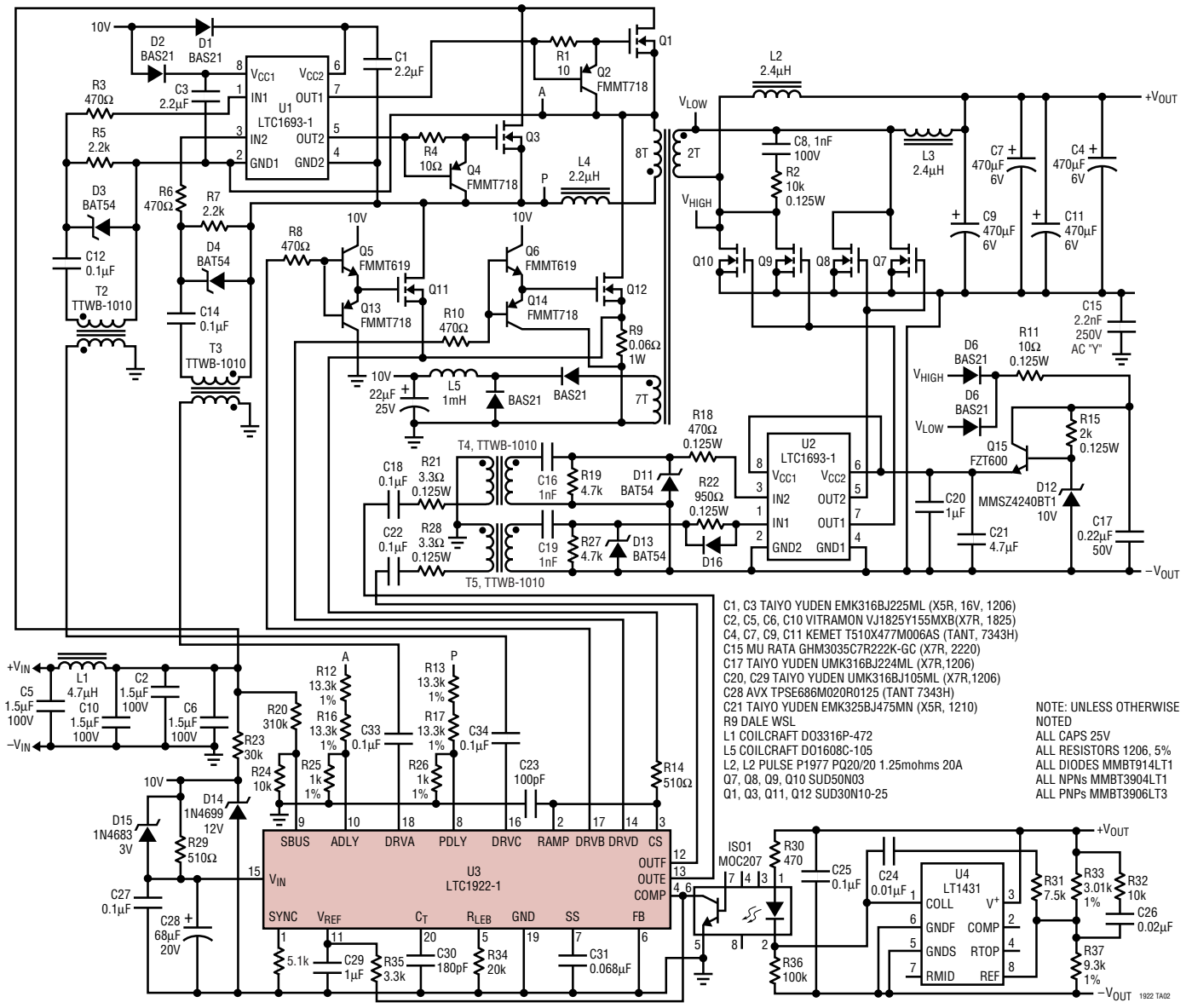


*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

N20 1098

TYPICAL APPLICATION

Synchronous Phase Shifted Full Bridge 48V to 3.3V, 40A Isolated Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1105	Off-Line Switching Regulator	Built-In Isolated Regulation without Optoisolator
LT1681/LTC1698	36V to 72V Input Isolated DC/DC Converter Chipset	Synchronous Rectification; Overcurrent, Overvoltage, UVLO Protection; Power Good Output Signal;h Voltage Margining; Compact Solution
LT1683	Ultralow Noise Push-Pull DC/DC Converter	Minimizes Conducted and Radiated EMI; Reduces Need for Filters, Shields and PCB Iterations
LTC1693-1	High Speed Dual MOSFET Driver	1.5A Peak Output Current; 4.5V ≤ V_{IN} ≤ 13.2V
LT1725	General Purpose Isolated Flyback Controller	48V to 5V Conversion; No Optoisolator Required

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