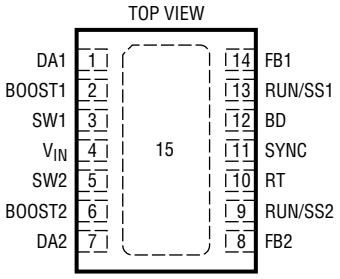
ABSOLUTE MAXIMUM RATINGS

(Note 1)

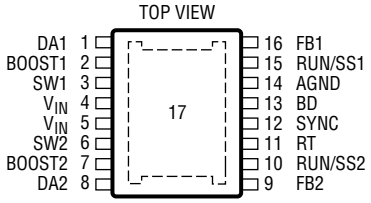
V_{IN} Pin (Note 2) 60V
BD Pin.....20V
BOOST Pins 60V
BOOST Pins above SW 30V
RUN/SS, FB, RT, SYNC pins.....6V
Operating Junction Temperature Range (Notes 3, 6)
LT3509E ..... –40°C to 125°C
LT3509I ..... –40°C to 125°C
LT3509H..... –40°C to 150°C

Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.)
MSOP Package .....300°C

PIN CONFIGURATION



DE14 PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
θ_{JA} = 43°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSOP
θ_{JA} = 43°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3509EDE#PBF	LT3509EDE#TRPBF	3509	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3509IDE#PBF	LT3509IDE#TRPBF	3509	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3509EMSE#PBF	LT3509EMSE#TRPBF	3509	16-Lead Plastic MSOP with Exposed Pad	–40°C to 125°C
LT3509IMSE#PBF	LT3509IMSE#TRPBF	3509	16-Lead Plastic MSOP with Exposed Pad	–40°C to 125°C
LT3509HMSE#PBF	LT3509HMSE#TRPBF	3509	16-Lead Plastic MSOP with Exposed Pad	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Undervoltage Lockout				3.3	3.6	V
V_{IN} Overvoltage Lockout			37	38.5	40	V
Input Quiescent Current	Not Switching V_{FB} > 0.8V			1.9	2.2	mA
Input Shutdown Current	V(RUN/SS[1,2]) < 0.3V			9	15	µA
Feedback Pin Voltage		●	0.784	0.8	0.816	V
Reference Voltage Line Regulation	3.6V < V_{IN} < 36V			0.01		%/V
RUN/SS Shutdown Threshold			0.4	0.6	0.8	V
RUN/SS Voltage for Full I_{OUT}					2	V
RUN/SS Pin Pull-up Current			0.7	1	1.3	µA
Feedback Pin Bias Current (Note 4)	V_{FB} = 0.8V	●		90	500	nA
Switch Current Limit		●	1.05	1.4	1.9	A
DA Comparator Current Threshold			0.7	0.95	1.2	A
Boost Pin Current	I_{SW} = 0.9A			22	36	mA
Switch Leakage Current				0.01	1.0	µA
Switch Saturation Voltage	I_{SW} = 0.9A (Note 5)			0.32		V
Minumum Boost Voltage above Switch	I_{SW} = 0.9A			1.5	2.2	V
Boost Diode Forward Voltage	I_{BD}= 20mA			0.7	0.9	V
Boost Diode Leakage	V_R = 30V			0.1	5	µA
Switching Frequency	R_T = 40.2kΩ R_T = 180kΩ R_T = 14.1kΩ	●	0.92 237 2.0	1.0 260 2.15	1.08 290 2.5	MHz kHz MHz
Sync Pin Input Threshold				1.0		V
Switch Minimum Off-Time		●		80	150	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. Absolute Maximum Voltage at the V_{IN} pin is 60V for non-repetitive 1 second transients and 36V for continuous operation.

Note 3. The LT3509E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3509I is guaranteed over the full –40°C to 125°C temperature range. The LT3509H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4. Current flows out of pin.

Note 5. Switch Saturation Voltage is guaranteed by design.

Note 6. This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

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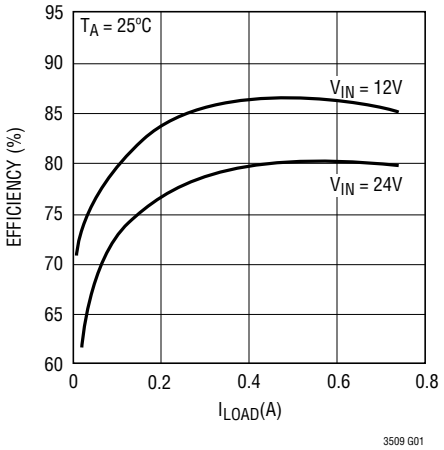
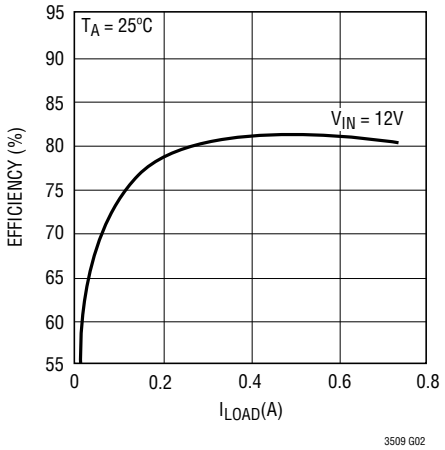
TYPICAL PERFORMANCE CHARACTERISTICS

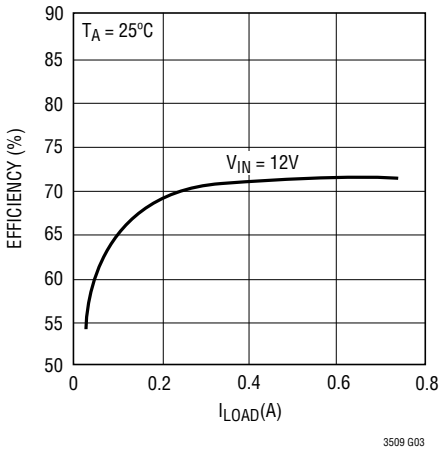
Efficiency vs Load Current
V_{OUT} = 5V, f_{SW} = 2.0MHz



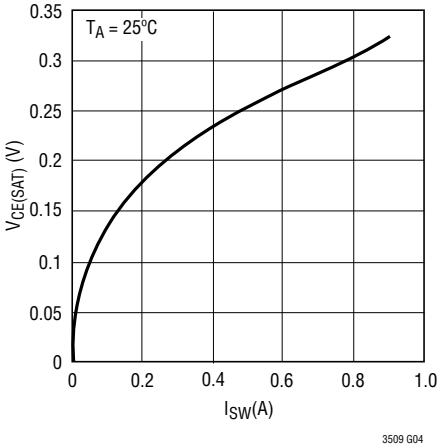
Efficiency vs Load Current
V_{OUT} = 3.3V, f_{SW} = 2.0MHz



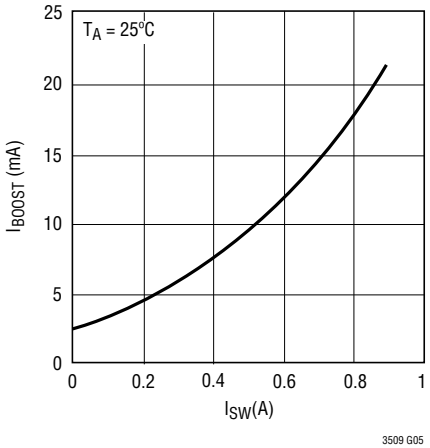
Efficiency vs Load Current
V_{OUT} = 1.8V, f_{SW} = 0.7MHz



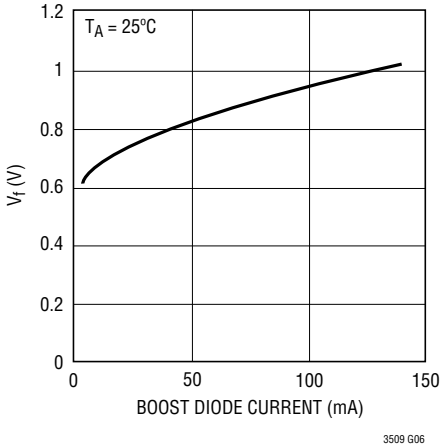
Switch $V_{CE(SAT)}$ vs I_{SW}



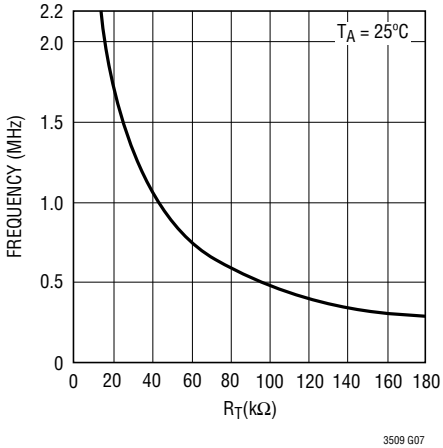
I_{BOOST} vs I_{SW}



Boost Diode Characteristics



Frequency vs R_T



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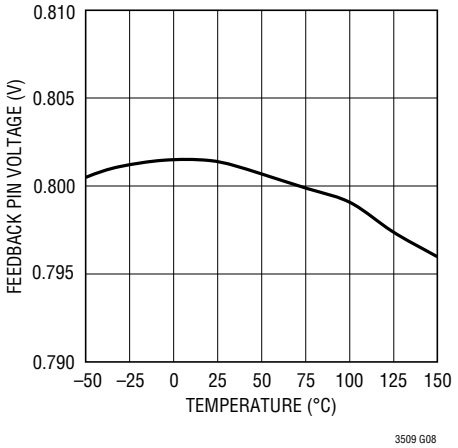
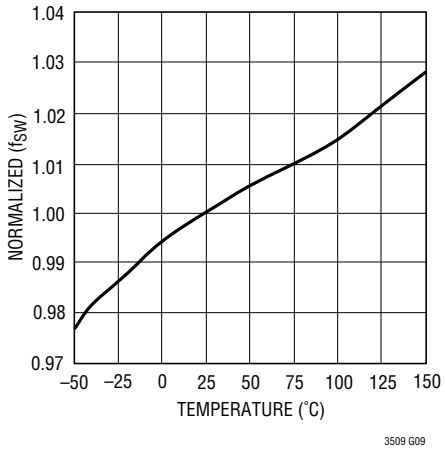
TYPICAL PERFORMANCE CHARACTERISTICS

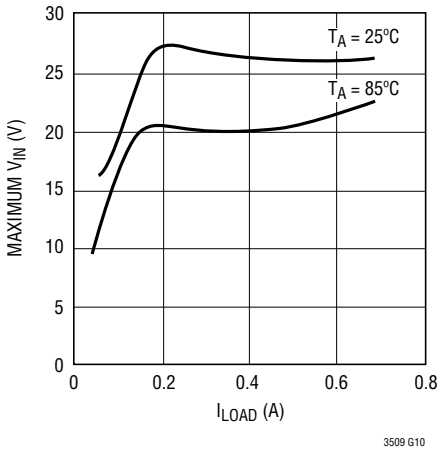
FB Pin Voltage vs Temperature



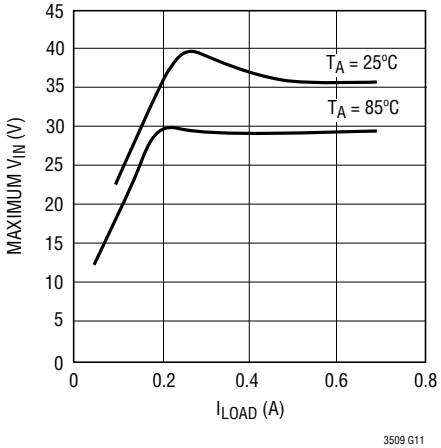
f_{SW} vs Temperature (Measured at 1MHz)



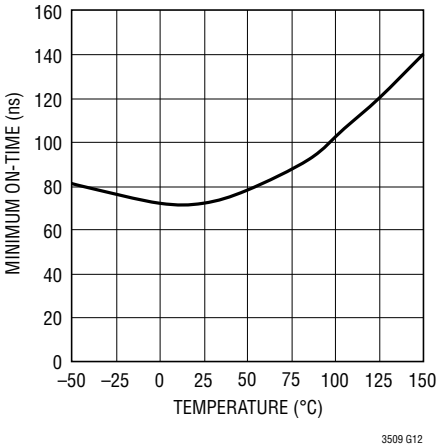
Max V_{IN} for Constant Frequency V_{OUT} = 3.3V, f_{SW} = 2MHz



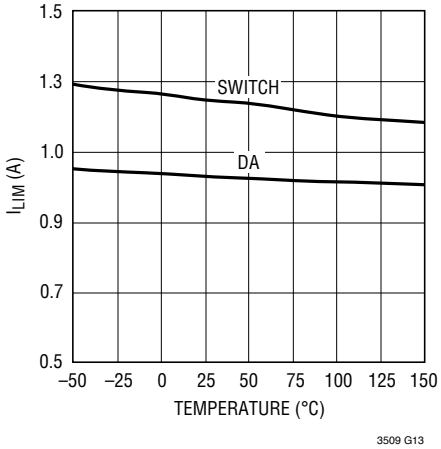
Max V_{IN} for Constant Frequency V_{OUT} = 5V, f_{SW} = 2MHz



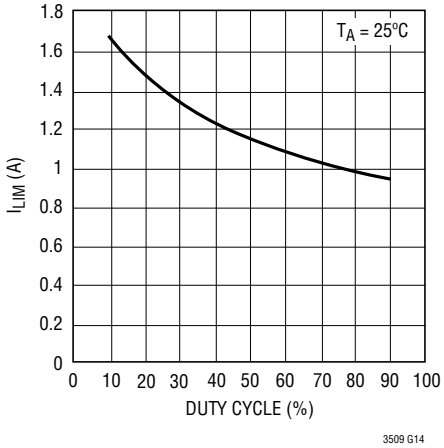
Minimum On-Time vs Temperature, I_{LOAD} = 0.3A



I_{LIM} vs Temperature



I_{LIM} vs Duty Cycle



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PIN FUNCTIONS (DFN/MSOP)

DA1, DA2 (Pins 1, 7/Pins 1, 8): The DA pins are the anode connections for the catch diodes. These are connected internally to the exposed ground pad by current sensing resistors.

BOOST1, BOOST2 (Pins 2, 6/Pins 2, 7): The BOOST pins are used to dynamically boost the power transistor base above V_{IN} to minimize the voltage drop and power loss in the switch. These should be tied to the associated switch pins through the boost capacitors.

SW1, SW2 (Pins 3, 5/Pins 3, 6): The SW pins are the internal power switch outputs. These should be connected to the associated inductors, catch diode cathodes, and the boost capacitors.

V_{IN} (Pin 4/Pins 4, 5): The V_{IN} pins supply power to the internal power switches and control circuitry. In the MSE package the V_{IN} pins must be tied together. The input capacitor should be placed as close as possible to the supply pins.

FB1, FB2 (Pins 14, 8/Pins 16, 9): The FB pins are used to set the regulated output voltage relative to the internal reference. These pins should be connected to a resistor divider from the regulated output such that the FB pin is at 0.8V when the output is at the desired voltage.

RUN/SS1, RUN/SS2 (Pins 13, 9/Pins 15, 10): The RUN/SS pins enable the associated regulator channel. If both pins are pulled to ground, the device will shut-down to a low power state. In the range 0.8V to 2V, the regulators are enabled but the peak switch current and the DA pin maximum current are limited to provide a soft-start function. Above 2V, the full output current is available. The inputs incorporate a 1µA pull-up so that they will float high or charge an external capacitor to provide a current limited soft-start. The pins are pulled down by approximately 250µA in the case of overvoltage or overtemperature conditions in order to discharge the soft-start capacitors. The pins can also be driven by a logic control signal of up to 5.0V. In this case, it is necessary place a 10k to 50k resistor in series along with a capacitor from the RUN/SS pin to ground to ensure that there will be a soft-start for both initial turn on and in the case of fault conditions. Do not tie these pins to V_{IN}.

RT (Pin 10/Pin 11): The RT pin is used to set the internal oscillator frequency. A 40.2k resistor from RT to ground results in a nominal frequency of 1MHz.

SYNC (Pin 11/Pin12): The SYNC pin allows the switching frequency to be synchronized to a external clock. Choose R_T resistor to set a free-run frequency at least 12% less than the external clock frequency for correct operation. The SYNC pin should not be allowed to float; if not used, it should be tied low through a resistance 10kΩ or less.

BD (Pin 12/Pin 13): The BD pin is common anode connection of the internal Schottky boost diodes. This provides the power for charging the BOOST capacitors. It should be locally bypassed for best performance.

Exposed Pad (Pin 15/Pin 17): GND. This is the reference and supply ground for the regulator. The exposed pad must be soldered to the PCB and electrically connected to supply ground. Use a large ground plane and thermal vias to optimize thermal performance. The current in the catch diodes also flows through the GND pad to the DA pins.

AGND (Pin 14, MSOP Package Only): This is the connected to the ground connection of the chip and may be used as a separate return for the low current control side components. It should not be used as the only ground connection or as a connection return for load side components.

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BLOCK DIAGRAM

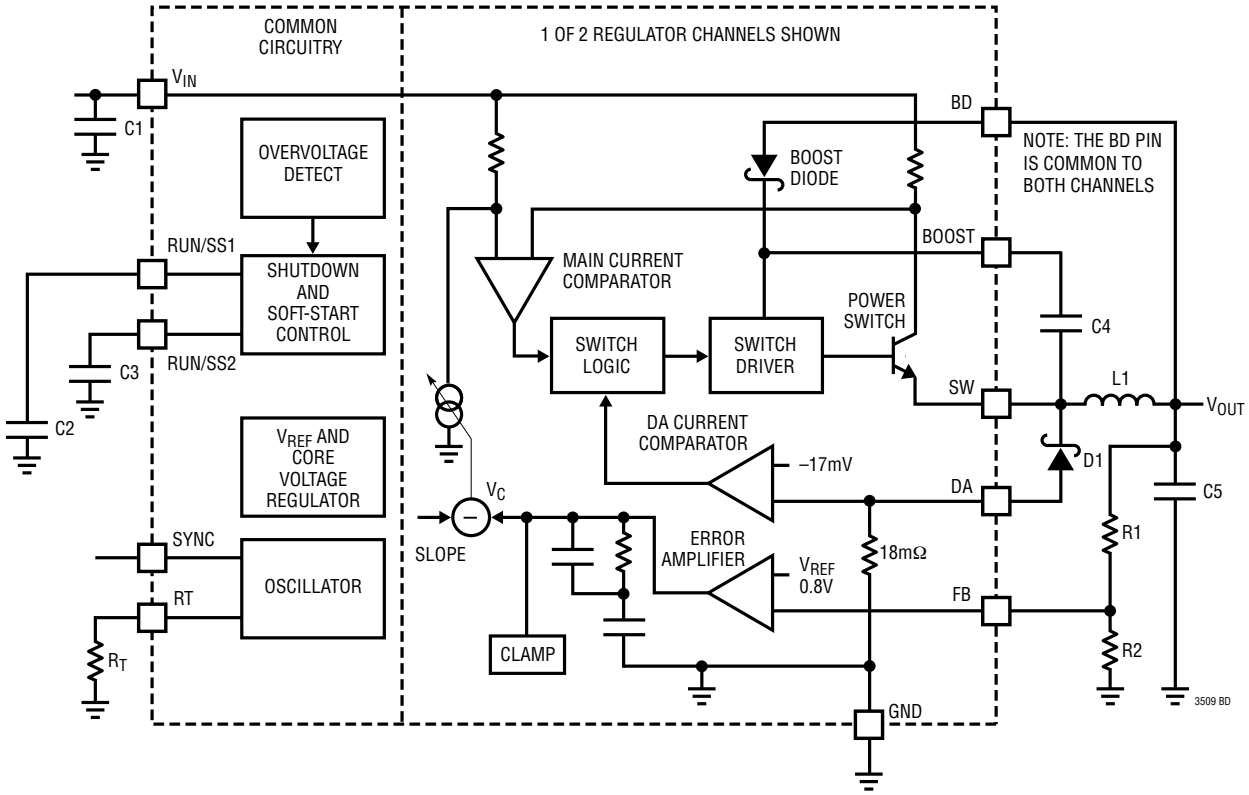

Figure 1. Functional Block Diagram

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OPERATION

Overview

The LT3509 is a dual, constant frequency, current mode switching regulator with internal power switches. The two independent channels share a common voltage reference and oscillator and operate in phase. The switching frequency is set by a single resistor and can also be synchronized to an external clock. Operation can be best understood by referring to the Block Diagram (Figure 1).

Startup and Shutdown

When the RUN/SS[1,2] pins are pulled low (<0.4V) the associated regulator channel is shut down. If both channels are shut down, the common circuitry also enters a low current state. When the RUN/SS pins exceed approximately 0.8V, the common circuitry and the associated regulator are enabled but the output current is limited. From 0.8V up to 2.0V the current limit increases until it reaches the full value. The RUN/SS pins also incorporate a 1μA pull-up to approximately 3V, so the regulator will run if they are left open. A capacitor to ground will cause a current limited soft-start to occur at power-up. In the case of undervoltage, overvoltage or overtemperature conditions the internal circuitry will pull the RUN/SS pins down with a current of approximately 250μA. Thus a new soft-start cycle will occur when the fault condition ends.

Voltage and Current Regulation

The power switches are controlled by a current-mode regulator architecture. The power switch is turned on at the beginning of each clock cycle and turned off by the main current comparator. The inductor current will ramp up while the switch is on until it reaches the peak current threshold. The current at which it turns off is determined by the error amp and the internal compensation network. When the switch turns off, the current in the inductor will cause the SW pin to fall rapidly until the catch diode, D1, conducts. The voltage applied to the inductor will now reverse and the current will linearly fall. The resistor divider, R1 and R2, sets the desired output voltage such that when the voltage at FB reaches 0.8V, the main current comparator threshold will fall and reduce the peak inductor current and hence the average current, until it matches the load current. By making current the controlled variable in the loop, the inductor impedance is effectively removed from the transfer function and the compensation network is simplified. The main current comparator threshold is reduced by the slope compensation signal to eliminate sub-harmonic oscillations at duty cycles >50%.

Current Limiting

Current mode control provides cycle-by-cycle current limiting by means of a clamp on the maximum current that can be provided by the switch. A comparator monitors the current flowing through the catch diode via the DA pin. This comparator delays switching if the diode current is higher than 0.95A (typical). This current level is indicative of a fault condition such as a shorted output with a high input voltage. Switching will only resume once the diode current has fallen below the 0.95A limit. This way the DA comparator regulates the valley current of the inductor to 0.95A during a short circuit. This will ensure the part will survive a short-circuit event.

Over and Undervoltage Shutdown

A basic undervoltage lockout prevents switching if V_{IN} is below 3.3V (typical). The overvoltage shutdown stops the part from switching when V_{IN} is greater than 38.5V (typical). This protects the device and its load during momentary overvoltage events. After the input voltage falls below 38.5V, the part initiates a soft start sequence and resumes switching.

BOOST Circuit

To ensure best efficiency and minimum dropout voltage the output transistor base drive is boosted above V_{IN} by the external boost capacitors (C4). When the SW pin is low the capacitors are charged via the BOOST diodes and the supply on BD.

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APPLICATIONS INFORMATION

Shutdown and Soft Start

When the RUN/SS pins are pulled to ground, the part will shut down to its lowest current state of approximately 9μA. If driving a large capacitive load it may be desirable to use the current limiting soft-start feature. Connecting capacitors to ground from the RUN/SS pins will control the delay until full current is available. The pull-up current is 1μA and the full current threshold is 2V so the start-up time is given by:

$$T = 2 \bullet C \bullet 10^6 \text{ s}$$

For example a 0.005μF capacitor will give a time to full current of 10ms. If both outputs can come up together then the two inputs can be paralleled and tied to one capacitor. In this case use twice the capacitor value to obtain the same start-up time. During the soft-start time both the peak current threshold and the DA current threshold will track so the part will skip pulses as required to limit the maximum inductor current. Starting up into a large capacitor is not much different to starting into a short-circuit in this respect.

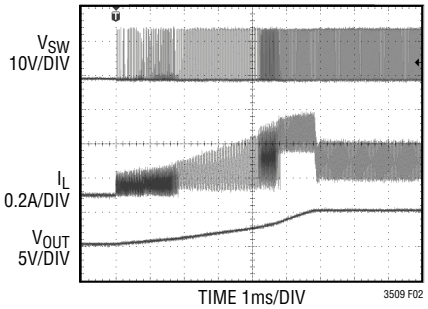

Figure 2. Soft-Start

Setting The Output Voltage

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistors according to:

$$R1 = R2 \bullet \left(\frac{V_{OUT}}{0.8} - 1 \right)$$

The designators correspond to Figure 1. R2 should be 20k or less to avoid bias current errors.

Frequency Setting

The timing resistor, R_T, for any desired frequency in the range 264kHz to 2.2MHz can be calculated from the following formula:

$$R_T = \left(\frac{1.215}{f_{SW}} - 0.215 \right) \bullet 40.2$$

where f_{SW} is in MHz and R_T is in kΩ.

Table 1. Standard E96 Resistors for Common Frequencies

FREQUENCY	TIMING RESISTOR R_T (kΩ)
264 kHz	178
300 kHz	154
400kHz	113
500kHz	88.7
1MHz	40.2
2MHz	15.8
2.2MHz	13.7

Note: The device is specified for operation down to 300kHz. The 264kHz value is to allow external synchronization at 300kHz

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APPLICATIONS INFORMATION

External Synchronization

The external synchronization provides a trigger to the internal oscillator. As such, it can only raise the frequency above the free-run value. To allow for device and component tolerances, the free run frequency should be set to at least 12% lower than the lowest supplied external synchronization reference. The oscillator and hence the switching frequency can then pushed up from 12% above the free-run frequency, set by the selected R_T. For example, if the minimum external clock is 300kHz, the R_T should be chosen for 264kHz.

The SYNC input has a threshold of 1.0V nominal so it is compatible with most logic levels. The duty cycle is not critical provided the high or low pulse width is at least 80ns. If not used, the SYNC input should be tied low with 10kΩ less to avoid noise pickup.

Design Procedure

Before starting detailed design a number of key design parameters should be established as these may affect design decisions and component choices along the way. One of the main things to determine apart from the desired output voltages is the input voltage range. Both the normal operating range and the extreme conditions of surges and/or dips or brown-outs need to be known. Then the operating frequency should be considered and if there are particular requirements to avoid interference. If there are very specific frequencies that need to be avoided then external synchronization may be needed. This could also be desirable if multiple switchers are used as low frequency beating between similar devices can be undesirable. For efficient operation this converter requires a boost supply so that the base of the output transistor can be pumped above the input voltage during the switch on time. Depending on the input and output voltages the boost supply can be provided by the input voltage, one of the regulated outputs or an independent supply such as an LDO.

Input Voltage Range

Firstly, the LT3509 imposes some hard limits due to the undervoltage lock-out and the overvoltage protection. A given application will also have a reduced, normal operating range over which maximum efficiency and lowest ripple are obtained. This usually requires that the device is operating at a fixed frequency without skipping pulses. There may also be zones above and below the normal range where regulation is maintained but efficiency and ripple may be compromised. At the low end, insufficient input voltage will cause loss of regulation and increased ripple—this is the dropout range. At the high end if the duty cycle becomes too low this will cause pulse skipping and excessive ripple. This is the pulse-skip region. Both situations also lead to higher noise at frequencies other than the chosen switching frequency. Occasional excursions into pulse-skip mode, during surges for example, may be tolerable. Pulse skipping will also occur at light loads even within the normal operating range but ripple is usually not degraded because at light load the output capacitor can hold the voltage steady between pulses.

For input voltages greater than 30V, there are restrictions on the inductor value. See the Inductor Selection section for details.

To ensure the regulator is operating in continuous mode it is necessary to calculate the duty cycle for the required output voltage over the full input voltage range. This must then be compared with minimum and maximum practical duty cycles.

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APPLICATIONS INFORMATION

In any step-down switcher the duty cycle when operating in continuous, or fixed frequency, mode is dependent on the step-down ratio. This is because for a constant average load current the decay of the inductor current when the switch is off must match the increase in inductor current when the switch is on. The can be estimated by the following formula:

$$DC = \frac{V_{OUT} + V_F}{V_{IN} - V_{SW} + V_F}$$

where:

DC = Duty Cycle (Fraction of Cycle when Switch is On)

V_{OUT} = Output Voltage

V_{IN} = Input Voltage

V_F = Catch Diode Forward Voltage

V_{SW} = Switch Voltage Drop

Note: This formula neglects switching and inductor losses so in practice the duty cycle may be slightly higher.

It is clear from this equation that the duty cycle will approach 100% as the input voltage is reduced and become smaller as the input voltage increases. There are practical limits to the minimum and maximum duty cycles for continuous operation due to the switch minimum off and on times. These are independent of operating frequency so it is clear that range of usable duty cycle is inverserly proportional to frequency. Therefore at higher frequency the input voltage range (for constant frequency operation) will narrow.

The minimum duty cycle is given by:

$$DC_{MIN} = f_{SW} \bullet t_{ON(MIN)}$$

where:

f_{SW} = Switching Frequency

$t_{ON(MIN)}$ = Switch Minimum On-Time

The minimum on time increases with increasing temperature so the value for the maximum operating temperature should be used. See the Minimum On-Time vs Temperature graph in the Typical Performance Characteristics.

The maximum input voltage for this duty cycle is given by:

$$V_{IN(MAX)} = \frac{V_{OUT} + V_F}{DC_{MIN}} - V_F + V_{SW}$$

Above this voltage the only way the LT3509 can maintain regulation is to skip cycles so the effective frequency will reduce. This will cause an increase in ripple and the switching noise will shift to a lower frequency. This calculation will in practice drive the maximum switching frequency for a desired step-down ratio.

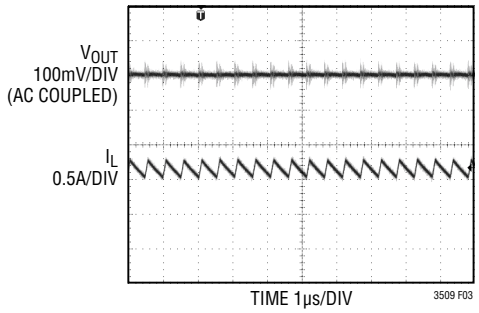

Figure 3. Continuous Mode

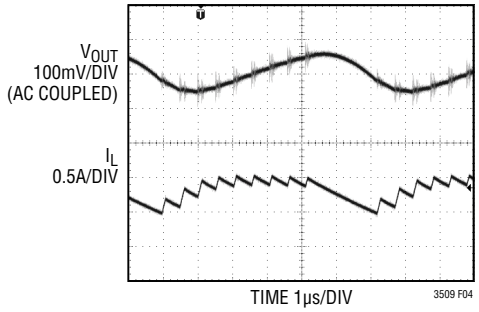

Figure 4. Pulse Skipping

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APPLICATIONS INFORMATION

Minimum Input Voltage and Boost Architecture

The minimum operating voltage is determined either by the LT3509's internal undervoltage lockout of ~3.6V or by its maximum duty cycle. The maximum duty cycle for fixed frequency operation is given by:

$$DC_{MAX} = 1 - t_{OFF(MIN)} \bullet f_{SW}$$

It follows that:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_F}{DC_{MAX}} - V_F + V_{SW}$$

If a reduction in switching frequency can be tolerated the minimum input voltage can drop to just above output voltage. Not only is the output transistor base pumped above the input voltage by the boost capacitor, the switch can remain on through multiple switching cycles resulting in a high effective duty cycle. Thus, this is a true low dropout regulator. As it is necessary to recharge the boost capacitor from time to time, a minimum width off-cycle will be forced occasionally to maintain the charge. Depending on the operating frequency, the duty cycle can reach 97% to 98%, although at this point the output pulses will be at a sub-multiple of the programmed frequency. One other consideration is that at very light loads or no load the part will go into pulse skipping mode. The part will then have trouble getting enough voltage on to the boost capacitors to fully saturate the switch. This is most problematic when the BD pin is supplied from the regulated output. The net result is that a higher input voltage will be required to start up the boost system. The typical minimum input voltage over a range of loads is shown in Figure 5 for 3.3V and Figure 6 for 5V.

When operating at such high duty cycles the peak currents in the boost diodes are greater and this will require a the BD supply to be somewhat higher than would be required at less extreme duty cycles. If operation at low input/output ratios and low BD supply voltages is required it may be desirable to augment the internal boost diodes with external discrete diodes in parallel.

Boost Pin Considerations

The boost capacitor, in conjunction with the internal boost diode, provides a bootstrapped supply for the power switch that is above the input voltage. For operation at 1MHz and above and at reasonable duty cycles a 0.1µF capacitor will work well. For operation at lower frequencies and/or higher duty cycles something larger may be needed. A good rule of thumb is:

$$C_{BOOST} = \frac{1}{10 \bullet f_{SW}}$$

where f_{SW} is in MHz and C_{BOOST} is in µF

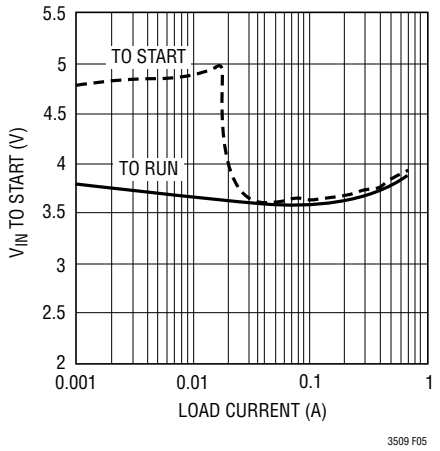

Figure 5. Minimum V_{IN} for 3.3V V_{OUT}

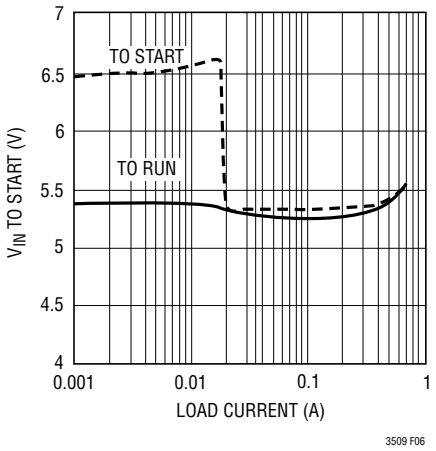

Figure 6. Minimum V_{IN} for 5V V_{OUT}

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APPLICATIONS INFORMATION

Boost Pin Considerations

Figure 7 through Figure 9 show several ways to arrange the boost circuit. The BOOST pin must be more than 2V above the SW pin for full efficiency. For outputs of 3.3V and higher, the standard circuit Figure 7 is best. For lower output voltages, the boost diode can be tied to the input Figure 8. The circuit in Figure 7 is more efficient because the boost pin current comes from a lower voltage source. Finally, as shown in Figure 9, the BD pin can be tied to another source that is at least 3V. For example, if you are generating 3.3V and 1.8V, and the 3.3V is on whenever the 1.8V is on, the 1.8V boost diode can be connected to the 3.3V output.

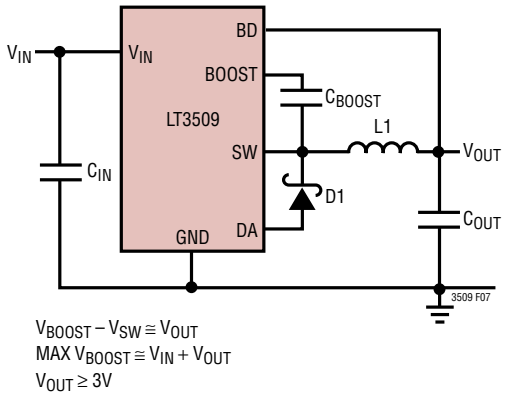

Figure 7. BD Tied to Regulated Output

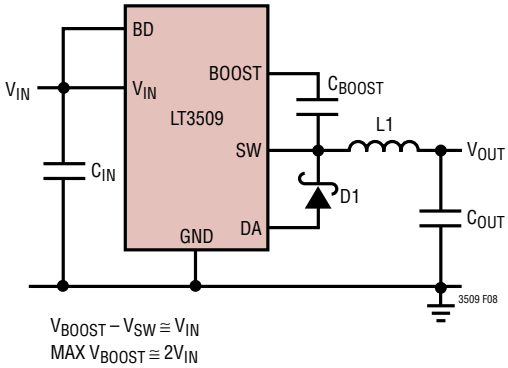

Figure 8. Supplied from V_{IN}

In any case, be sure that the maximum voltage at the BOOST pin is less than 60V and the voltage difference between the BOOST and SW pins is less than 30V.

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = (V_{OUT} + V_F) \bullet \frac{2.1MHz}{f_{SW}}$$

where V_F is the voltage drop of the catch diode (~0.5V) and L is in μH.

The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be at least 30% higher. For highest efficiency, the series resistance (DCR) should be less than 0.15Ω. Table 2 lists several vendors and types that are suitable.

The current in the inductor is a triangle wave with an average value equal to the load current. The peak switch current is equal to the output current plus half the peak-to-peak inductor ripple current. The LT3509 limits its switch current in order to protect itself and the system from overcurrent faults. Therefore, the maximum output current that the LT3509 will deliver depends on the switch current limit, the inductor value and the input and output voltages.

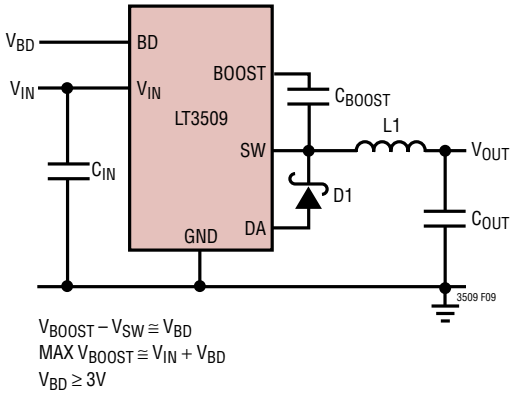

Figure 9. Separate Boost Supply

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APPLICATIONS INFORMATION

When the switch is off, the potential across the inductor is the output voltage plus the catch diode forward voltage. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = (1-DC)\frac{V_{OUT}+V_F}{L \bullet f_{SW}}$$

where:

DC = Duty Cycle

f_{SW} = Switching Frequency

L = Inductor Value

V_F = Diode Forward Voltage

The peak inductor and switch current is:

$$I_{SWPK} = I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2}$$

To maintain output regulation, this peak current must be less than the LT3509's switch current limit I_{LIM}. This is dependent on duty cycle due to the slope compensation. For I_{LIM} is at least 1.4A at low duty cycles and decreases linearly to 1.0A at DC = 0.8.

The theoretical minimum inductance can now be calculated as:

$$L_{MIN} = \frac{1-DC_{MIN}}{f} \bullet \frac{V_{OUT}+V_F}{I_{LIM}-I_{OUT}}$$

where DC_{MIN} is the minimum duty cycle called for by the application i.e.:

$$DC_{MIN} = \frac{V_{OUT(MAX)}+V_F}{V_{IN(MIN)}-V_{SW}+V_F}$$

There is a limit to the actual minimum duty cycle imposed by the minimum on-time of the switch. For a robust design it is important that inductor that will not saturate when the switch is at its minimum on-time, the input voltage is at maximum and the output is short circuited. In this case the full input voltage, less the drop in the switch, will appear across the inductor. This doesn't require an actual short, just starting into a capacitive load will provide the same conditions. The Diode current sensing scheme will ensure that the switch will not turn-on if the inductor current is above the DA current limit threshold, which has a maximum of 1.1A. The peak current under short-circuit conditions can then be calculated from:

$$I_{PEAK} = \frac{V_{IN} \bullet t_{ON(MIN)}}{L} + 1.1A$$

The inductor should have a saturation current greater than this value. For safe operation with high input voltages this can often mean using a physically larger inductor as higher value inductors often have lower saturation currents for a given core size. As a general rule the saturation current should be at least 1.8A to be short-circuit proof. However, it's generally better to use an inductor larger than the minimum value. For robust operation at input voltages greater than 30V, use an inductor with a value of 4.2µH or greater, and a saturation current rating of 1.8A or higher. The minimum inductor has large ripple currents which increase core losses and require large output capacitors to keep output voltage ripple low. Select an inductor greater than L_{MIN} that keeps the ripple current below 30% of I_{LIM}.

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APPLICATIONS INFORMATION

Table 2. Recommended Inductors

MANUFACTURER/ PART NUMBER	VALUE (µH)	I_{SAT} (A)	DCR (Ω)	HEIGHT (mm)
Coilcraft				
LPS4018-222ML	2.2	2.8	0.07	1.7
LPS5030-332ML	3.3	2.5	0.066	2.9
LPS5030-472ML	4.7	2.5	0.083	2.9
LPS6225-682ML	6.8	2.7	0.095	2.4
LPS6225-103ML	10	2.1	0.105	2.4
Sumida				
CDRH4D22/HP-2R2N	2.2	3.2	0.0035	2.4
CDRH4D22/HP-3R5N	3.5	2.5	0.052	2.4
CDRH4D22/HP-4R7N	4.7	2.2	0.066	2.4
CDRH5D28/HP-6R8N	6.8	3.1	0.049	3.0
CDRH5D28/HP-8R2N	8.2	2.7	0.071	3.0
CDRH5D28R/HP-100N	10	2.45	0.074	3.0
Cooper				
SD52-2R2-R	2.2	2.30	0.0385	2.0
SD52-3R5-R	3.5	1.82	0.0503	2.0
SD52-4R7-R	4.7	1.64	0.0568	2.0
SD6030-5R8-R	5.8	1.8	0.045	3.0
SD7030-8R0-R	8.0	1.85	0.058	3.0
SD7030-100-R	10.0	1.7	0.065	3.0
Toko				
A997AS-2R2N	2.2	1.6	0.06	1.8
A997AS-3R3N	3.3	1.2	0.07	1.8
A997AS-4R7M	4.7	1.07	0.1	1.8
Würth				
7447745022	2.2	3.5	0.036	2.0
7447745033	3.3	3.0	0.045	2.0
7447745047	4.7	2.4	0.057	2.0
7447745076	7.6	1.8	0.095	2.0
7447445100	10	1.6	0.12	2.0

The prior analysis is valid for continuous mode operation ($I_{OUT} > \Delta I_{LIM} / 2$). For details of maximum output current in discontinuous mode operation, see Linear Technology's Application Note 44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid subharmonic oscillations. This minimum inductance is

$$L_{MIN} = (V_{OUT} + V_F) \bullet \frac{1.4}{f_{SW}}$$

where f_{SW} is in MHz and L_{MIN} is in µH.

If using external synchronization, calculate L_{MIN} using the R_T frequency and not the SYNC frequency.

Frequency Compensation

The LT3509 uses current mode control to regulate the output, which simplifies loop compensation and allows the necessary filter components to be integrated. The fixed internal compensation network has been chosen to give stable operation over a wide range of operating conditions but assumes a minimum load capacitance. The LT3509 does not depend on the ESR of the output capacitor for stability so the designer is free to use ceramic capacitors to achieve low output ripple and small PCB footprint.

Figure 10 shows an equivalent circuit for the LT3509 control loop. The error amp is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switch and inductor is modeled as a transconductance amplifier generating an output current proportional to the voltage at the COMP-NODE. The gain of the power stage (gmp) is 1.1S. Note that the output capacitor integrates this current and that the internal capacitor integrates the error amplifier output current, resulting in two poles in the loop. In most cases, a zero is required and comes either from the output capacitor ESR

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APPLICATIONS INFORMATION

or from R_C. This model works well as long as the inductor current ripple is not too low ($\Delta I_{RIPPLE} > 5\%\ I_{OUT}$) and the loop crossover frequency is less than $f_{SW}/5$. An optional phase lead capacitor (CPL) across the feedback divider may improve the transient response.

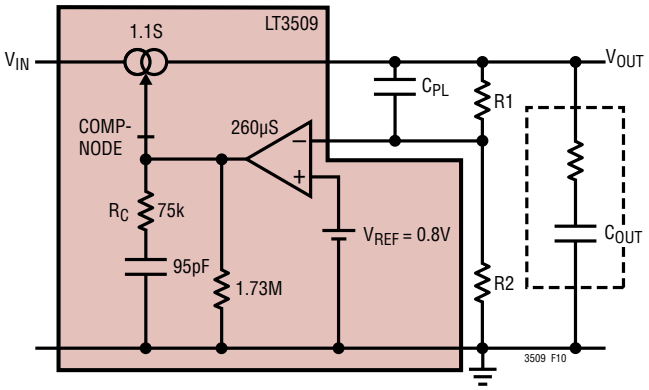

Figure 10. Small-Signal Equivalent Circuit

Output Capacitor Selection

The output capacitor filters the inductor current to generate an output with low voltage ripple. It also stores energy in order to satisfy transient loads and stabilize the LT3509's control loop. Because the LT3509 operates at a high frequency, minimal output capacitance is necessary. In addition, the control loop operates well with or without the presence of output capacitor series resistance (ESR). Ceramic capacitors, which achieve very low output ripple and small circuit size, are therefore an option.

You can estimate output ripple with the following equations.

For ceramic capacitors where low capacitance value is more significant than ESR:

$$V_{RIPPLE} = \Delta I_L / (8 \bullet f_{SW} \bullet C_{OUT})$$

For electrolytic capacitors where ESR is high relative to capacitive reactance:

$$V_{RIPPLE} = \Delta I_L \bullet ESR$$

where ΔI_L is the peak-to-peak ripple current in the inductor. The RMS content of this ripple is very low so the RMS current rating of the output capacitor is usually not of concern. It can be estimated with the formula:

$$I_{C(RMS)} = \Delta I_L / \sqrt{12}$$

Another constraint on the output capacitor is that it must have greater energy storage than the inductor; if the stored energy in the inductor transfers to the output, the resulting voltage step should be small compared to the regulation voltage. For a 5% overshoot, this requirement indicates:

$$C_{OUT} > 10 \bullet L \bullet (I_{LIM} / V_{OUT})^2$$

The low ESR and small size of ceramic capacitors make them the preferred type for LT3509 applications. Not all ceramic capacitors are the same, however. Many of the higher value capacitors use poor dielectrics with high temperature and voltage coefficients. In particular, Y5V

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APPLICATIONS INFORMATION

and Z5U types lose a large fraction of their capacitance with applied voltage and at temperature extremes. Because loop stability and transient response depend on the value of C_{OUT}, this loss may be unacceptable. Use X7R and X5R types.

The value of the output capacitor greatly affects the transient response to a load step. It has to supply extra current demand or absorb excess current delivery until the feedback loop can respond. The loop response is dependent on the error amplifier transconductance, the internal compensation capacitor and the feedback network. Higher output voltages necessarily require a larger feedback divider ratio. This will also reduce the loop gain and slow the response time. Fortunately this effect can be mitigated by use of a feed-forward capacitor, C_{PL}, across the top feedback resistor. The small-signal model shown in Figure 10 can be used to model this in a simulator or to give insight to an empirical design. Figure 11 shows some load step responses with differing output capacitors and C_{PL} combinations.

Input Capacitor

The input capacitor needs to supply the pulses of charge demanded during the on time of the switches. Little total capacitance is required as a few hundred millivolts of ripple at the V_{IN} pin will not cause any problems to the device. When operating at 2MHz and 12V, 2µF will work well. At the lowest operating frequency and/or at low input voltages a larger capacitor such as 4.7µF is preferred.

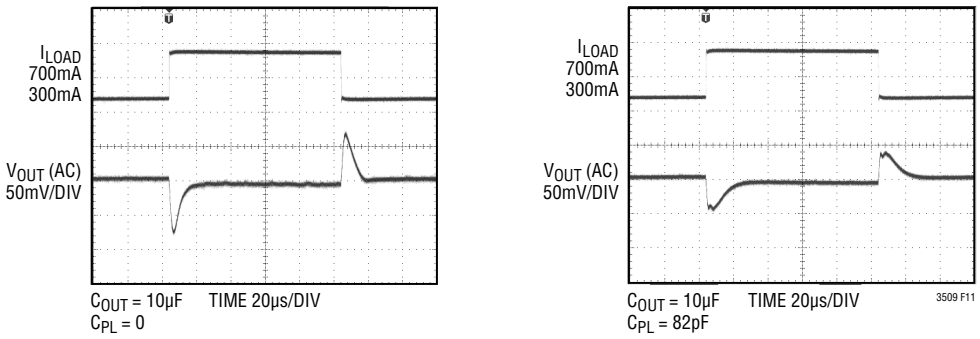

Figure 11. Transient Load Response with Different Combinations of C_{OUT} and C_{PL} Load Current Step from 300mA to 700mA R1 = 10k, R2 = 32.4k, V_{IN} = 12V, V_{OUT} = 3.3V, f_{SW} = 2.0MHz

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APPLICATIONS INFORMATION

Diode Selection

The catch diode (D1 from Figure 1) conducts current only during switch off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = I_{OUT}(V_{IN} - V_{OUT}) / V_{IN}$$

The only reason to consider a diode with a larger current rating than necessary for nominal operation is for the worst-case condition of shorted output. The diode current will then increase to the typical peak switch current limit. If transient input voltages exceed 40V, use a Schottky diode with a reverse voltage rating of 45V or higher. If the maximum transient input voltage is under 40V, use a Schottky diode with a reverse voltage rating greater than the maximum input voltage. Table 3 lists several Schottky diodes and their manufacturers:

Table 3. Schottky Diodes

MANUFACTURER/ PART NUMBER	V_R (V)	I_{AVE} (A)	V_F at 1A (mV)
On Semiconductor			
MBRM140	40	1	550
MicroSemi			
UPS140	40	1	450
Diodes Inc.			
DFLS140L	40	1	550
1N5819HW	40	1	450

Short and Reverse Protection

Provided the inductors are chosen to not go deep into their saturation region at the maximum I_{LIMIT} current the LT3509 will tolerate a short circuit on one or both outputs. The excess current in the inductor will be detected by the DA comparator and the frequency will reduced until the valley current is below the limit. This shouldn't affect the other channel unless the channel that is shorted is also providing the boost supply to the BD pin. In this case the voltage drop of the other switch will increase and lower the efficiency. This could eventually cause the part to reach the thermal shutdown limit. One other important feature of the part that needs to be considered is that there is a parasitic diode in parallel with the power switch. In normal operation this is reverse biased but it could conduct if the load can be powered from an alternate source when the LT3509 has no input. This may occur in battery charging applications or in battery backup systems where a battery or some other supply is diode ORed with one of the LT3509 regulated outputs. If the SW pin is at more than about 4V the V_{IN} pin can attain sufficient voltage for LT3509 control circuitry to power-up to the quiescent bias level and up to 2mA could be drawn from the backup supply. This can be minimized if some discrete FETs or open-drain buffers are used to pull down the RUN/SS pins. Of course the gates need to be driven from the standby or battery backed supply. If there is the possibility of a short circuit at the input or just other parallel circuits connected to V_{IN} it would be best to add a protection diode in series with V_{IN}. This will also protect against a reversed input polarity. These concepts are illustrated in Figure 12.

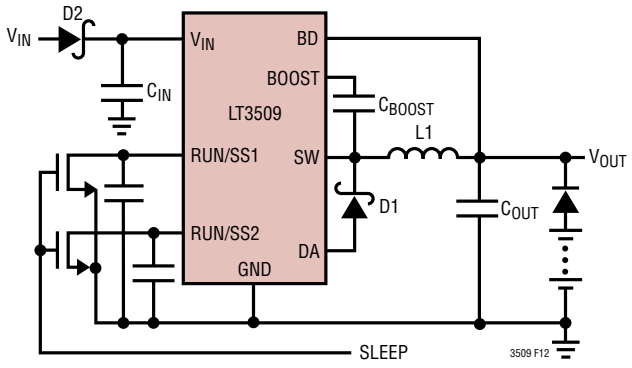

Figure 12. Reverse Bias Protection

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APPLICATIONS INFORMATION

Hot Plugging Considerations

The small size, reliability and low impedance of ceramic capacitors make them attractive for the input capacitor. Unfortunately they can be hazardous to semiconductor devices if combined with an inductive supply loop and a fast power transition such as through a mechanical switch or connector. The low loss ceramic capacitor combined with the just a small amount of wiring inductance forms an underdamped resonant tank circuit and the voltage at the V_{IN} pin of the LT3509 can ring to twice the nominal input voltage. See Linear Technology Application Note 88 for more details.

PCB Layout and Thermal Design

The PCB layout is critical to both the electrical and thermal performance of the LT3509. Most important is the connection to the Exposed Pad which provides the main ground connection and also a thermal path for cooling the chip. This must be soldered to a topside copper plane which is also tied to backside and/or internal plane(s) with an array of thermal vias.

To obtain the best electrical performance particular attention should be paid to keeping the following current paths short:

- The loop from the V_{IN} pin through the input capacitor back to the ground pad and plane. This sees high di/dt transitions as the power switches turn on and off. Excess impedance will degrade the minimum usable input voltage and could cause crosstalk between channels.
- The loops from the switch pins to the catch diodes and back to the DA pins. The fast changing currents and voltage here combined with long PCB traces will cause ringing on the switch pin and may result in unwelcome EMI.
- The loop from the regulated outputs through the output capacitor back to the ground plane. Excess impedance here will result in excessive ripple at the output.

The area of the SW and BOOST nodes should as small as possible. Also the feedback components should be placed as close as possible to the FB pins so that the traces are short and shielded from the SW and BOOST nodes by the ground planes.

Figure 13 shows a detail view of a practical board layout showing just the top layer. The complete board is somewhat larger at 7.5cm × 7.5cm. The device has been evaluated on this board in still air running at 700kHz switching frequency. One channel was set to 5V and the other to 3.3V and both channels were fully loaded to 700mA. The device temperature reached approximately 15°C above ambient for input voltages below 12V. At 24V input it was slightly higher at 17°C above ambient.

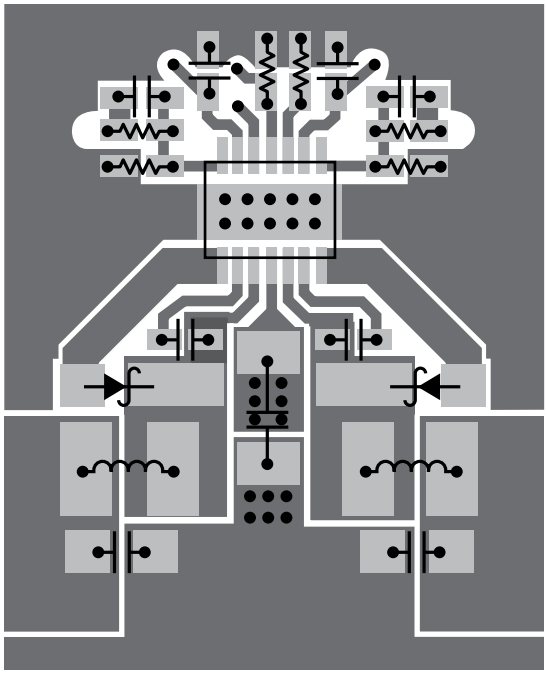

Figure 13. Sample PCB Layout (Top Layer Only)

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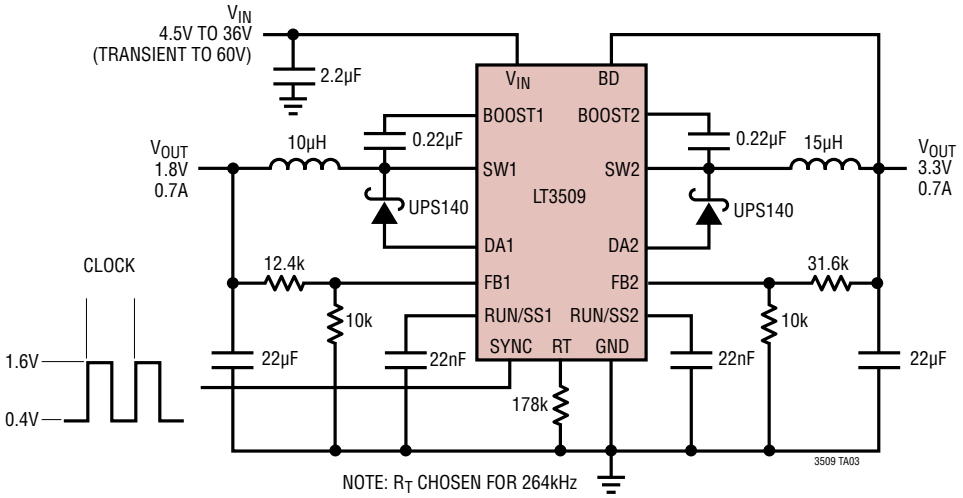
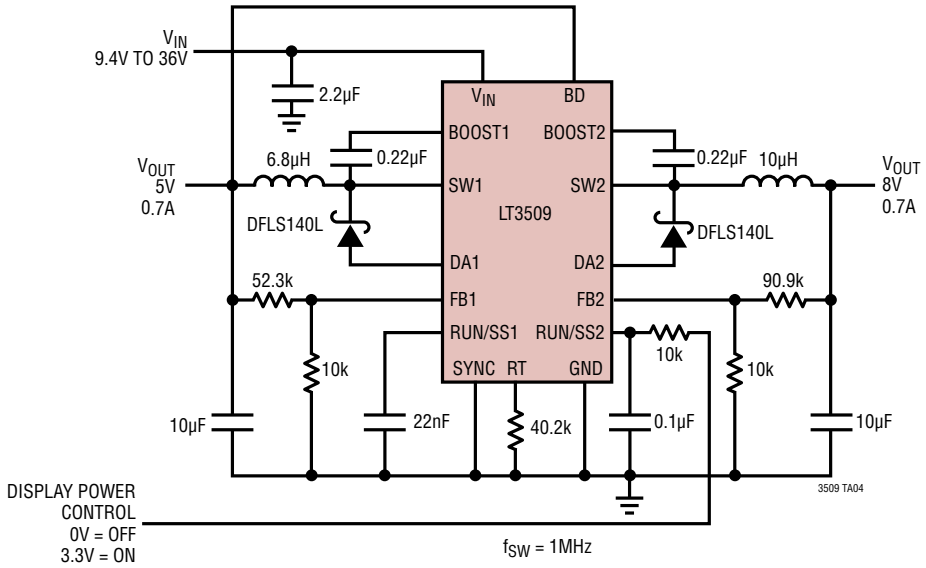
TYPICAL APPLICATIONS

1.8V and 3.3V Outputs, Synchronized to 300kHz to 600kHz



Automotive Accessory Application
5V Logic Supply and 8V for LCD Display with Display Power Controlled by Logic



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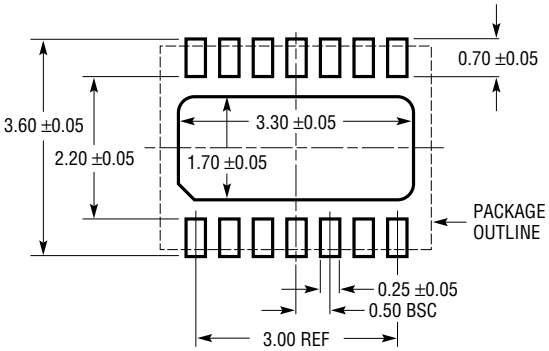
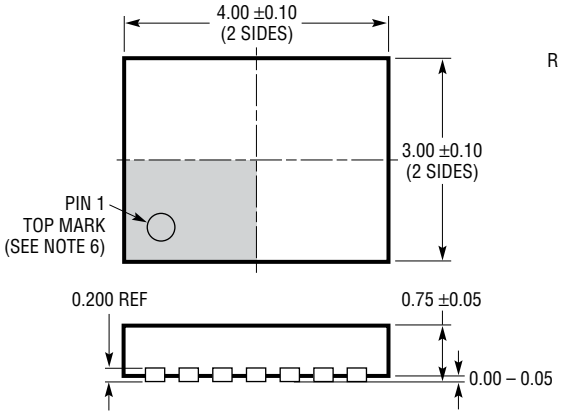
PACKAGE DESCRIPTION

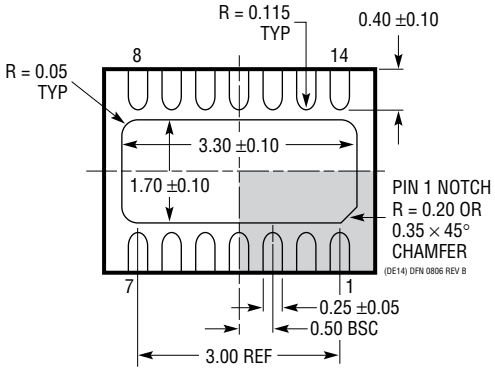
Please refer to http://www.linear.com/product/LT3509#packaging for the most recent package drawings.

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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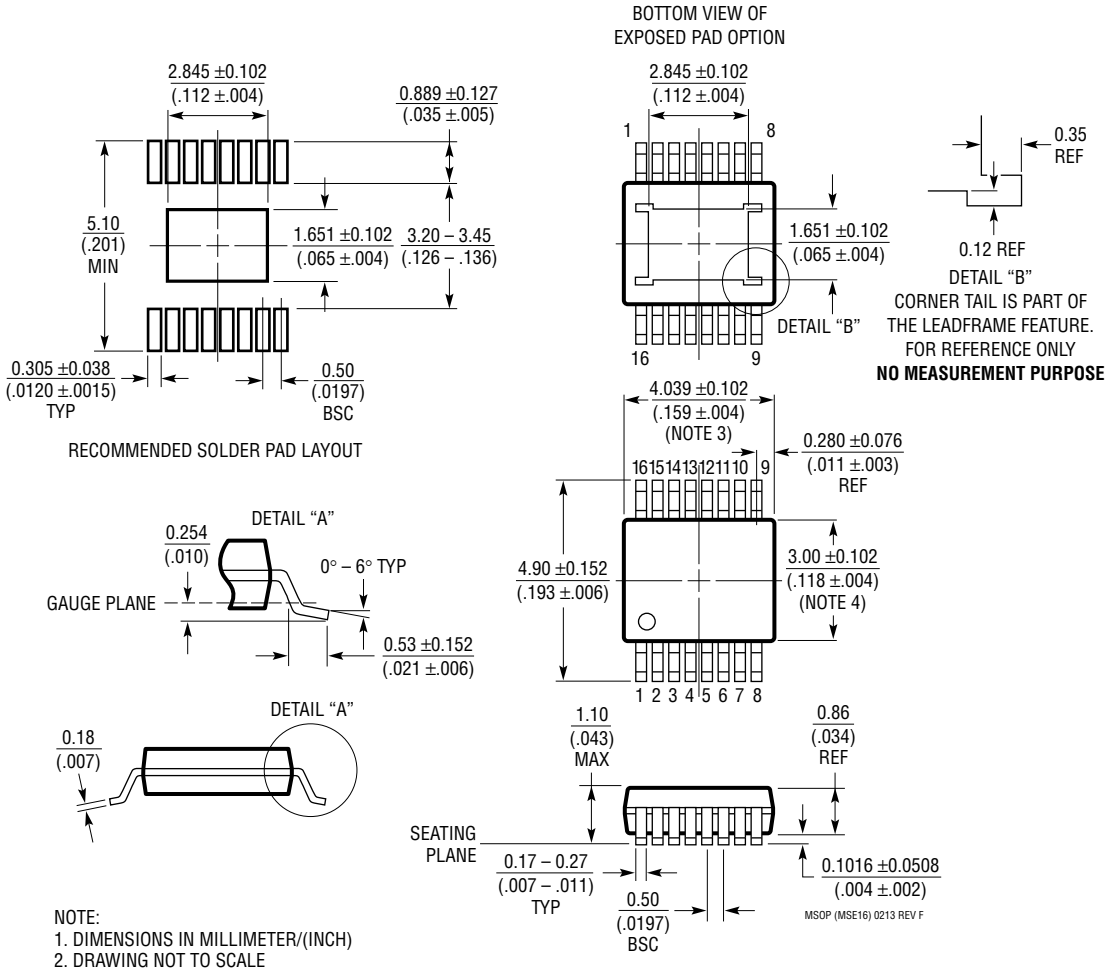
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LT3509#packaging for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

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REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	4/10	Changed Pin Name to RT	1, 2, 6, 7, 20, 21, 24
		Revised Absolute Maximum Ratings	2
		Updated Notes and Change/Add Values in Electrical Characteristics	3
		Revised Values in Typical Performance Characteristics	5
		Revised Values in Pin Functions	6
		Revised Values in Startup and Shutdown Section	8
		Revised Values in Shutdown and Soft-Start, Frequency Setting Sections, and Table 1	9
D	01/16	Clarified Sync Pin Function Description	6
		Clarified External Synchronization Applications Information	10

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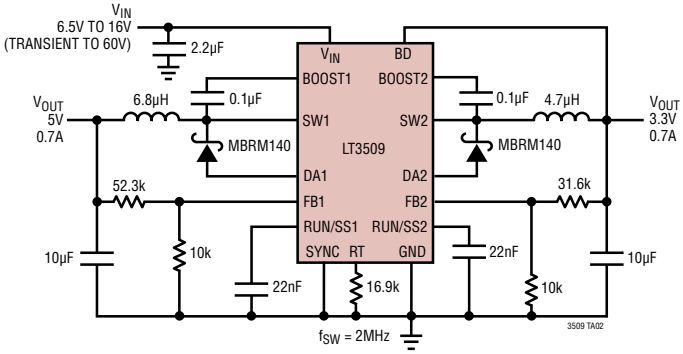
TYPICAL APPLICATIONS

2MHz, 5V and 3.3V Outputs



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1766	60V, 1.2A (I_{OUT}), 200kHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 5.5V to 60V, V_{OUT} = 1.20V, I_Q = 2.5mA, I_{SD} < 25µA, TSSOP16/E Package
LT1936	36V, 1.4A (I_{OUT}) , 500kHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 36V to 36V, V_{OUT} = 1.20V, I_Q = 1.9mA, I_{SD} < 1µA, MS8E Package
LT1939	25V, 2A, 2.5MHz High Efficiency DC/DC Converter and LDO Controller	V_{IN}: 3.6V to 25V, V_{OUT} = 0.8V, I_Q = 2.5µA, I_{SD} < 10µA, 3mm × 3mm DFN-10
LT1976/ LT1977	60V, 1.2A (I_{OUT}), 200/500kHz, High Efficiency Step-Down DC/DC Converter with Burst Mode® Operation	V_{IN}: 3.3V to 60V, V_{OUT} = 1.20V, I_Q = 100µA, I_{SD} < 1µA, TSSOP16E Package
LT3434/ LT3435	60V, 2.4A (I_{OUT}), 200/500kHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.3V to 60V, V_{OUT} = 1.20V, I_Q = 100µA, I_{SD} < 1µA, TSSOP16E Package
LT3437	60V, 400mA (I_{OUT}), MicroPower Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.3V to 60V, V_{OUT} = 1.25V, I_Q = 100µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, TSSOP-16E Package
LT3480	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.6V to 38V, V_{OUT} = 0.78V, I_Q = 70µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E Package
LT3481	34V with Transient Protection to 36V, 2A (I_{OUT}), 2.8MHz, High Efficiency Step-Down DC/DC Converter with Burst Mode Operation	V_{IN}: 3.6V to 34V, V_{OUT} = 1.26V, I_Q = 50µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E Package
LT3493	36V, 1.4A(I_{OUT}), 750kHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 36V to 36V, V_{OUT} = 0.8V, I_Q = 1.9mA, I_{SD} < 1µA, 2mm × 3mm DFN-6 Package
LT3500	36V, 40Vmax, 2A, 2.5MHz High Efficiency DC/DC Converter and LDO Controller	V_{IN}: 3.6V to 36V, V_{OUT} = 0.8V, I_Q = 2.5mA, I_{SD} < 10µA, 3mm × 3mm DFN-10
LT3501	25V, Dual 3A (I_{OUT}), 1.5MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.3V to 25V, V_{OUT} = 0.8V, I_Q = 3.7mA, I_{SD} = 10µA, TSSOP-20E Package
LT3505	36V with Transient Protection to 40V, 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 34V, V_{OUT} = 0.78V, I_Q = 2mA, I_{SD} < 2µA, 3mm × 3mm DFN-8, MSOP-8E Package
LT3506/ LT3506A	25V, Dual 1.6A (I_{OUT}), 575kHz,/1.1MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 25V, V_{OUT} = 0.8V, I_Q = 3.8mA, I_{SD} = 30µA, 5mm × 4mm DFN-16 TSSOP-16E Package
LT3507	36V 2.5MHz, Triple (2.4A + 1.5A + 1.5A (I_{OUT})) with LDO Controller High Efficiency Step-Down DC/DC Converter	V_{IN}: 4V to 36V, V_{OUT} = 0.8V, I_Q = 7mA, I_{SD} = 1µA, 5mm × 7mm QFN-38
LT3508	36V with Transient Protection to 40V, Dual 1.4A (I_{OUT}), 3MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.7V to 37V, V_{OUT} = 0.8V, I_Q = 4.6mA, I_{SD} = 1µA, 4mm × 4mm QFN-24, TSSOP-16E Package
LT3510	25V, Dual 2A (I_{OUT}), 1.5MHz High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.3V to 25V, V_{OUT} = 0.8V, I_Q = 3.7mA, I_{SD} = 10µA, TSSOP-20E Package
LT3684	34V with Transient Protection to 36V, 2A (I_{OUT}), 2.8MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 34V, V_{OUT} = 1.26V, I_Q = 850µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E Package
LT3685	36V with Transient Protection to 60V, 2A (I_{OUT}), 2.4MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3.6V to 38V, V_{OUT} = 0.78V, I_Q = 70µA, I_{SD} < 1µA, 3mm × 3mm DFN-10, MSOP-10E Package

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