COMPLIES WITH FOLLOWING STANDARDS

	Peak surge voltage (V)	Voltage waveform (µs)	Required peak current (A)	Current waveform (µs)	Minimum serial resistor to meet standard (Ω)
ITU-T K20	4000 1000	10/700 10/700	100 25	5/310 5/310	50 0
ITU-T K21	4000 1500	10/700 10/700	100 37.5	5/310 5/310	50 0
VDE0433	2000	10/700	50	5/310	5
VDE0878	2000	1.2/50	50	1/20	0
IEC61000-4-5	level 3 level 4	10/700 1.2/50	50 100	5/310 8/20	5 25
FCC Part 68 lightning surge type A	1500 800	10/160 10/560	200 100	10/160 10/560	20 15
FCC Part 68 lightning surge type B	1000	9/720	25	5/320	0
BELLCORE GR-1089-CORE First level	2500 1000	2/10 10/1000	500 100	2/10 10/1000	20 25
BELLCORE GR-1089-CORE Second level	5000	2/10	500	2/10	40
BELLCORE GR-1089-CORE Intrabuilding	800 1500	2/10 2/10	100 100	2/10 2/10	0 0

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C)

Symbol	Parameter		Value	Unit
I_{PP}	Peak pulse current	10/1000µs 5/310µs 1/20µs	30 45 65	A
I_{TSM}	Non repetitive surge peak on-state current (F = 50Hz)	t_p = 0.2 s t_p = 1s t_p = 15 min	5.5 4.2 1.5	A
V_{GN} max V_{GP} max ΔV_{bat} max	Maximum negative battery voltage range Maximum positive battery voltage range Total battery supply voltage	See fig.1	-110 to 0 0 to +95 190	V
T_{op}	Operating temperature range (see note 1)		-20 to +85	°C
T_{stg}	Storage temperature range		- 55 to + 150	°C
T_L	Lead solder temperature (10s duration)		260	°C

Note 1: Within the Top range, the LCP02-150B1 keeps on operating. The impacts of the ambient temperature are given by derating curves.

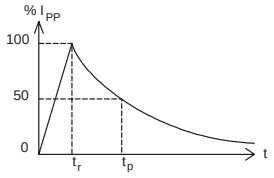
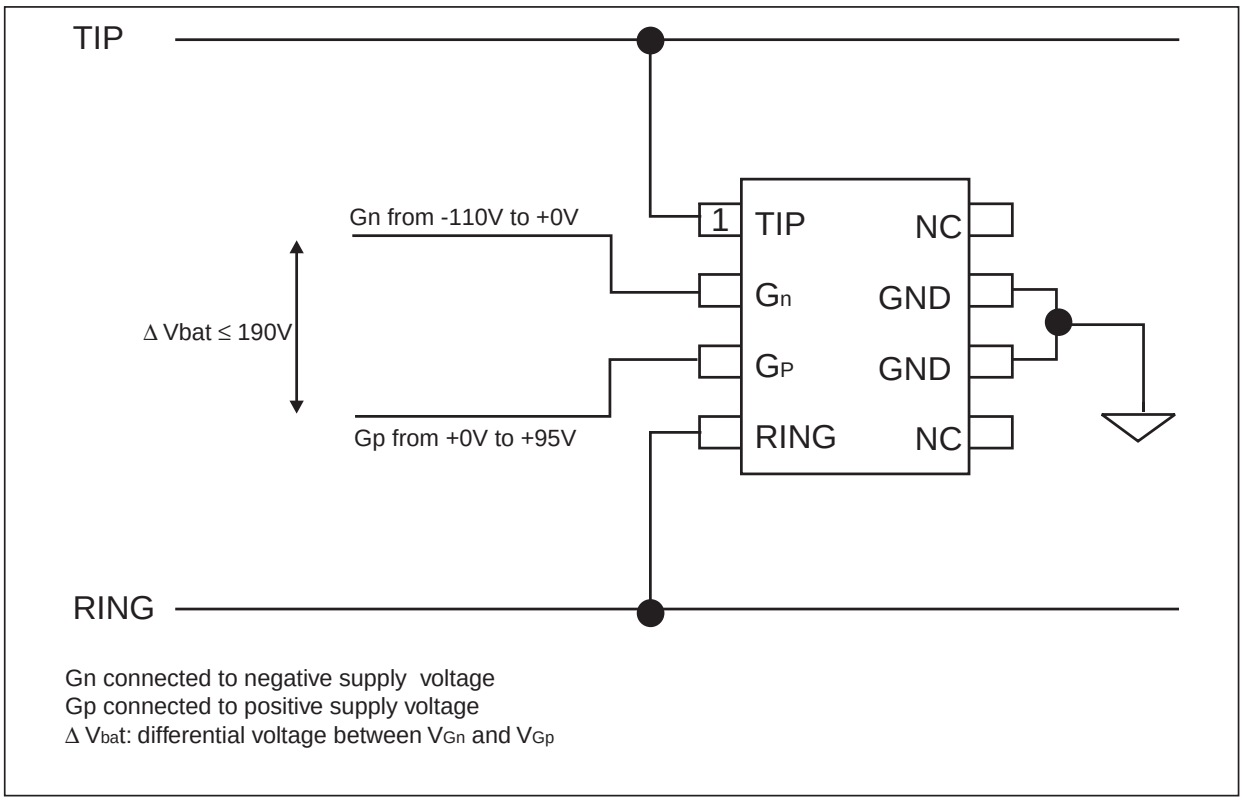


Fig. 1: Test circuit



Gn connected to negative supply voltage
Gp connected to positive supply voltage
ΔV_{bat}: differential voltage between V_{Gn} and V_{Gp}

THERMAL RESISTANCE

Symbol	Parameter	Value	Unit
$R_{th\ (j-a)}$	Junction to ambient	150	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C)

1 - PARAMETERS RELATED TO THE NEGATIVE SUPPRESSOR

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{Gn}	Negative gate trigger current	$V_{Gn/GND}$ = -60V Measured at 50Hz		5	mA
I_{H-}	Holding current (see fig.2)	Go-No Go test, V_{Gn} = -60V	150		mA
I_{RGL-}	Reverse leakage current Gn/Line	Tj = 25°C, $V_{Gn/line}$ = -190V		5	µA
V_{DGL-}	Dynamic switching voltage Gn / Line (see note 2)	$V_{Gn/GND}$ = -60V 10/1000µs 1kV R_P = 25Ω I_{PP} = 30A 10/700µs 2kV R_P = 25Ω I_{PP} = 30A 1.2/50µs 2kV R_P = 25Ω I_{PP} = 30A		18 8 15	V

2 - PARAMETERS RELATED TO THE POSITIVE SUPPRESSOR

Symbol	Parameter	Test conditions	Min.	Max.	Unit
I_{Gp}	Positive gate trigger current	$V_{Gp/GND}$ = 60V Measured at 50Hz		5	mA
I_{RGL+}	Reverse leakage current Gp/LINE	Tj = 25°C, $V_{Gp/line}$ = +190V		5	µA
V_{DGL+}	Dynamic switching voltage Gp / Line (see note 2)	$V_{Gp/GND}$ = +60V 10/1000µs 1kV R_P = 25Ω I_{PP} = 30A 10/700µs 2kV R_P = 25Ω I_{PP} = 30A 1.2/50µs 2kV R_P = 25Ω I_{PP} = 30A		18 8 35	V

3 - PARAMETERS RELATED TO LINE/GND

Symbol	Parameter	Test conditions	Typ.	Max.	Unit
I_R	Reverse leakage current	Tj = 25°C, V_{LINE} = +90V, $V_{GP/LINE}$ = +1V Tj = 25°C, V_{LINE} = -105V, $V_{GN/LINE}$ = -1V		5 5	µA
C_{off}	Capacitance LINE/GND	V_R = -3V, F =1MHz, V_{Gp} = 60V, V_{Gn} = -60V	60		pF

Note 2: The V_{DGL} value is the difference between the peak line voltage during the surge and the programmed gate voltage.

Fig. 2: Relative variation of holding current versus junction temperature.

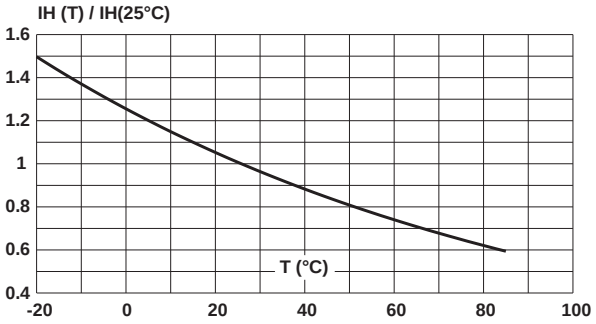


Fig. 3: Maximum non repetitive surge peak on state current versus overload duration (with 50Hz sinusoidal wave and initial junction temperature equal to +25°C).

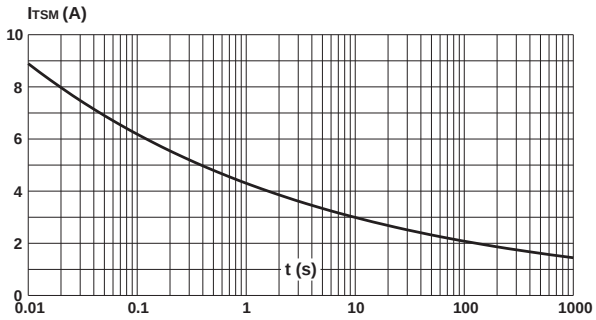
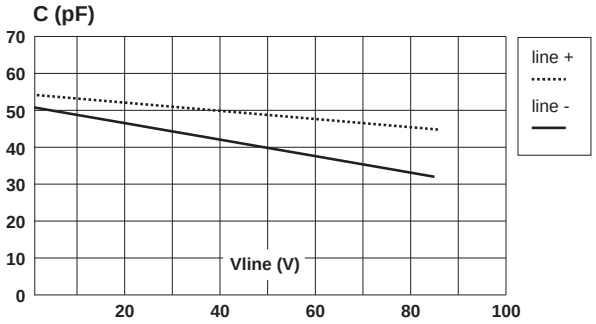


Fig. 4: Capacitance versus reverse applied voltage (typical values) with V_{GN} = -90V and V_{GP} = +90V.



TECHNICAL INFORMATION

Fig. 5: LCP02 concept behavior.

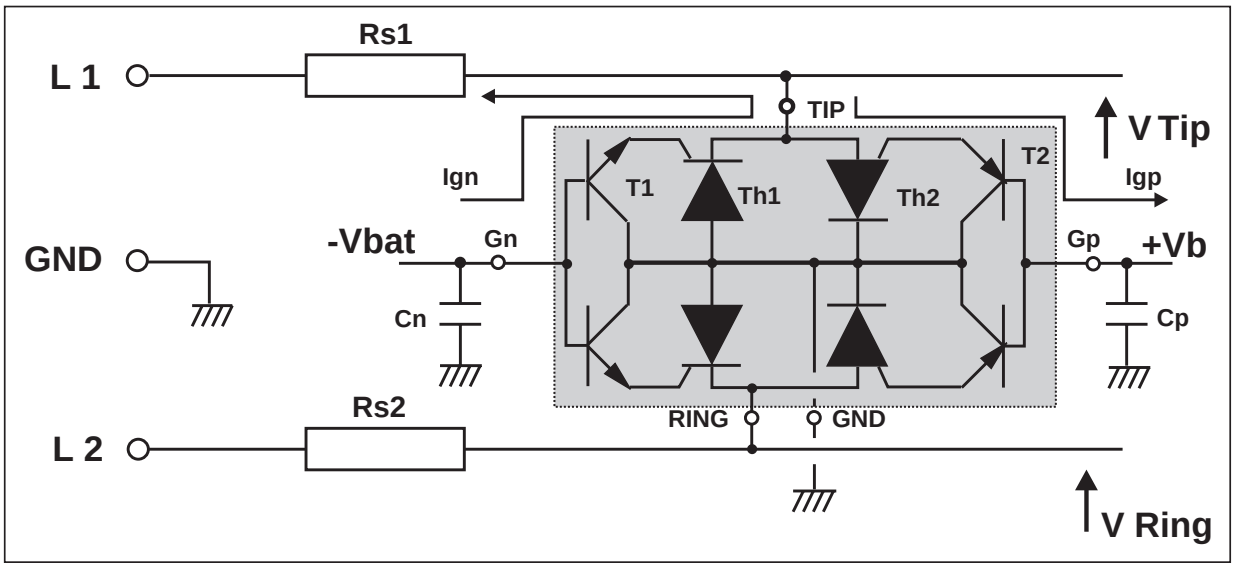


Figure 5 shows the classical protection circuit using the LCP02 crowbar concept. This topology has been developped to protect the new two-battery voltage SLICs. It allows both positive and negative firing thresholds to be programmed. The LCP02-150B1 has two gates (Gn and Gp). Gn is biased to negative battery voltage -Vbat, while Gp is biased to the positive battery voltage +Vb.

When a negative surge occurs on one wire (L1 for example), a current Ign flows through the base of the transistor T1 and then injects a current in the gate of the thyristor Th1 which fires. All the surge current flows through the ground. After the surge, when the current flowing through Th1 becomes less negative than the negative holding current Ih-, Th1 switches off. This holding current I_{H-} is temperature dependant as per figure2.

When a positive surge occurs on one wire (L1 for example), a current Igp flows through the base of the transistor T2 and then injects a current in the gate of the thyristor Th2 which fires. All the surge current flows through the ground. After the surge, when the current flowing through Th2 becomes less positive than the positive holding current Ih+, Th2 switches off. This holding current I_{H+}, typically 20mA at 25°C, is temperature dependant and the same figure 2 also applies.

The capacitors Cn and Cp are used to speed up the crowbar structure firing during the fast rise or fall edges. This allows to minimize the dynamical breakover voltage at the SLIC Tip and Ring inputs during fast surges. Please note that these capacitors are generally available around the SLIC. To be efficient they have to be as close as possible to the LCP02-150B1 gate pins (Gn and Gp) and to the reference ground track (or plan). The optimized value for Cn and Cp is 220nF.

The series resistors Rs1 and Rs2 designed in figure 5 represent the fuse resistors or the PTCs which are needed to withstand the power contact or the power induction tests imposed by the country standards. Taking this factor into account, the actual lightning surge current flowing through the LCP02-150B1 is equal to :

$$I_{surge} = V_{surge} / (Rg + Rs)$$

With
V surge = peak surge voltage imposed by the standard.
Rg = series resistor of the surge generator
Rs = series resistor of the line card (e.g. PTC)

e.g. : For a line card with 50Ω of series resistors which has to be qualified under Bellcore 1000V 10/1000µs surge, the present current through the LCP02-150B1 is equal to :

$I_{surge} = 1000 / (10 + 50) =$ **17A**

The LCP02-150B1 topology is particularly optimized for the new telecom applications such as fiber in the loop, WLL systems, decentralized central office for example. The schematics of figures 6 and 7 give the 2 most frequent topologies used for these emergent applications

Fig. 6: Protection of SLIC with positive and negative battery voltages.

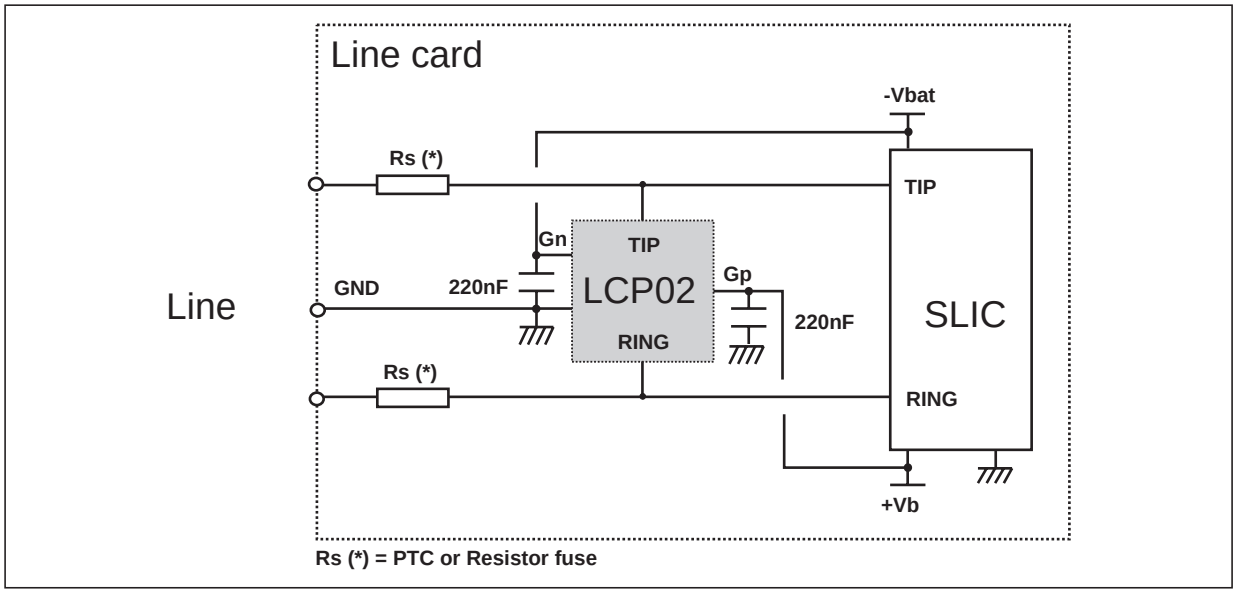


Fig. 7: Protection of high voltage SLIC

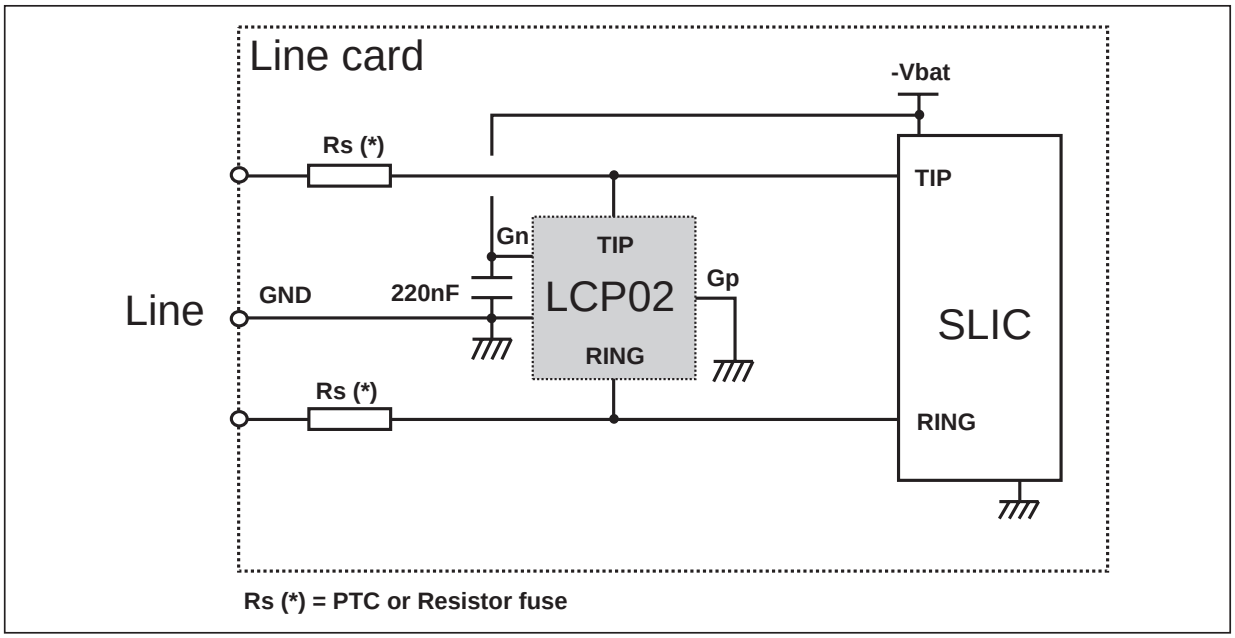
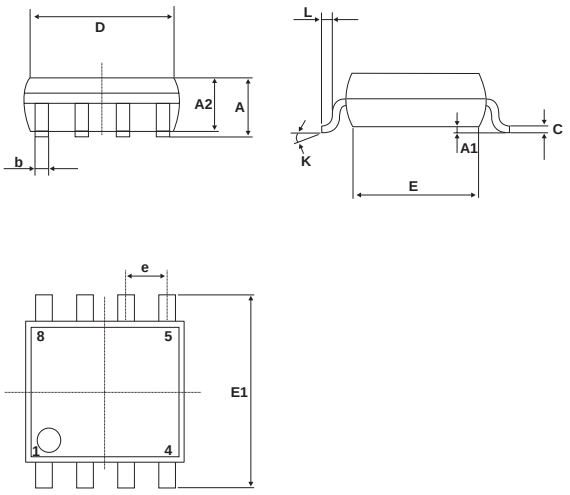


Figure 6 shows the classical protection topology for SLIC using both positive and negative battery voltages. With such a protection the SLIC is protected against surge over +Vb and lower than -Vbat. In this case, +Vb can be programmed up to +95V while -Vbat can be programmed down to -110V. Please note that the differential voltage does not exceed ΔV_{bat} max at 190V.

Figure 7 gives the protection topology for the new SLIC using high negative voltage down to -110V.

PACKAGE MECHANICAL DATA

SO-8 Wide Plastic



REF.	DIMENSIONS					
	Millimetres			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.50			0.099
A1			0.25			0.010
A2	1.51		2.00	0.059		0.079
b	0.35	0.40	0.51	0.013	0.016	0.020
c	0.10	0.20	0.35	0.003	0.008	0.014
D			6.05			0.239
E	5.02		6.22	0.197		0.245
E1	7.62		8.89	0.30		0.35
e		1.27			0.05	
K	10°					
L	0.50		0.80	0.019		0.032

ORDER CODE

Ordering Type	Marking	Package	Weight	Base qty	Delivery mode
LCP02-150B1	LCP02	SO-8-Wide	0.13g	90	Tube
LCP02-150B1RL				1500	Tape & Reel