

1 Block diagram

VT5V VDD5 VDD5REF VDDREF VOLTAGE REFERENCE GENERATOR IO[12:1] 5V REF VADC 1 REF CMP th3
CMP th2
CMP th1 MUX IO_5 : IO_8 IO[12:1] ANALOG IO[15:1] CMP th3 Vref=1,25V ∑Delta ADC 1 12 bit IO_1 : IO_4 ANALOG / SENT 500κΩ 🕽 SENT1 / GTM1 CMP th3 IO_9: IO_12 3<u>.3</u>V ANALOG / LAMBDA from ADC 1 from ADC 2 INT CTRL_CFG from SENT cs from ADC 1 SEQUENCER from ADC 2 EU 1 EU 2 CLK MOSI SCLK SPI CMP th3 MISO MISO THRESHOLD adaption IO_13:IO_15 VRSP ADC1 voltage dividers -> Full Scale R_GND \$ \$ GND

Figure 1. Block diagram

GADG0401180943PS



2 Pin description

10_1 10_12 12 0 2 90 8 0 6<u>0</u> 7_0 S S 48 46 45 44 43 42 41 40 39 38 37 RR3 36 **RST** RR2 2 35 SS_CLK RR1 3 34 SS_CS R_GND 4 33 MOSI VRSP 5 32 MISO **VRSN** 6 31 SYNC 7 VDD5V GND 30 VDD5REF 8 29 INT 9 SENT1_GTM1 AOX 28 VT5V 10 27 SENT2_GTM2 SENT3_GTM3 VRS_OUT 11 26 VI5V 25 SENT4_GTM4 17 18 19 20 21 22 23 24 CTRL_CFG 13 0 GADG0401181015PS

Figure 2. Pin connection diagram

Table 1. Pin description

| Pin-Nr. | Pin-name | Description | Pin-class (1) |
|---------|-----------|---|---------------|
| 1 | RR3 | Reference Pullup Resistor 3 for R-Measurement | 1 |
| 2 | RR2 | Reference Pullup Resistor 2 for R-Measurement | I |
| 3 | RR1 | Reference Pullup Resistor 1 for R-Measurement | I |
| 4 | R_GND (2) | Reference Ground for high accuracy signals | I |
| 5 | VRSP | Positive variable reluctance sensor input | А |
| 6 | VRSN | Negative variable reluctance sensor input | А |

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| Pin-Nr. | Pin-name | Description | Pin-class (1) | |
|---------|------------|--|---------------|--|
| 7 | GND | Ground for supply voltage | S | |
| 8 | VDD5REF | Positive reference to both ADC | | |
| 9 | AOX | Analog output for input channel x | | |
| 10 | VT5V | Ratiometric Voltage output VI5V | | |
| 11 | VRS_Out | Digital Output of Variable reluctance sensor | | |
| 12 | VI5V | Input Voltage | I | |
| 13 | nc | Not connected | - | |
| 14 | VTX | Ratiometric Voltage output VIX | I | |
| 15 | VIX | Input Voltage | I | |
| 16 | CTRL_CFG | Input to control current source / Configuration input to select SPI Address-Mux during Reset | I | |
| 17 | IO_13 | Flexible Input and current output 13 | D | |
| 18 | IO_14 | Flexible Input and current output 14 | D | |
| 19 | IO_15 | Flexible Input and current output 15 | D | |
| 20 | IO_1 | Flexible Input and current output 1 / SENT1 | Α | |
| 21 | IO_2 | Flexible Input and current output 2 / SENT2 | Α | |
| 22 | IO_3 | Flexible Input and current output 3 / SENT3 | Α | |
| 23 | IO_4 | Flexible Input and current output 4 / SENT4 | Α | |
| 24 | nc | Not connected | - | |
| 25 | SENT4_GTM4 | Digital Output for SENT 4 channel / GTM_TO_SENT_4 | I | |
| 26 | SENT3_GTM3 | Digital Output for SENT 3 channel r/ GTM_TO_SENT_3 | I | |
| 27 | SENT2_GTM2 | Digital Output for SENT 2 channel / GTM_TO_SENT_2 | I | |
| 28 | SENT1_GTM1 | Digital Output for SENT 1 channel / GTM_TO_SENT_1 | I | |
| 29 | INT | Interrupt (result status for controller) | I | |
| 30 | VDD5V | 5 V Power supply | I | |
| 31 | SYNC | Digital input to synchronize sequencer start | I | |
| 32 | MISO | Communication interface clock for Master-IN/ Slave-OUT | I | |
| 33 | MOSI | Communication interface for Master-OUT/ Slave-IN | I | |
| 34 | CS | Communication interface chip select | I | |
| 35 | SCLK | Communication interface clock | I | |
| 36 | RST | Reset | I | |
| 37 | nc | Not connected | - | |
| 38 | nc | Not connected | - | |
| 39 | IO_12 | Flexible Input and current output 12 / LAMBDA | Α | |
| 40 | IO_11 | Flexible Input and current output 11 / LAMBDA | Α | |
| 41 | IO_10 | Flexible Input and current output 10 / LAMBDA | Α | |
| 42 | IO_9 | Flexible Input and current output 9 / LAMBDA | Α | |
| 43 | IO_8 | Flexible Input and current output 8 | Α | |
| 44 | IO_7 | Flexible Input and current output 7 | Α | |
| 45 | IO_6 | Flexible Input and current output 6 | Α | |
| 46 | IO_5 | Flexible Input and current output 5 | Α | |

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| Pin-Nr. | Pin-name | Description | Pin-class (1) |
|---------|----------|--------------------|---------------|
| 47 | WAKE | Output for wake-up | I |
| 48 | UBSW | Battery supply | S |

1. see Pin-class legend:

2. R_GND is the ground reference for ADC1, ADC2, VDD5REF voltage divider, input channel voltage dividers. In case R_GND connection to ground on the PCB is lost, R_GND is referenced one diode voltage drop above GND.

Pin-class legend:

- I: ECU Internal Pins: connection to other electrical components on the ECU (Local pins).
- Supply Pins: connection to supply sources with protected battery supply (Local pins except UBSW that is a global pin).
- A: Analog Inputs: connection to external ECU pins (Global pin).
- **D:** Digital Inputs: connection to external ECU pins (Global pin).

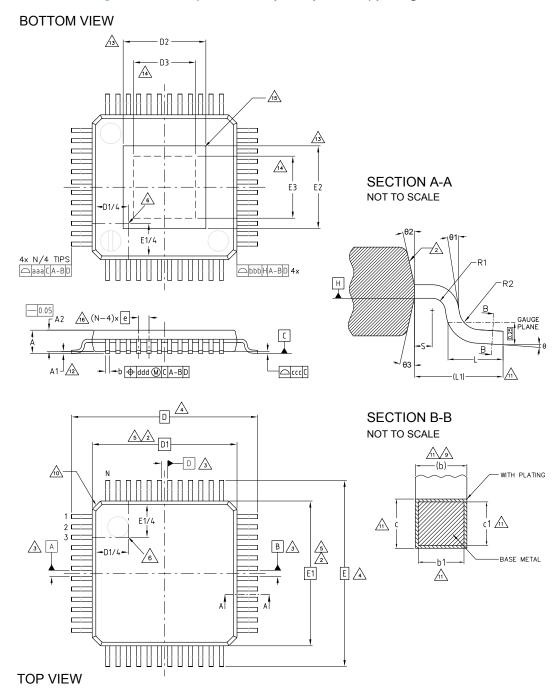


3 Package information

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3.1 TQFP48 (7x7x1 mm exposed pad down) package information

Figure 3. TQFP48 (7x7x1 mm exposed pad down) package outline



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Table 2. TQFP48 (7x7x1 mm exp. pad down) package mechanical data

| | Dimensions | | | | |
|--------------------------------|------------|----------|------|--------|--|
| Symbol | Min. | Тур. | Max. | - Note | |
| Θ | 0° | 3.5° | 7° | | |
| Θ1 | 0° | - | - | | |
| Θ2 | 11° | 12° | 13° | | |
| Θ3 | 11° | 12° | 13° | | |
| Α | - | - | 1.20 | 15 | |
| A1 | 0.05 | - | 0.15 | 12 | |
| A2 | 0.95 | 1.00 | 1.05 | 15 | |
| b | 0.17 | 0.22 | 0.27 | 9, 11 | |
| b1 | 0.17 | 0.20 | 0.23 | 11 | |
| С | 0.09 | - | 0.20 | 11 | |
| c1 | 0.09 | - | 0.16 | 11 | |
| D | | 9.00 BSC | | 4 | |
| D1 | | 7.00 BSC | | 2, 5 | |
| D2 | - | - | 4.15 | 13 | |
| D3 | 3.89 | - | - | 14 | |
| е | | 0.50 BSC | | | |
| E | | 9.00 BSC | | | |
| E1 | | 7.00 BSC | | 2, 5 | |
| E2 | - | - | 4.15 | 13 | |
| E3 | 3.89 | - | - | 14 | |
| L | 0.45 | 0.60 | 0.75 | | |
| L1 | | 1.00 REF | | | |
| N | | 48 | | | |
| R1 | 0.08 | - | - | | |
| R2 | 0.08 | - | 0.20 | | |
| S | 0.20 | - | - | | |
| Tolerance of form and position | | | | | |
| aaa | aaa 0.20 | | | | |
| bbb | 0.20 | | | 1, 7 | |
| ccc | 0.08 | | | | |
| ddd | 0.08 | | | | |

Notes:

- 1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
- 2. The top package body size may be smaller than the bottom package size up to 0.15 mm.
- 3. Datum A-B and D to be determined at datum plane H.
- 4. To be determined at seating datum plane C.
- 5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is "0.25 mm" per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.

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- 6. Details of pin 1 identifier are optional but must be located within the zone indicated.
- All dimensions are in millimeters.
- 8. No intrusion allowed inwards the leads.
- 9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
- 10. Exact shape of each corner is optional.
- 11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
- 12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
- 13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself.
- 14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
- 15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
- 16. "N" is the number of terminal positions for the specified body size.

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Revision history

Table 3. Document revision history

| Date | Version | Changes |
|-------------|---------|------------------|
| 22-Nov-2018 | 1 | Initial release. |



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