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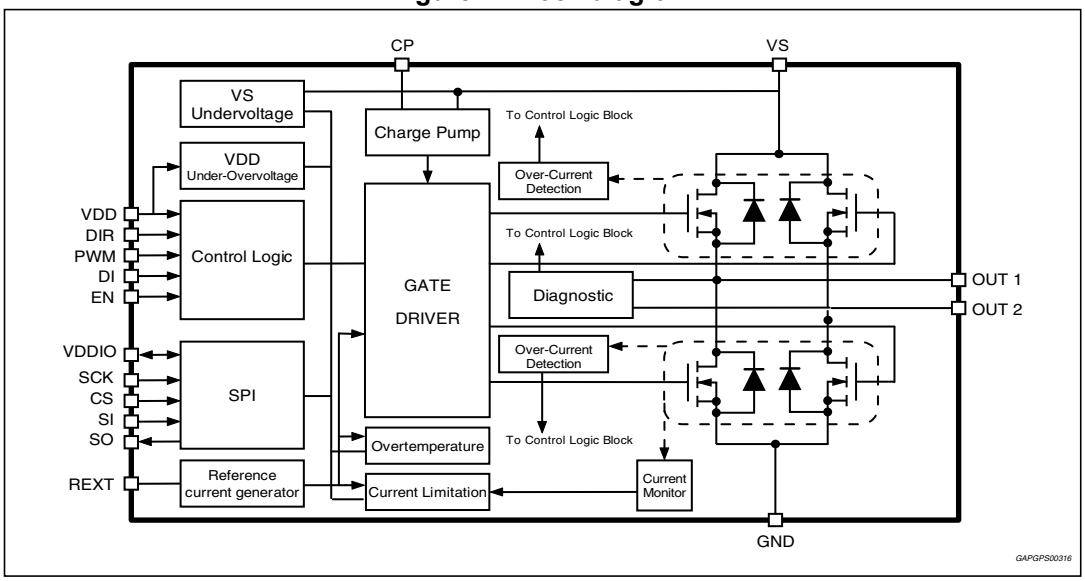
1 Block diagram

Figure 1. Block diagram



2 Pins description

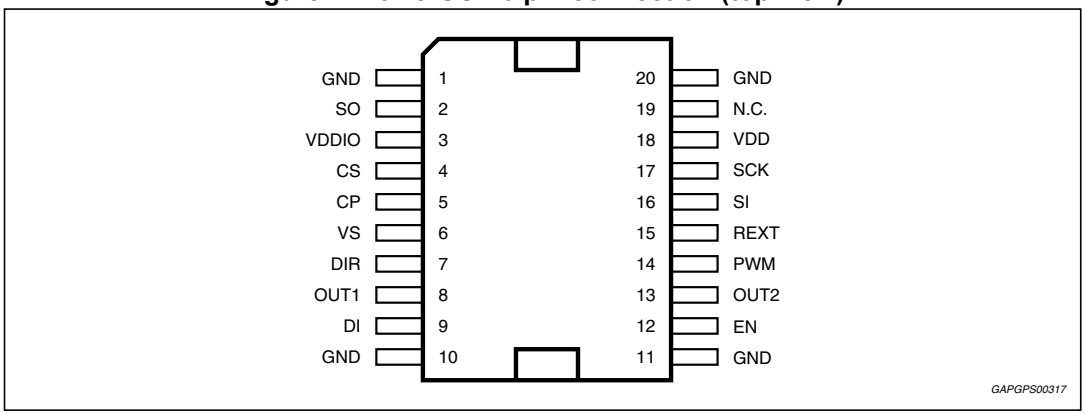
2.1 PowerSO-20

The exposed slug must be soldered on the PCB and connected to GND.

Table 2. PowerSO-20 pin function

Pin N°	Name	Description
1	GND	Ground
2	SO	Serial out
3	VDDIO	Supply voltage for SPI
4	CS	Chip select
5	CP	Charge pump
6	VS	Supply voltage
7	DIR	Direction input
8	OUT1	Output 1
9	DI	Disable
10	GND	Ground
11	GND	Ground
12	EN	Enable
13	OUT2	Output 2
14	PWM	PWM input
15	REXT	External reference resistor
16	SI	Serial in
17	SCK	SPI clock
18	VDD	Supply voltage
19	N.C.	Not connected (To be connected to GND on the PCB)
20	GND	Ground

Figure 2. PowerSO-20 pin connection (top view)



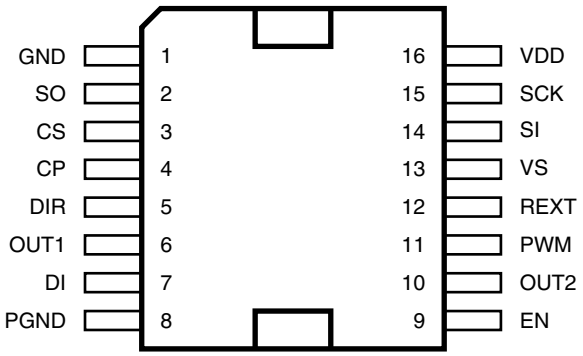
2.2 PowerSO16

The exposed slug must be soldered on the PCB and connected to GND

Table 3. PowerSO16 pin function

Pin Nº	Name	Description
1	GND	Ground
2	SO	Serial Out
3	CS	Chip Select
4	CP	Charge pump
5	DIR	Direction Input
6	OUT1	Output 1
7	DI	Disable
8	PGND	Power Ground
9	EN	Enable
10	OUT2	Output 2
11	PWM	PWM Input
12	REXT	External Reference Resistor
13	VS	Supply Voltage
14	SI	Serial In
15	SCK	SPI Clock
16	VDD	Supply Voltage

Figure 3. PowerSO16 pin connection (top view)



2.3 PowerSSO24

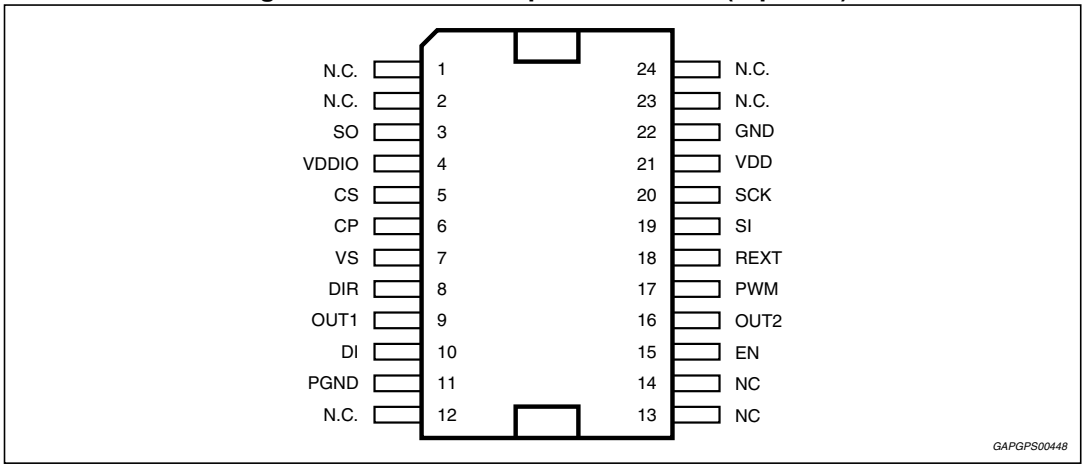
Although this package has two separate pins for the ground (pin 11 = PGND = Power Ground and pin 22 = GND = Logic Ground), the device is designed to work with shortening ground and is mandatory that the two pins have to be connected nearby the IC on the PCB.

The exposed slug must be soldered on the PCB and connected to GND.

Table 4. PowerSSO24 pin function

Pin Nº	Name	Description
1, 2, 12, 13, 14, 23, 24	N.C.	Not Connected
3	SO	Serial Out
4	VDDIO	Supply Voltage for SPI
5	CS	Chip Select
6	CP	Supply Voltage for SPI
7	VS	Supply Voltage
8	DIR	Direction Input
9	OUT1	Output 1
10	DI	Disable
11	PGND	Power Ground
15	EN	Enable
16	OUT2	Output 2
17	PWM	PWM Input
18	REXT	External Reference Resistor
19	SI	Serial In
20	SCK	SPI Clock
21	VDD	Supply Voltage
22	GND	Ground

Figure 4. PowerSSO24 pin connection (top view)



3 Device description

3.1 Supply range

The L9958 has an operating supply range from "Vs_uv" (battery monitoring) up to 28 V. However, the device is tested until 16 V; the functionality of the device is guaranteed until 28 V. The absolute maximum rating is defined to 40 V DC.

3.2 Control inputs

The bridge is controlled by the Inputs PWM, DIR, EN and DI.
All the digital inputs and outputs of the L9958 are compatible with 3.3 V and 5 V CMOS. The power stages output OUT1 and OUT2 are controlled by the direct inputs DIR and PWM as given in *Table 5*. The DIR input gives the direction of output current, while the PWM input controls whether the current is increased or reduced.

3.2.1 DI and EN inputs

The pin DI is internally pulled-up and high active. When DI is active (set to HIGH), the bridge is set to tristate, whatever the state of the DIR and PWM inputs. All the data stored in SPI registers are not reset and SPI communication with the MCU is still possible. When DI is inactive (set to LOW), the bridge is controlled by the DIR and PWM inputs.

The pin EN is internally pulled down and high active. When EN is inactive (set to LOW), the bridge is set to tri-state, whatever the state of the DIR and PWM inputs. All the data stored in SPI registers are not reset and SPI communication with the MCU is still possible. When EN is active (set to HIGH), the bridge is controlled by the DIR and PWM inputs. The coding is performed as shown in the next table. The state of the bridge is transferred in the diagnostic register in a bit called "ACT".

Table 5. Control pins EN, DI

EN	DI	Bit “ACT”	Bridge status
0	0	0	Tri-state
0	1	0	Tri-state
1	0	1	On-state
1	1	0	Tri-state

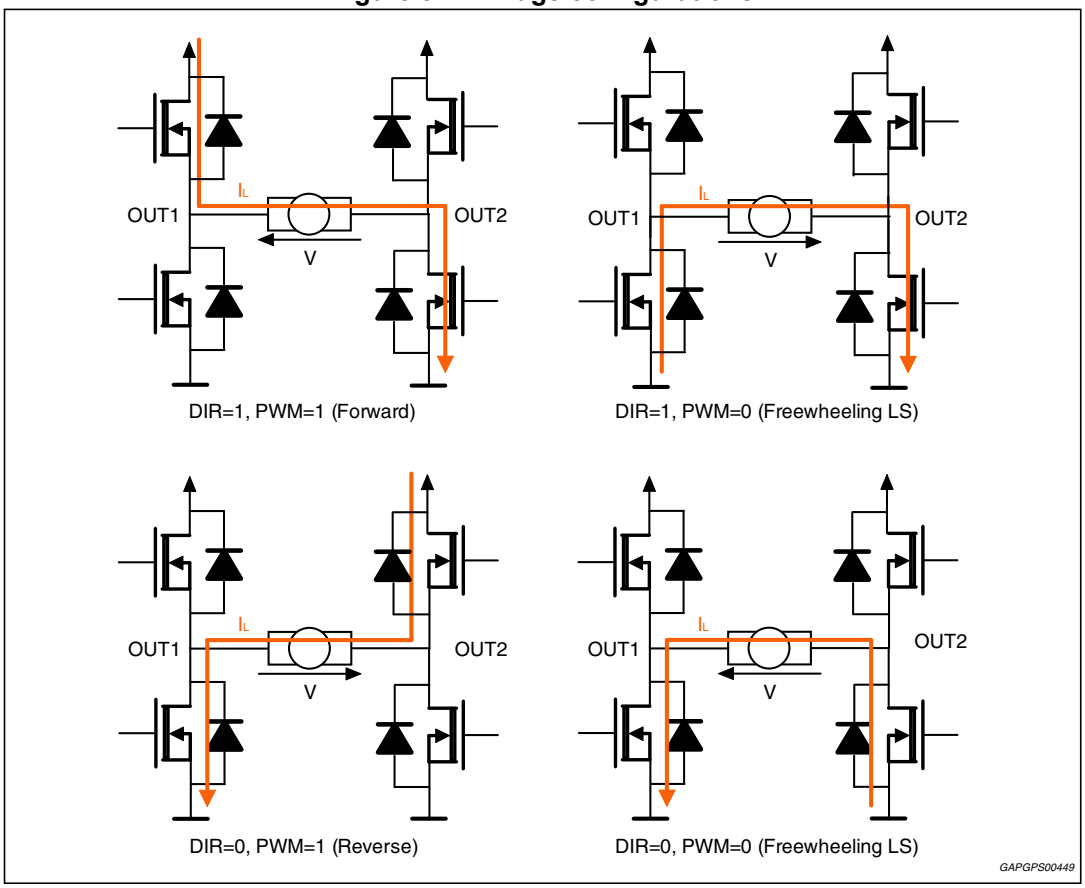
3.2.2 DIR and PWM inputs

The pins DIR and PWM are internally pulled down. The bridge is controlled by these two inputs according to the table below.

Table 6. Control pins DIR, PWM

DIR	PWM	OUT1	OUT2	Bridge Status
H	H	H	L	Forward
L	L	L	L	Freewheeling Low
L	H	L	H	Reverse
H	L	L	L	Freewheeling low

Figure 5. H-Bridge configurations



The outputs can be disabled (set to tri-state) by the Disable and Enable inputs DI and EN. Input DI has an internal pull-up. Input EN has an internal pull-down. During freewheeling phase, an active freewheeling on the Low-Side MOS is automatically set, switching ON the power transistor in parallel to the internal freewheeling diode.

3.3 Serial peripheral interface (SPI)

The SPI is used for bidirectional communication with a control unit, allowing IC configuration, diagnosis and identification. L9958 can also be used in daisy-chain configuration (number of device in the daisy chain is not limited).

The SPI interface of L9958 is a slave SPI interface: the master is the µC which provides CS and SCK to L9958.

Transfer format uses 16 bits word in case of single device configuration and multiple of 16 bits word in case of daisy chain configuration.

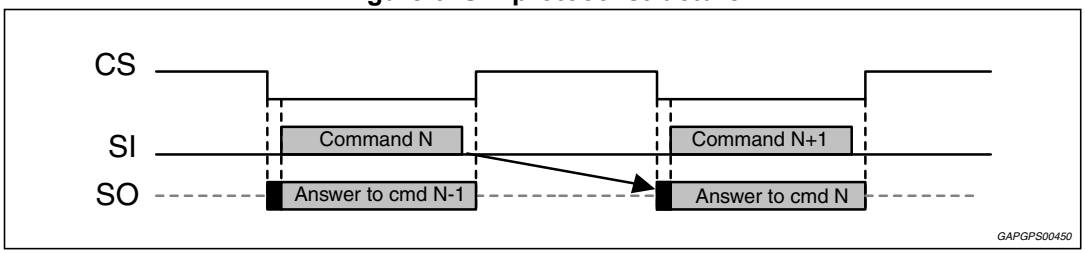
The first answer after Power-ON-Reset is the IC identifier.

A command sent by the µC during transfer N is answered during transfer N+1. SO is clocked on SCK rising edge. SI is sampled on falling edge. When CS = '1' and during power-ON reset, SO is in tri-state. Otherwise, the SPI interface is always active.

Settings made by the SPI control word become active at the end of the SPI transmission and remain valid until a different control word is transmitted or a power on reset occurs.

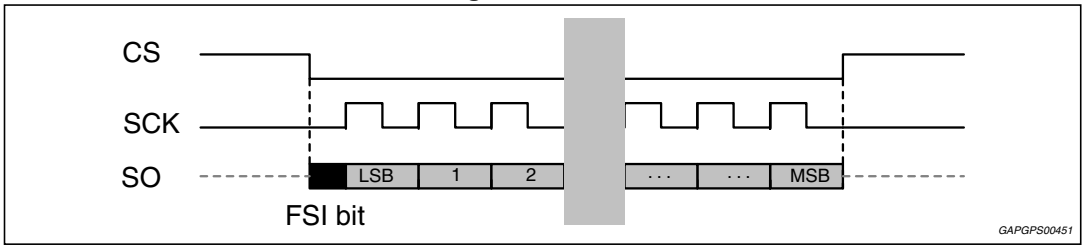
At each SPI transmission, the diagnosis bits as currently valid in the error logic are transmitted. Details on diagnosis are described in *Section 5*.

Figure 6. SPI protocol structure



Between CS falling edge and SCK rising edge, an internal signal called "FSI bit" is set asynchronously on SO output. This can be useful to have internal information on the device without stimulating the SCK clock. The definition of the FSI bit is presented in the diagnostics chapter.

Figure 7. FSI bit



Except the Enable / Disable bit (“ACT” pin), all the bits of diagnosis register are latched and can be released by:

- Diagnosis register read by SPI
- Power-On-Reset condition.

The coding for the Configuration and Diagnosis Registers is reported in the table below.

Table 7. Configuration protocol (CFG_REG)

Bit	Name	Description	Config. value after reset
0 - LSB	RES	Reserved	—
1	DR	Diagnostic Reset Bit	0
2	CL_1	Bit1 for Regulation Current Level	0
3	CL_2	Bit2 for Regulation Current Level	1
4	RES	Reserved	—
5	RES	Reserved	—
6	RES	Reserved	—
7	RES	Reserved	—
8	VSR	Voltage Slew Rate Control Value	0
9	ISR	Current Slew Rate Control Value	0
10	ISR_DIS	Current Slew Rate Control Disable	0
11	OL_ON	Open Load in ON state Enable	0
12	RES	Reserved	—
13	RES	Reserved	—
14	0	“0” to be written	—
15-MSB	0	“0” to be written	—

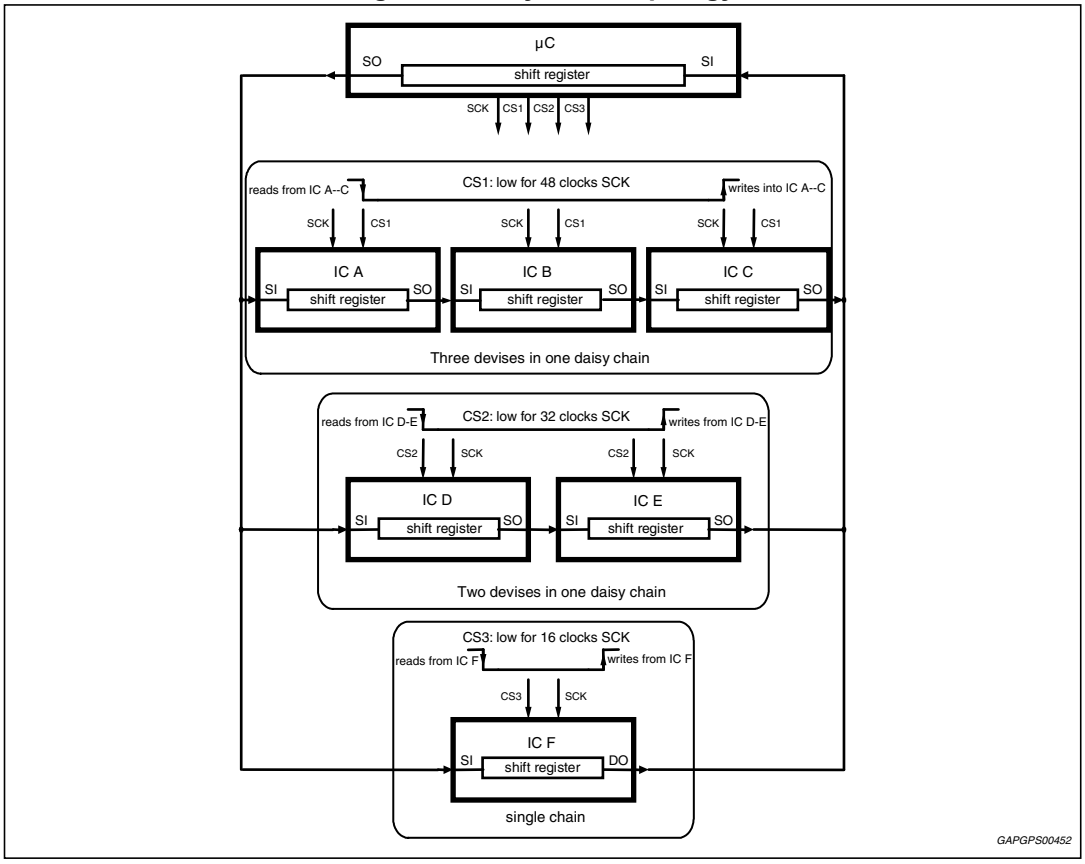
Table 8. Diagnosis protocol (DIA_REG)

Bit	Name	Description	Status after reset	Bit state	DR impact	H-bridge status
0-LSB	OL_OFF	Open Load in OFF condition	0	Latched	–	–
1	OL_ON	Open Load in ON condition	0	Latched	–	–
2	VS_UV	Vs undervoltage	0	Not latched	–	Hi-Z if “1”
3	VDD_OV	Vdd overvoltage	0	Latched	X	Hi-Z if “1”
4	ILIM	Current Limitation reached	0	Latched	–	–
5	TWARN	Temperature warning	0	Latched	–	–
6	TSD	Over-temperature Shutdown	0	Latched	X	Hi-Z if “1”
7	ACT	Bridge enable	1	Not latched	–	Hi-Z if “0”
8	OC_LS1	Over-Current on Low Side 1	0	Latched	X	Hi-Z if “1”
9	OC_LS2	Over-Current on Low Side 2	0	Latched	X	Hi-Z if “1”
10	OC_HS1	Over-Current on High Side 1	0	Latched	X	Hi-Z if “1”
11	OC_HS2	Over-Current on High Side 2	0	Latched	X	Hi-Z if “1”
12	Null	Not Used	–	–	–	–
13	Null	Not Used	–	–	–	–
14	SGND_OFF	Short to GND in OFF condition	0	Latched	–	–
15-MSB	SBAT_OFF	Short to Battery in OFF condition	0	Latched	–	–

3.3.1 Daisy chain operation

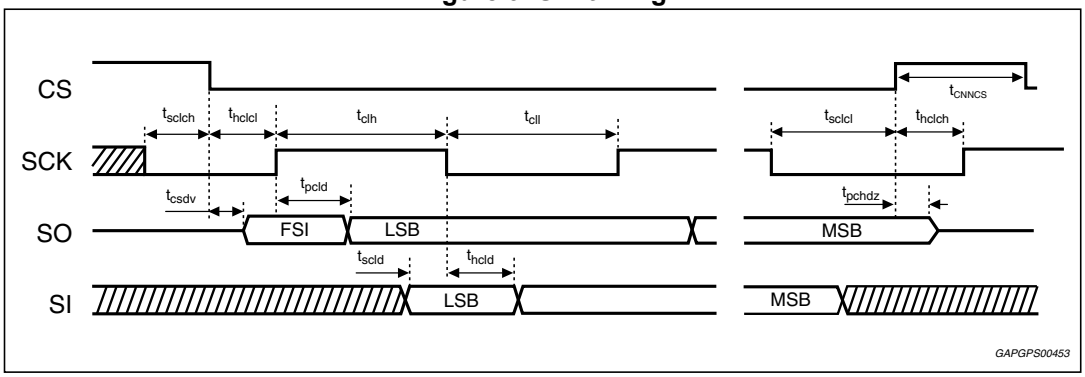
Several L9958 can be connected to one SPI connection in daisy chain operation to save µC interface pins. The number of devices connected in daisy chain is unlimited.

Figure 8. Daisy chain topology



3.4 SPI timing

Figure 9. SPI timing

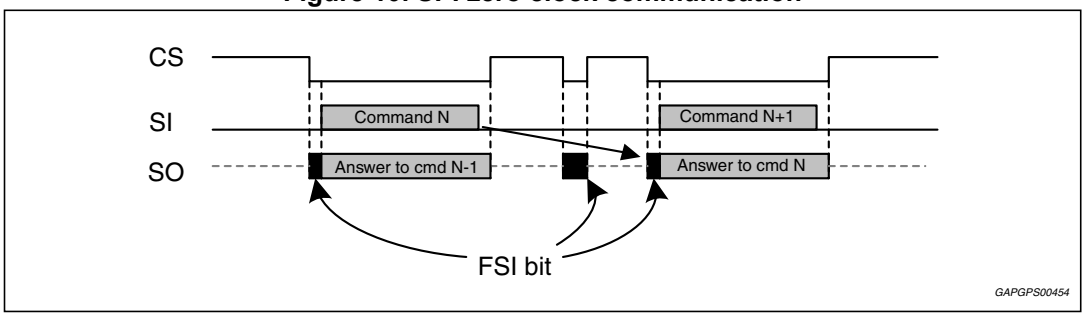


3.5 SPI communication failure

In case of "no SCK edge" when CS = '0', the transfer is considered as valid: no error is returned to the µC. The answer of last command is sent during next transfer.

When the number of SCK period is different from 0 or multiple of 16, next SPI answer is all zero.

Figure 10. SPI zero clock communication



3.6 5 V and 3.3 V output compatibility

In order to ensure a full compatibility with 5V and 3.3V MCU peripherals, the pin VDDIO is dedicated to supply the output buffer of SO. The overall current consumption on Vddio is "Ivddio". A parasitic current from the pin SO could flow through the pin VDDIO in case of over-voltage on SO pin vs. VDDIO pin.

4 Current regulation

To protect the actuator and limit power dissipation, a two-level chopper current limitation is integrated as shown in figure below. The current is measured by sense cells integrated in the low-side switches. As soon the upper current limit “IH” is reached, both low-side drivers are switched on to allow free-wheeling recirculation, until the lower current limit “IL” is reached. During the current regulation, all the slew rate controls are disabled in order to minimize the power dissipation. Four current limit levels can be set by the SPI control bits 0 and 1. In order to achieve very precise current threshold and ripple, an external resistance is required (1 % accuracy on all temp range/lifetime) to generate a current reference. Detailed values for current thresholds and ripple are reported in *Table 9*.

Figure 11. Current limitation

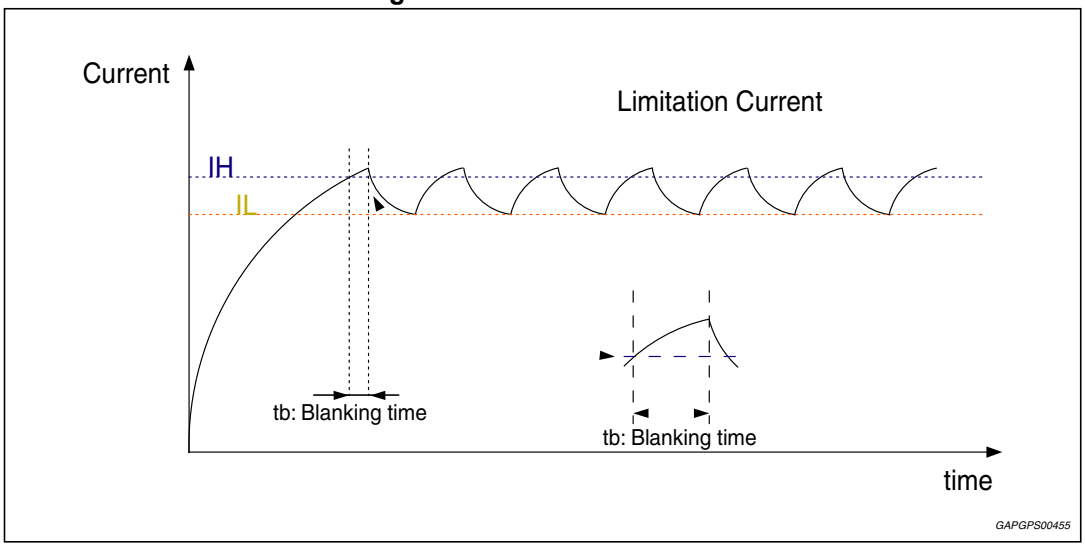


Table 9. Current limitation programmability

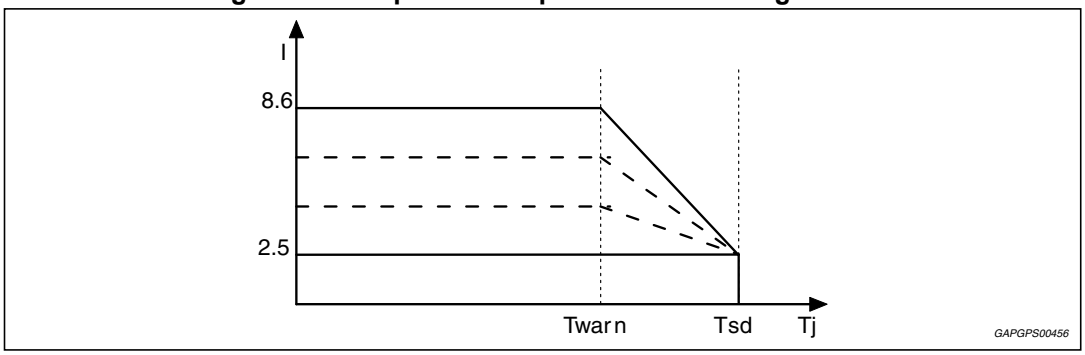
CL_2	CL_1	Current limit (typical values)
0	0	2.5 A
0	1	4 A
1	0	6.6 A (default value)
1	1	8.6 A

4.1 Temperature-dependent current regulation

In order to reduce power dissipation and thus the junction temperature, above a temperature **Twarn** = 160 °C, current regulation high limit linearly decreases with temperature, to reach about 2.5 A at **Tsd** = 175 °C (shutdown temperature).

When this thermal threshold is reached during a current limitation phase, the information is stored and latched in a coding of bits called "**Twarn**". This bit can be reset only if the settings conditions (T_j > Twarn and I_{LIM} = 0) are not present anymore. This feature is mainly used to reduce the power dissipation and thus the junction temperature.

Figure 12. Temperature dependent current regulation

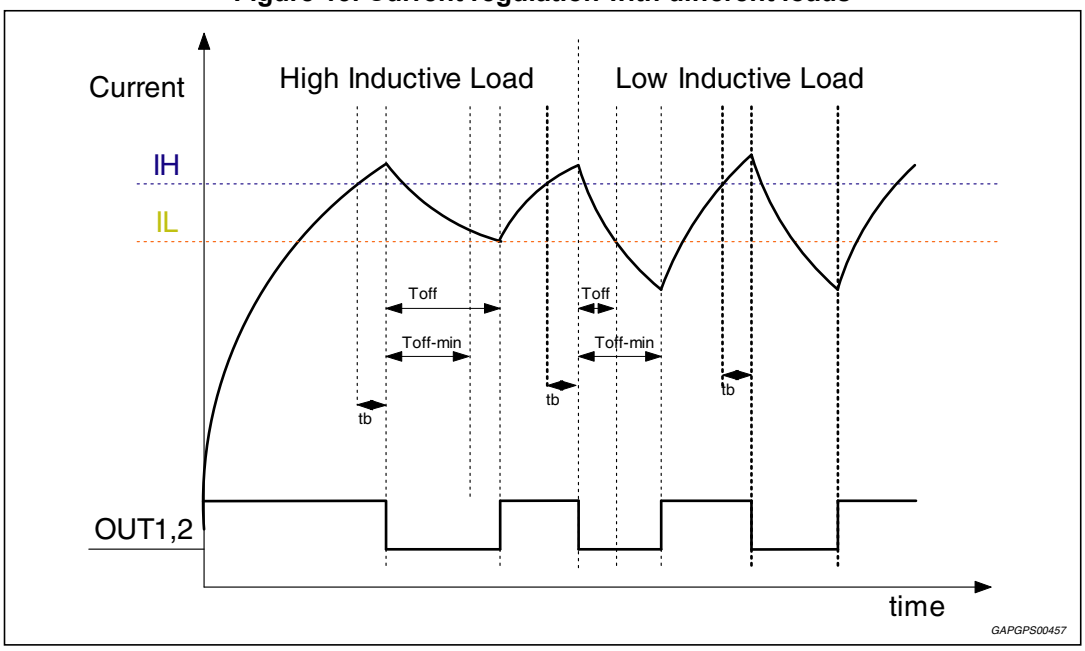


4.2 Current regulation with low-inductive loads

Each time output stages are turned off, an internal timing starts for duration **Toff-min**. Whenever turn-on is reached in a time Toff that is shorter than **Toff-min**, output stages are kept OFF, until **Toff-min** is reached.

In such case the ripple control could be not so precise as specified.

Figure 13. Current regulation with different loads



4.3 Slew rate control in case of current limitation on low-side

The slew rate control can be done on voltage and current or only on voltage. This can be selected by SPI through the bit ISR_DIS.

The slew rate of each high-side power transistor of the bridge is controlled either during turn-on and turn-off (current AND voltage slew rate). The same setting is applied for both switching. Moreover, this slew rate is configurable by SPI in order to get the best trade-off between conducted/radiated EMI and power dissipation during switching. The slew rate

selection can be done "on the fly" by SPI. The corresponding bits are called "**VSR**" and "**ISR**". No external component is needed to select the slew rate range. Only the power transistors not used for freewheeling can be adjusted, the two others can be controlled with a preset slew rate.

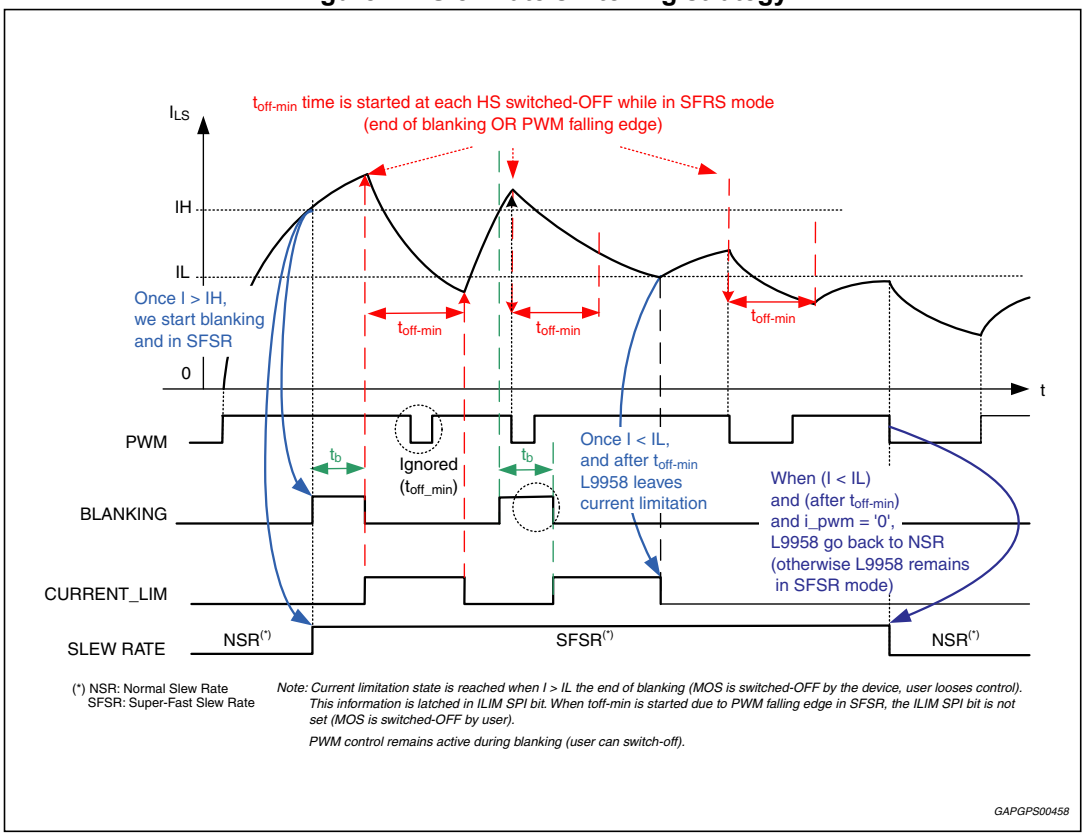
The couples of value defined to fulfill most of the application requirements are described in the table below. The required accuracy is ±50 % for an output current from 1A to 8A and with output voltage up to 19 V. The overall delay implemented between high-side and low-side transistor switching must be adjusted automatically to avoid any cross-conduction through one half-bridge in all conditions.

Table 10. Slew rate control on low side MOS

Range	VSR	ISR	dV/dt (V/µs)	dI/dt (A/µs)
1 (**default value**)	0	0	4	3
2	0	1	4	0.3
3	1	0	2	3
4	1	1	2	0.3
No SR control	Not selectable		14	14

In case of current limitation and any detection that put the bridge in tri-state, the slew rate is not related anymore to the preset bits "**VSR**"; "**ISR**" but to a dedicated faster slew rate control named "SUPER FAST" mode. The automatic change from SPI selectable to SUPER FAST slew rate is described hereafter.

Figure 14. Slew rate switching strategy



5 Diagnostics and protections

A detailed diagnostic of the H-bridge is available through SPI communication. The 16 bits diagnostic word is sent back to the MCU in return of a command word. The diagnostic word is used to report two kinds of information:

- H-Bridge failures:
  - Over-current on each transistor in on-state,
  - Vps under-voltage,
  - Vdd over-voltage,
  - Over-temperature,
  - Open-load in on-state,
  - Off-state diagnostic.
- H-bridge functional status:
  - Current limitation condition,
  - Current limitation decreasing condition,
  - Disable / Enable status.

5.1 Diagnosis reset strategy

5.1.1 Reset requests

Except "ACT" and "VS_UV" bits, all the others are latched and can only be released by:

- Transition from "Disable" to "Enable" on DI / EN pins,
- Diagnostic register read by SPI (see details on each failure release) depending on bit "DR",
- Power-On-Reset condition.

When the diagnostic register is reset, the bridge is switched back to normal mode driven by DIR and PWM. All the settings are kept as before the failure. In case of SPI read, no additional action on DI / EN is needed.

5.1.2 Diagnosis reset bit

In case of "DR" set to LOW (default value), all the bits of the diagnostic register can be reset by the three possibilities described in previous section.

In case of "DR" set to HIGH, the over-current, Vdd over-voltage and over-temperature diagnostic bits can NOT be reset by SPI read and therefore, the bridge is kept in tri-state until a transition from "Disable" to "Enable" on DI/EN pins or Power-on-Reset condition.

Table 11. Diagnosis reset strategy

DR	Diagnosis reset strategy
0	All diagnostic bits reset at each SPI reading (Default)
1	Over current bits (8..11) + Temp. shutdown TSD bit (6) + Vdd over voltage bit (3) NOT reset by SPI

5.2 Protection and on state diagnostics

L9958 is protected against short circuits, overload and invalid supply voltage by the following measures.

5.2.1 Over-current on high-side - short to ground

The high-side switches are protected against a short of the output to ground by an over-current shutdown. If a high-side switch is turned on and the current rises above the short circuit detection current **Ioc** all output transistors are turned off after a filter time **Toc_ls** and the error bits "overcurrent on high side 1 (2)", **OC_HS1** (**OC_HS2**) are stored in the internal status register.

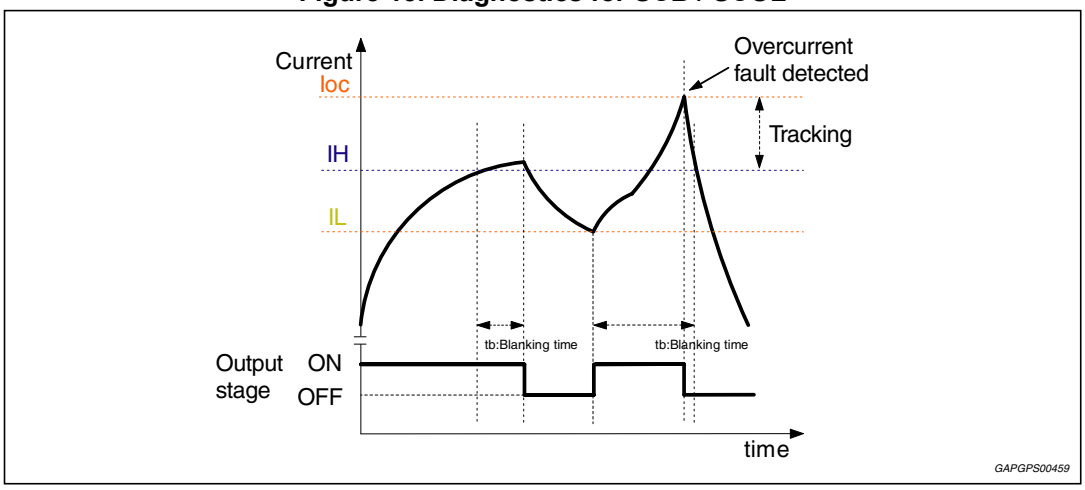
5.2.2 Over-current on low-side - short to Vs

Due to the chopper current regulation, the low-side switches are already protected against a short to the supply voltage. To be able to distinguish a short circuit from normal current limit operation, the current limitation is deactivated for the blanking time $\mathbf{t_b}$ after the current has exceeded the current limit threshold IH. If the short circuit detection current $\mathbf{I_{oc}}$ is reached within this blanking time, a short circuit is detected. All output transistors are turned OFF and the according error bit “Over-Current on Low Side 1 (2)”, **OC_LS1** (**OC_LS2**) is set.

5.2.3 Short circuit over-load

If, during the Blanking time ($\mathbf{t_b}$) of the current regulation mode, the current reaches the $\mathbf{I_{oc}}$ threshold; after a filtering time, the output MOS are switched OFF and the “Short circuit over load” can be checked by the reading of the overcurrent bits of the DIA_REG (please refer to *Table 8* bit 8, 9,10 and 11).

Figure 15. Diagnostics for SCB / SCOL

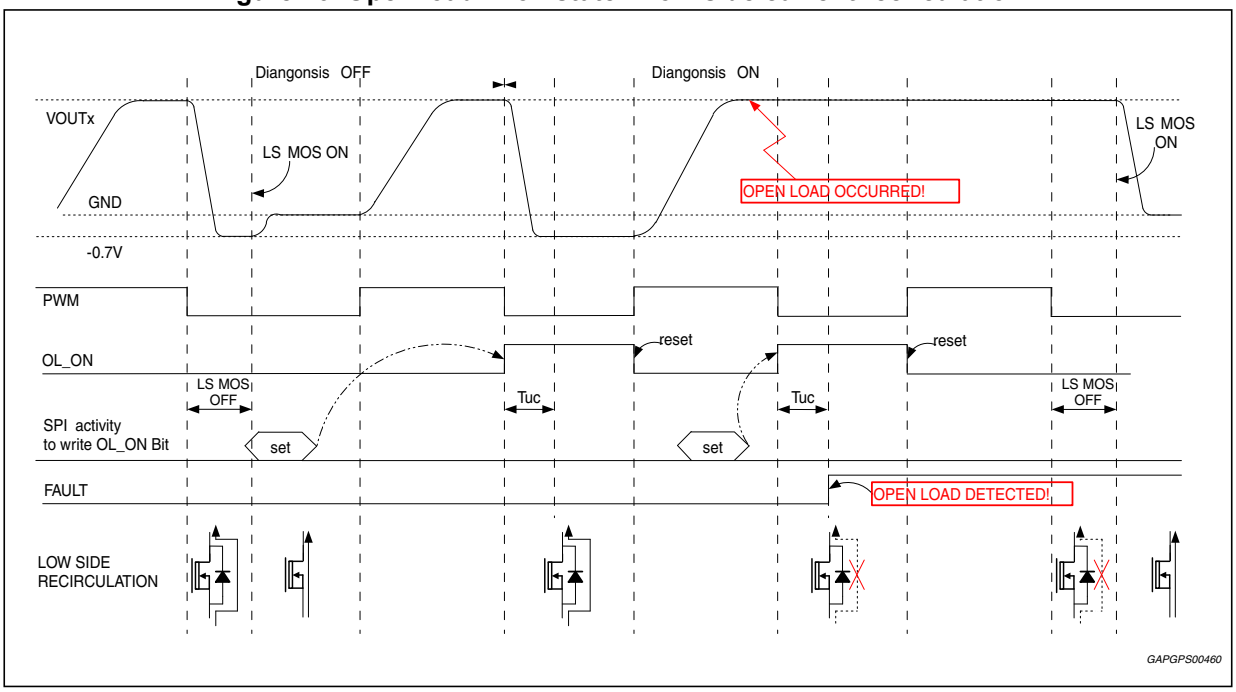


5.2.4 Open load in on state

To perform the Open Load diagnosis in ON state, the flag OL_ON has to be set high through SPI. After every open load diagnosis in ON state, the OL_ON flag is resetted, to perform a new open load diagnosis in ON state the OL_ON flag has to be set again.

This disable the turning on of the low-side drivers during current recirculation. The current flows through the body diode of the low-side MOS for a fixed time. At the end of this fixed time the Vout voltage is sampled and the possible open load condition detected (see *Figure 16*).

Figure 16. Open load in on state - Low-side current recirculation



5.2.5 Over-temperature

When **Twarn** is reached, thermal current reduction is activated, and the information is stored and latched. When **Tsd** is reached, the "**TSD**" bit is set and all output transistors are put in tri-state conditions as long as a reset is applied.

Table 12. Over-temperature

TSD	Comments	Bridge state	FSI
1	Tj > TSD	Tri-state-	1
0 (default)	Tj < TSD	-	0

5.2.6 Vs under-voltage shutdown

If the supply-voltage at the V_S pins falls below the under-voltage detection threshold **Vs_uv_off**, the outputs are set to tri-state and the error bit "Undervoltage at V_S" is set. A filtering time "**Tuv_Vs**" is implemented to avoid unwanted detection due to parasitic glitches. The information is transferred into the SPI register in a bit called "**VS_UV**". This bit is NOT latched. As soon as the voltage rises again above the Vs under-voltage threshold (hysteresis implemented), the bridge is switched back to normal mode driven by DIR and PWM. All the settings are kept as before the under-voltage event.

Figure 17. Battery voltage monitoring

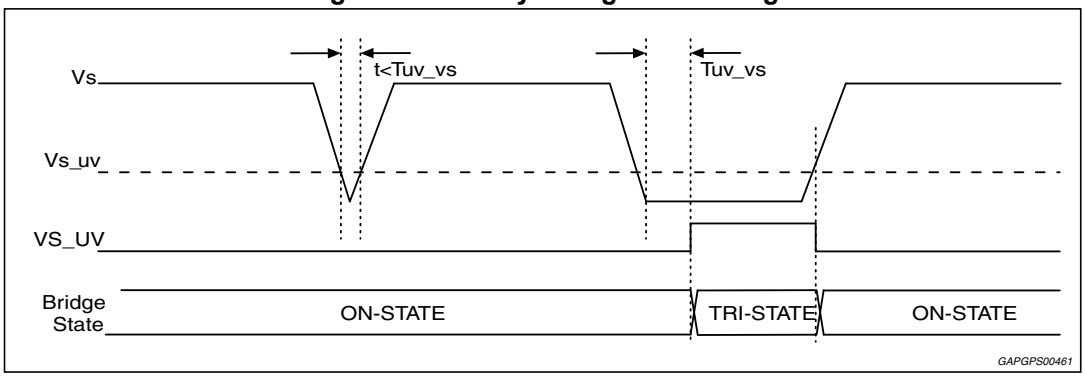


Table 13. Vs under-voltage

VS_UV	Comments	Bridge state	FSI
1	Vs < Vs_uv_off	Hi Z	1 (not latched)
0 (default)	Vs > Vs_uv_on	-	0

5.2.7 Vdd over-voltage detection

Although the Vdd input pin and all I/O's are able to withstand up to 19 V, an over-voltage circuitry is implemented to ensure that the bridge is kept in tri-state when the Vdd voltage is higher than the Vdd overvoltage threshold "**Vdd_ov_off**" for duration longer than "**Tov_Vdd**". The information is detected and stored into the SPI register in a bit called "**VDD_OV**". The bridge is kept in tri-state as long as an appropriate reset is not requested (see *Section 5.1*).

Table 14. Vdd over-voltage detection

VDD_OV	Comments	Bridge state	FSI
1	Vdd > Vdd_ov_off	Hi-Z	1 (latched)
0 (default)	Vdd < Vdd_ov_on	-	0

5.2.8 Vdd under-voltage detection

When the Vdd voltage falls below the under-voltage detection threshold "**Vdd_uv_off**" for duration longer than "**Tuv_vdd**", the bridge is switched to tri-state. In such a condition, the L9958 is going in sleep mode. When the voltage increases above the threshold (hysteresis implemented), the L9958 starts with all the settings reset to their default values (Power On Reset).

5.2.9 Output short protection

The L9958 can sustain short on the outputs. In case of short to GND, short to battery or short between outputs the battery voltage cannot exceed 18 V. The connection of a 100 µF plus a 1µF decoupling capacitors as close as possible to V_s pin and the GND connection of the slug or of the exposed pad is mandatory to improve the robustness.

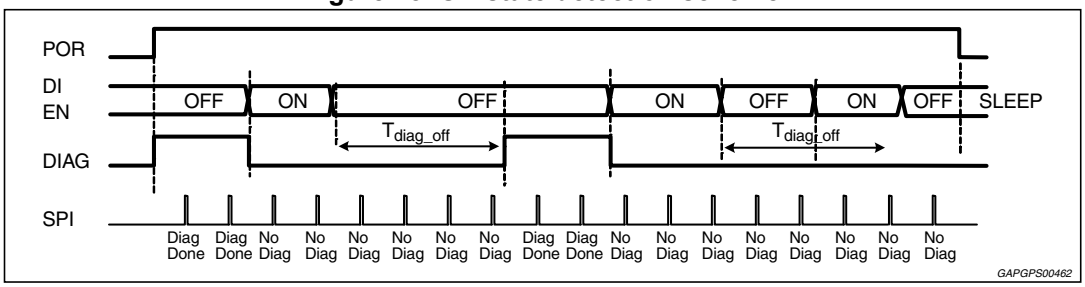
5.3 Off-state diagnosis

This diagnostic is performed in any off-state condition, just after ignition key-on or during an off-state phase occurring after an on-state phase of the bridge.

5.3.1 Off-state detection scheme

In order to avoid any wrong diagnostic, a filtering time "**Tdiag_off**" is applied before performing the detection if the bridge was in on-state before. This filtering time is not applied in case of detection after key on.

Figure 18. Off-state detection scheme

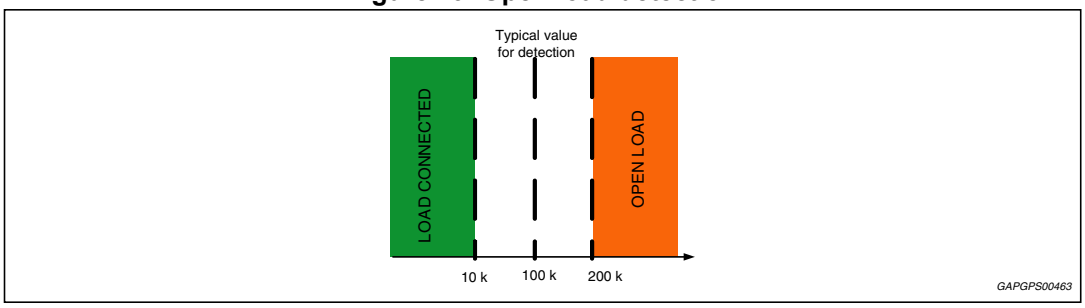


5.3.2 Open load detection

An equivalent resistor of 100 kΩ (typ.) is targeted for open-load detection.

In order to avoid any unwanted supply of the bridge through the high-side transistor body diode during off-state measurement, the current source is connected only if Vs is higher than the Vs under-voltage threshold.

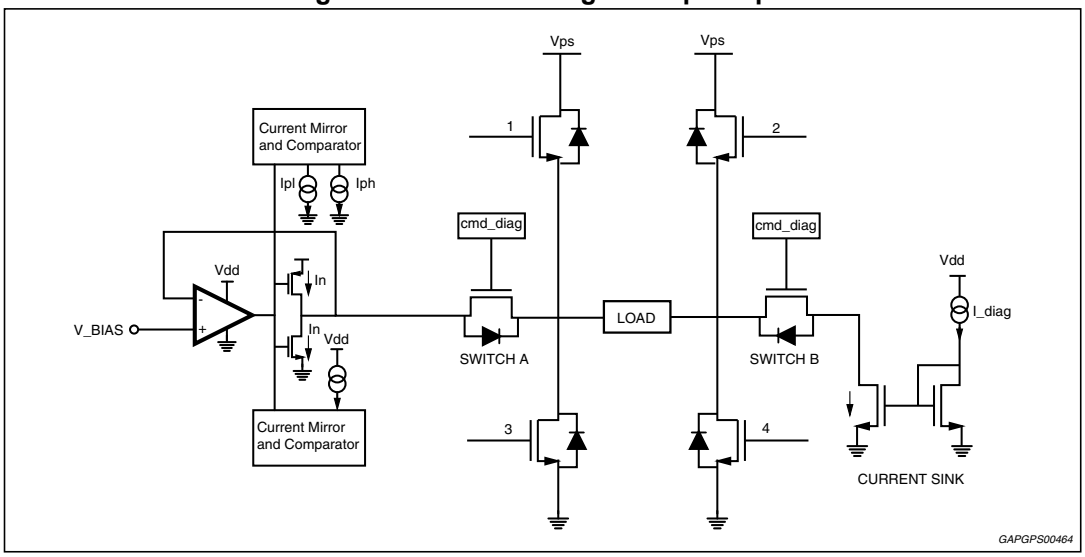
Figure 19. Open load detection



The diagnostic is based on a closed loop voltage control on OUT1 and associated current measurement.

A voltage amplifier forces a constant voltage on OUT1 through two current sources (high-side source and low-side current sink). The OUT2 is pulled-down through a constant current sink. Based on the current flowing out of the amplifier (Ip – In) compared to several current thresholds, open-load as well as short-circuit to ground and battery can be detected.

Figure 20. Off-state diagnostic principle



5.4 H-Bridge functional status

Three bits in the diagnosis register are used to give a feedback about the state of the H-Bridge. Status are Current Limitation (bit 4 "C_LIM"), Temperature Warning (bit 5 "T_WRN") and Bridge Enable Status (bit 7 "ACT"). Those bits do not report a failure but only a functional state of the H-bridge that could be useful to change the control strategy mainly in term of power dissipation.

6 Electrical specifications

6.1 Absolute maximum ratings

The component must withstand the overall following stimulus without any damage or latch-up. Beyond these values, damage to the component may occur.

Table 15. Absolute maximum ratings

Symbol	Parameter	Test condition	Min.	Max.	Unit
V_{ps}	Supply voltage	Continuous Transient (0.5 s; I ≤ 10 A)	-1 -2	40 40	V
V_{dd}	Logic supply voltage	0 V < V_{ps} < 40 V	-0.3	19	V
V_{ddio}	SDO supply voltage	0 V < V_{ps} < 40 V	-0.3	19	V
V_i	Logic input voltage	0 V < V_{ps} < 40 V 0 V < V_{dd} < 19 V	-0.3	19	V
V_o	Logic output voltage	0 V < V_{ps} < 40 V 0 V < V_{dd} < 18.7V	-0.3	Vddio+0.3	V
Output pins (OUTx, VPS)	ESD Compliance	EIA/JESD22-A114-B	±4	-	kV
Input pins			±2	-	
-	ISO 7637 pulses	Cf. standards	-	-	-
-	Latch-up immunity	Jedec standard	-100	+100	mA

Note: In case of load dump condition, status of device outputs is kept unchanged.

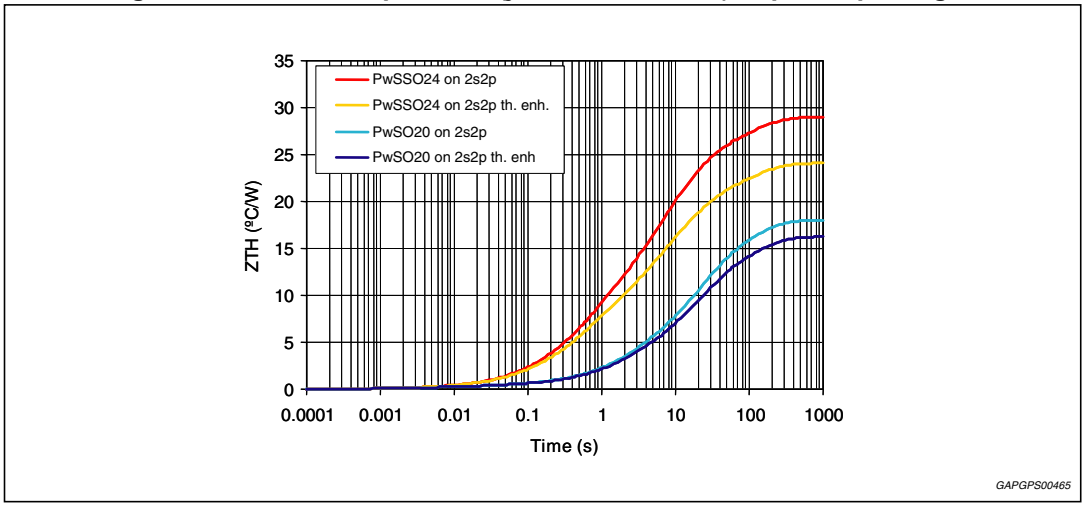
6.2 Thermal data

Table 16. Thermal data

Symbol	Parameter	Test condition	Min.	Max.	Unit
T_j	Junction temperature	Failure condition	-40	OTsd	°C
		Lifetime	-40	150	
T_{stg}	Storage temperature	-	-55	150	°C
T_{amb}	Ambient temperature	0 V < V_{ps} < 40 V	-40	125	°C
$R_{thj\text{-}case}$	Thermal resistance junction to case(1)	Package PowerSO-20	-	1	°C/W
		Package PowerSO16	-	1	
		Package PowerSSO24	-	2	

1. Guaranteed by design and package characterization.

Figure 21. Thermal impedance (junction-ambient) of power packages



6.3 Range of functionality

Within the range of functionality, all L9958 functionalities have to be guaranteed. All voltages refers to GND. Currents are positive into and negative out of the specified pin.

Table 17. Range of functionality

Pos.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
FR1	V_{ps}	Supply voltage	-	Vps_uv_off	14	28(1)	V
FR2	dV_{ps}/d_t	Supply voltage slew rate	-	-20	-	20	V/µs
FR3	V_{dd}	Logic supply voltage	-	Vdd_uv_off	5	Vdd_ov_off	V
FR4	dV_{dd}/d_t	Logic supply voltage slew rate	-	-	-	0.025(2)	V/µs
FR5	V_i	Logic input voltage (SDI, SCLK, NCS, DI, EN, DIR, PWM)	See also *Table 15: Absolute maximum ratings*.	-0.3	-	Vdd_ov_off	V
FR6	V_{ddio}	SDO output voltage	-	3	-	5.5	V
FR7	f_{spi}	SPI clock frequency	-	-	-	5	MHz

1. In load dump conditions V_{ps} ranges between 28V and 40V. During load dump, status of device outputs is kept unchanged,
2. To VDD pin are connected 10µF and 10nF (close to the pin) capacitors.

6.4 Electrical characteristics

T_{case} = -40 °C to 125 °C unless otherwise specified,

V_{dd} = 4.5 V to 5.5 V unless otherwise specified

V_{ps} = 4 V to 28 V unless otherwise specified

All voltages refer to GND. Currents are positive into and negative out of the specified pin.

6.4.1 Device supply

Table 18. Device supply

Pos.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
1.1	I_{ps}	Power supply current	V_{dd} < 0.7 V; V_{ps} = 16 V from -40 °C to 25 °C	-	-	20	µA
			V_{dd} < 0.7 V; V_{ps} = 16 V at 125 °C	-	-	35	µA
			F_{pwm} = 0, I_{out} = 0	-	-	20	mA
1.2	I_{out}	Leakage current on output	Bridge in tri-state	-	-	100	µA
1.3	I_{cc}	Logic-supply current	V_{dd} >$V_{dd\_uv\_on}$ F_{PWM} = 0	-	-	5	mA
			F_{PWM} = 20 kHz (Average value)	-	-	5	mA

6.4.2 Device supply monitoring

Table 19. Device supply monitoring

Pos.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
2.1	$V_{ps\_uv\_off}$	V_{ps} under-voltage threshold	V_{ps} decreasing	-	-	4	V
2.2	$V_{ps\_uv\_on}$	V_{ps} under-voltage threshold	V_{ps} increasing	-	-	4.5	V
2.3	$V_{ps\_uv\_hyst}$	V_{ps} under-voltage hysteresis	-	0.1	-	-	V
2.4	T_{uv_vps}	V_{ps} under-voltage filtering time	V_{ps} decreasing	1	-	3	µs
2.5	$V_{dd\_uv\_off}$	V_{dd} under-voltage threshold	V_{dd} decreasing	3	-	3.7	V
2.6	$V_{dd\_uv\_on}$	V_{dd} under-voltage threshold	V_{dd} increasing	3.3	-	4	V
2.7	$V_{dd\_uv\_hyst}$	V_{dd} under-voltage hysteresis	-	0.1	-	-	V
2.8	T_{uv_Vdd}	V_{dd} under-voltage filtering time	V_{dd} decreasing	1	-	4	µs
2.9	$V_{dd\_ov\_off}$	V_{dd} over-voltage threshold	V_{dd} increasing	5.8	-	6.8	V
2.10	$V_{dd\text{-}ov\_on}$	V_{dd} over-voltage threshold	V_{dd} decreasing	5.5	-	6.5	V
2.11	$V_{dd\_ov\_hyst}$	V_{dd} over-voltage hysteresis	-	0.1	-	-	V
2.12	T_{ov_Vdd}	V_{dd} over-voltage filtering time	V_{dd} increasing	60	100	140	µs

6.4.3 SPI

Table 20. SPI

Pos.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
3.1	f_{spi}	Clock frequency (50 % duty cycle)	-	-	-	5	MHz
3.2	T_{sdo_trans}	SDO transition speed, 20-80 %	V_{sdo} = 5V, C_{load} = 50 pF (1)	5	-	30	ns
			V_{sdo} = 5 V, C_{load} = 150 pF	5	-	50	ns
3.3	T_{clh}	Minimum time SCLK = HIGH	-	75	-		ns
3.4	T_{cll}	Minimum time SCLK = LOW	-	75	-		ns
3.5	T_{pcld}	Propagation delay (SCLK to data at 10% of SDO rising edge)	-	-	-	40	ns
3.6	T_{csdv}	NCS = LOW to data at SDO active	-	-	-	85	ns
3.7	T_{sclch}	SCLK low before NCS low (setup time SCLK to NCS change H/L)	-	75	-	-	ns
3.8	T_{hclcl}	SCLK change L/H after NCS = low	-	75	-	-	ns
3.9	T_{scld}	SDI input setup time (SCLK change H/L after SDI data valid)	-	40	-	-	ns
3.10	T_{hcld}	SDI input hold time (SDI data hold after SCLK change H/L)	-	40	-	-	ns
3.11	T_{sclcl}	SCLK low before NCS high	-	100	-	-	ns
3.12	T_{hclch}	SCLK high after NCS high	-	100	-	-	ns
3.13	T_{pchdz}	NCS L/H to SDO @ high impedance	-	-	-	75	ns
3.14	T_{onncs}	NCS min. high time	-	300	-		ns
3.15	-	Capacitance at SDI, SCLK; NCS	-	-	-	14	pF
	-	Capacitance at SDO	-	-	-	19	pF
3.16	T_{fncs}	NCS Filter time will be ignored) Guaranteed by design (Pulses = TfNCS	Guaranteed by design	10	-	40	ns
3.17	V_{ddio}	Supply voltage for SDO output buffer	-	3	-	5.5	V
3.18	I_{vddio}	Current consumption on Vddio	(2)	-	-	1	mA
3.19	sdo_H	High output level on SDO	I_{sdo} = 1.5 mA	V_{ddio}-0.4	-	-	V
3.20	sdo_L	Low output level on SDO	I_{sdo} = 2 mA	-	-	0.4	V
3.21	I_{sdo}	Tri state leakage current	NCS = HIGH V_{DDIO} = 5 V	-5	-	5	µA

1. Not tested – guaranteed by C_{load} = 150 pF measurement
2. Measured for PSO16 at wafer sort level only.

6.4.4 Digital inputs: TTL // 3.3V / 5V CMOS compatible

Table 21. Digital inputs: TTL // 3.3V / 5V CMOS compatible

Pos.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
4.1	V_{ih}	Input voltage HIGH	-	2	-	Vdd+0.3	V
4.2	V_{il}	Input voltage LOW	-	-0.3	-	0.8	V
4.3		Hysteresis of input voltage	-	200	-	-	mV
4.4	I_{inl}	Input current source for: DI / NCS / SCLK / SDI	V_{in} = 0 V	-100	-	-30	µA
			V_{in} = 5 V No back supply allowed	-	-	5	
4.5	I_{inh}	Input current sink for: EN / DIR / PWM	V_{in} = 5 V	30	-	100	µA
			V_{in} = 0 V	-5	-	-	
4.6	V_{rext}	External resistor	-	-	1.24	-	V
	R_{ext}		-	-	10	-	kΩ
			Overall tolerance can be taken as 3.5 %	-	1	-	%

6.4.5 Bridge output drivers

Table 22. Bridge output drivers

Pos.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
5.1	R_{dson_h}	High-side transistor R_{dson}	T_j = 150 °C, I_{out} = 3 A 4 V < V_{ps} < 5 V	-	-	300	mΩ
			T_j = 150 °C, I_{out} = 3 A V_{ps} > 5 V	-	-	150	
5.2	R_{dson_l}	Low-side transistor R_{dson}	T_j = 150 °C, I_{out} = 3 A 4 V < V_{ps} < 5 V	-	-	300	mΩ
			T_j = 150 °C, I_{out} = 3 A V_{ps} > 5 V	-	-	150	
5.3	V_{bd_h}	Body diode forward voltage drop high-side transistor	I_{diode} = 3 A	-	1.2	2	V
5.4	V_{bd_l}	Body diode forward voltage drop low-side transistor	I_{diode} = 3 A	-	1.2	2	V

6.4.6 Over-temperature monitoring

Table 23. Over-temperature monitoring

Pos.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
6.1	OTwarn	Over-temperature warning	-	150	-	170	°C
6.2	OTsd	Over-temperature shut-down	-	170	-	200	°C
6.3	OThyst	Over-temperature hysteresis	-	10	-	-	°C
6.4	T_{TSD}	Over-temperature filtering time	Guaranteed by clock measurement	-	36	-	µs

6.4.7 Current limitation and over-current detection

Table 24. Current limitation and over-current detection

Pos.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
7.1	I_{lim_H}	Current limitation high threshold	CL1:0 = 00; -40 °C ≤ T_j ≤ 150 °C	2	2.5	3.1	A
			CL1:0 = 01; -40 °C ≤ T_j ≤ 150 °C	3.5	4	4.85	
			CL1:0 = 10; -40 °C ≤ T_j < 25 °C	5.5	6.75	8	
			CL1:0 = 10; 25 °C ≤ T_j ≤ 150 °C	5.5	6.6	7.7	
			CL1:0 = 11; -40 °C ≤ T_j < 25 °C	7.8	9.1	10.4	
			CL1:0 = 11; 25 °C ≤ T_j ≤ 150°C	7.6	8.6	9.6	
			CL1:0 = XX, T_j = OTsd	2	2.5	3	
7.2	I_{lim_L}	Current limitation low threshold	CL1:0 = 0X; -40 °C ≤ T_j ≤ 150 °C	I_{lim_H}–0.2	I_{lim_H}-0.5	I_{lim_H}-0.8	A
			CL1:0 = 10; -40°C ≤ T_j < 25 °C	I_{lim_H}-0.35	I_{lim_H}-0.65	I_{lim_H}-0.95	
			CL1:0 = 10; 25 °C ≤ T_j ≤ 150°C	I_{lim_H}-0.35	I_{lim_H}-0.55	I_{lim_H}-0.85	
			CL1:0 = 11; -40°C ≤ T_j < 25°C	I_{lim_H}–0.4	I_{lim_H}-0.7	I_{lim_H}-1	
			CL1:0 = 11; 25 °C ≤ T_j ≤ 150°C	I_{lim_H}–0.4	I_{lim_H}-0.55	I_{lim_H}-0.95	
7.3	T_{limh}	High current limitation threshold filtering time	can be included in T_{blanck}	0.1	-	1	µs
7.4	T_{liml}	Low current limitation threshold filtering time	-	1	-	3	µs
7.5	T_{offmin}	Current limitation delay time	-	30	-	45	µs
7.6	T_b	Blanking time	-	4.9	-	8.7	µs

Table 24. Current limitation and over-current detection (continued)

Pos.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
7.7	Ioc_ls Ioc-hs	Low-side over-current threshold High-side over-current threshold	CL1:0 = 0X; -40 °C ≤ T_j ≤ 150 °C	5.5	7.7	11	A
			CL1:0 = 1X; -40°C ≤ T_j < 25 °C	9.3	12	16.5	
			CL1:0 = 1X; 25 °C ≤ T_j ≤ 150°C	9.3	11.5	14	
	Tracking		CL1:0 = 0X; CL1:0 = 10; -40 °C ≤ T_j ≤ 150 °C	I_{lim_h}+2	-	-	
			CL1:0 = 11; -40 °C ≤ T_j ≤ 150 °C	I_{lim_h}+1.3	-	-	
7.8	Toc_ls Toc_hs	Low-side & high-side over-current detection filtering time	-	0.8	-	2.5	µs

6.4.8 Diagnostic of open-load in on-state

Table 25. Diagnostic of open-load in on-state

Pos.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
8.1	Is_OL-on	Current source	T_j = -40 °C (go-no-go functional test)	50	-	120	µA
			T_j = 25 °C to 150 °C (go-no-go functional test)	50	-	100	
8.2	Tmeas_on	Detection time (settling time)	-	-	3	5	µs

6.4.9 Off-state diagnostic

Table 26. Off-state diagnostic

Pos.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
9.1	R_{OL}	Load detection threshold		10	60	200	kΩ
9.2	Tdiag_off	Delay time before enabling off-state diagnostic structure	diag after on-state Guaranteed through SCAN	100	125	150	ms
9.3	$T_{diag\text{-}off\_1}$	Off-state diag filtering time when OUT 1 and/or 2 decrease from V_{ps}	used each time OUT pins are released from Vps (after release of SCB, after Tdiag_off) Guaranteed through SCAN	2.4	3	3.6	ms
9.4	$T_{diag\_off\_2}$	Off-state diagnostic filtering time on failure detection	One symmetric filter for each failure type (OL, SCG, SCB) Guaranteed through SCAN	200	250	300	µs
9.5	T_{clock}	Oscillator frequency	-	4	-	6	MHz

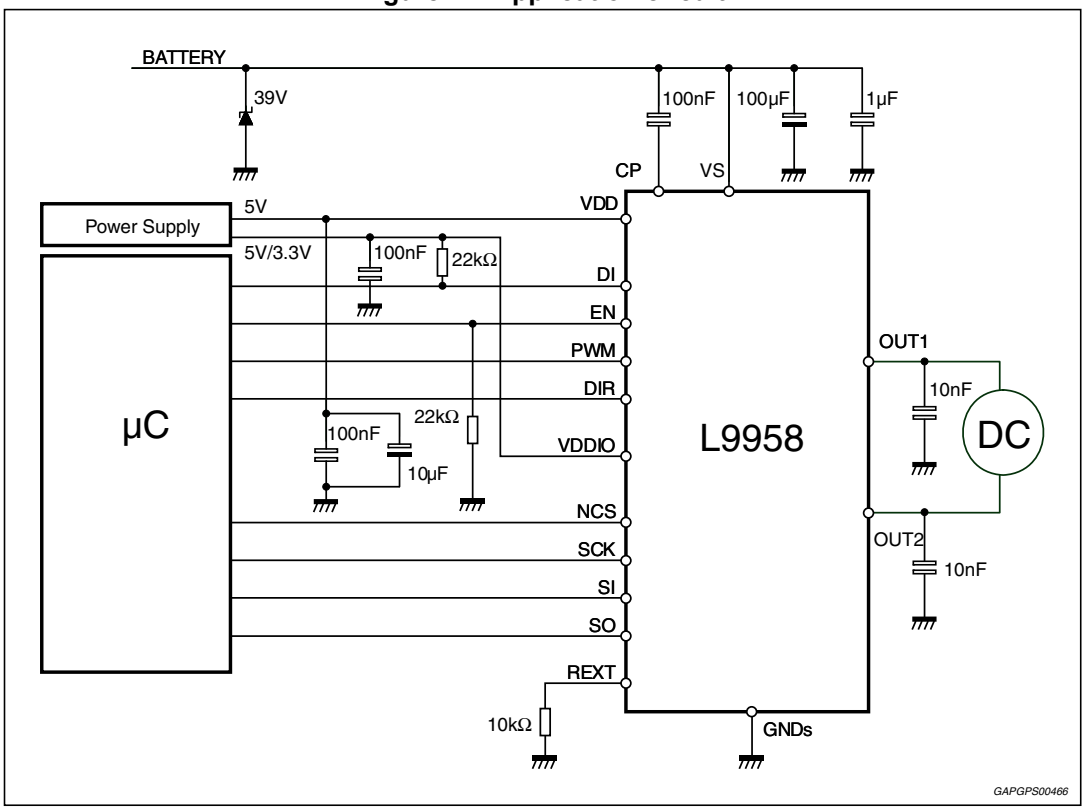
6.4.10 Timing characteristics

Table 27. Timing characteristics

Pos.	Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
10.1	f_{pwm}	PWM frequency	-	-	-	20	kHz
10.2	T_{don}	Delay time for switch-on	R_{load} @ I_{out} = 3 A PWM → 90% V_{out} (or 10 % I_{out})	-	-	10	µs
	T_{doff}	Delay time for switch-off	R_{load} @ I_{out} = 3 A PWM → 10 % V_{out} (or 90% Iout)	-	-	10	µs
	ΔT_d	Delay time: symmetry	PWM accuracy = 1% @ 2kHz	-	-	5	µs
10.3	T_{d_dis}	Disable delay time	DI / EN → 90% OUTx @ I_{out} = 3 A	-	-	6	µs
10.4	T_{d_en}	Enable delay time	DI / EN → 10 % OUT	-	-	6	µs
10.5	T_{d_pow}	Power-on delay time	DIR= PWM=EN=1 / DI=0 no load / V_{PS} = V_{dd} increasing V_{ps} = V_{dd} → 10 % V_{out1} (= V_{ps})	-	-	200	µs
10.6	T_{d_filter}	DI / EN digital filter time	-	1	-	3	µs
10.7	T_{rise_H}	Low-side transistor rise time	Non selectable by SPI	0.04	-	0.2	µs
10.8	T_{fall_H}	Low-side transistor fall time	Non selectable by SPI	1	-	3	µs
10.9	dV_{out}/d_t	Voltage slew rate for high-side transistors (Measurement is performed between 30 % and 70 % of the slope)	super fast mode	7	14	24	V/µs
			VSR = 0	2	4	6	
			VSR = 1	1	2	3	
10.10	dI_{out}/d_t	Current slew rate for high-side transistors (Measurement is performed between 40 % and 60 % of the slope)	ISR=0	1.5	3	4.5	A/µs
			ISR=1	0.15	0.3	0.45	
10.11	T_{diag}	Timing for reliable diagnostic	Guaranteed through SCAN pattern	35	-	55	µs

7 Application circuit

Figure 22. Application circuit



1. The above application diagram shows all the suggested components for a proper device operation.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

Figure 23. PowerSO-20 mechanical data and package dimensions

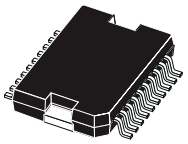
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1 (2)	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8°(typ.)					
S	8°(max.)					
T		10			0.394	

(1) "D and E1" do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006")
- Critical dimensions: "E", "G" and "a3".

(2) For subcontractors, the limit is the one quoted in jedec MO-166

OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



JEDEC MO-166

PowerSO20

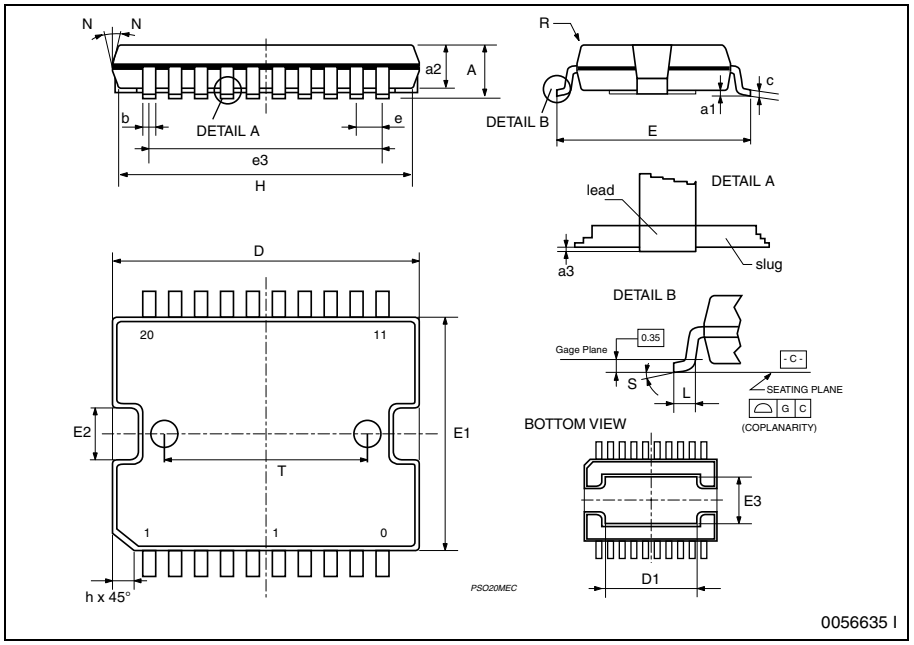
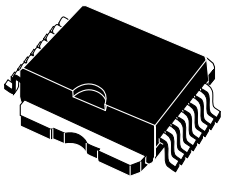


Figure 24. PowerSO16 mechanical data and package dimensions

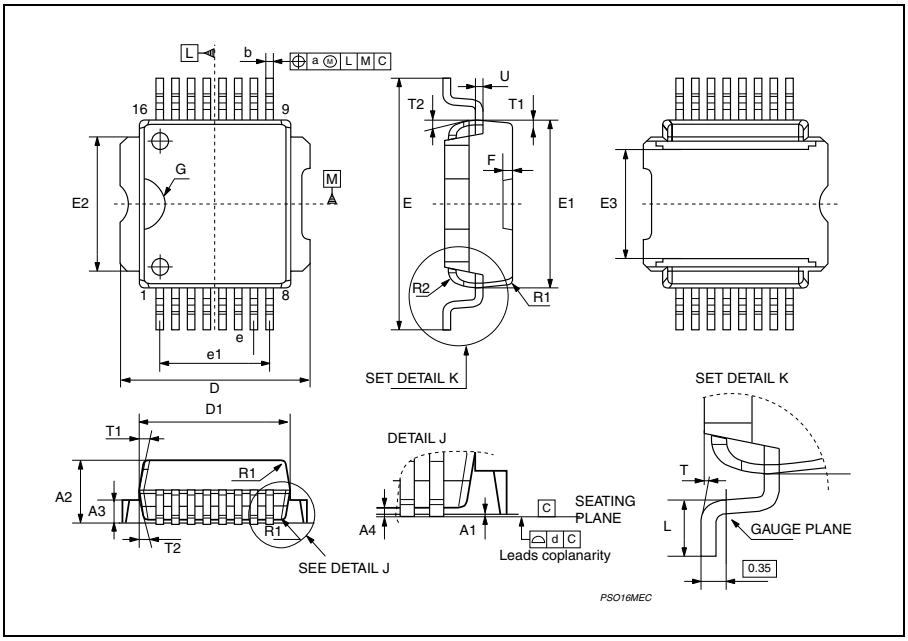
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A1	0	0.05	0.1	0	0.002	0.004
A2	3.4	3.5	3.6	0.133	0.137	0.141
A3	1.2	1.3	1.4	0.048	0.05	0.052
A4	0.15	0.2	0.25	0.006	0.007	0.01
a		0.2			0.007	
b	0.27	0.35	0.43	0.011	0.013	0.017
c	0.23	0.27	0.32	0.009	0.01	0.012
D	9.4	9.5	9.6	0.37	0.374	0.377
D1	7.4	7.5	7.6	0.291	0.295	0.299
d		0.1			0.004	
E (1)	13.85	14.1	14.35	0.545	0.555	0.565
E1	9.3	9.4	9.5	0.366	0.37	0.374
E2	7.3	7.4	7.5	0.287	0.291	0.295
E3	5.9	6.1	6.3	0.232	0.24	0.248
e		0.8			0.031	
e1		5.6			0.22	
F		0.5			0.019	
G		1.2			0.047	
L	0.8	0.95	1.1	0.031	0.037	0.043
R1			0.25			0.01
R2		0.8			0.031	
T	2° (min.), 5° (typ.), 8° (max.)					
T1	6° (typ.)					
T2	10° (typ.)					

(1) Resin protrusions not included (max value: 0.1mm per side).

OUTLINE AND MECHANICAL DATA



PowerSO16



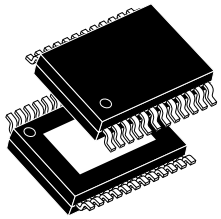
GAPGPS00467

Figure 25. PowerSSO24 mechanical data and package dimensions

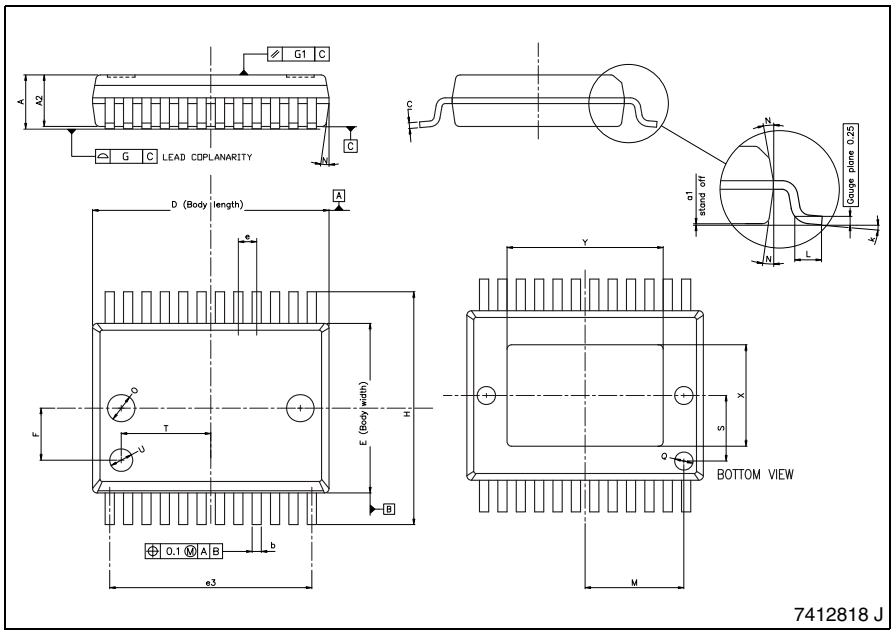
Dim.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			2.45			0.0965
A2	2.15		2.35	0.084		0.0925
a1	0		0.10	0		0.003
b	0.33		0.51	0.013		0.020
c	0.23		0.32	0.009		0.012
D (1)	10.10		10.50	0.398		0.413
E (1)	7.40		7.60	0.291		0.299
e0		.80			0.031	
e3		8.80			0.346	
F2		.30			0.090	
G			0.10			0.004
G1			0.06			0.002
H	10.10		10.50	0.398		0.413
h			0.40			0.016
k	0° (min.), 8° (max.)					
L	0.55		0.85	0.0217		0.0335
O		1.20				0.047
Q		0.80				0.031
S		2.90				0.114
T		3.65				0.143
U		1.0				0.039
N	10° (max)					
X	4.10		4.70	0.161		0.185
Y	6.50 4.90(4)		7.10 5.50(4)	0.256 0.192(4)		0.279 0.216(4)

(1) "D and E1" do not include mold flash or protusions.
Mold flash or protusions shall not exceed 0.15mm (0.006")
(2) No intrusion allowed inwards the leads.
(3) Flash or bleeds on exposed die pad shall not exceed 0.4 mm per side
(4) Variation for small window leadframe option.

OUTLINE AND MECHANICAL DAT A



PowerSSO24 (Exposed pad down)



9 Revision history

Table 28. Document revision history

Date	Revision	Changes
16-Mar-2010	1	Initial release.
08-Apr-2011	2	Updated *Table 27: Timing characteristics on page 32* (Pos. 10.8).
03-Aug-2011	3	Updated *Table 17*, *Table 20*, *Table 24* and *Table 27*.
23-Mar-2012	4	Updated: *Table 17: Range of functionality*; *Table 20: SPI*.
19-Sep-2013	5	Updated disclaimer.
05-Dec-2013	6	Updated *Table 24: Current limitation and over-current detection* pag 31.

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