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# 1 Electrical data

## 1.1 Absolute maximum ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_S$	Supply voltage	36	V
$V_{SS}$	Logic supply voltage	36	V
$V_i$	Input voltage	7	V
$V_{en}$	Enable voltage	7	V
$I_o$	Peak output current (100 $\mu$ s non repetitive)	1.2	A
$P_{tot}$	Total power dissipation at $T_{pins} = 90\text{ }^{\circ}\text{C}$	4	W
$T_J$	Junction temperature	150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature	– 40 to 150	$^{\circ}\text{C}$

## 1.2 Recommended conditions

**Table 2. Recommended conditions**

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
$V_S$	Supply voltage	$V_{SS}$		36	V
$V_{SS}$	Logic supply voltage	2.8 <sup>(1)</sup>		36	V
$T_J$	Junction temperature	-20 <sup>(1)</sup>		125	$^{\circ}\text{C}$

1. See [Figure 2](#)

1.3 Thermal data

Figure 2. Typical minimum logic supply voltage vs junction temperature

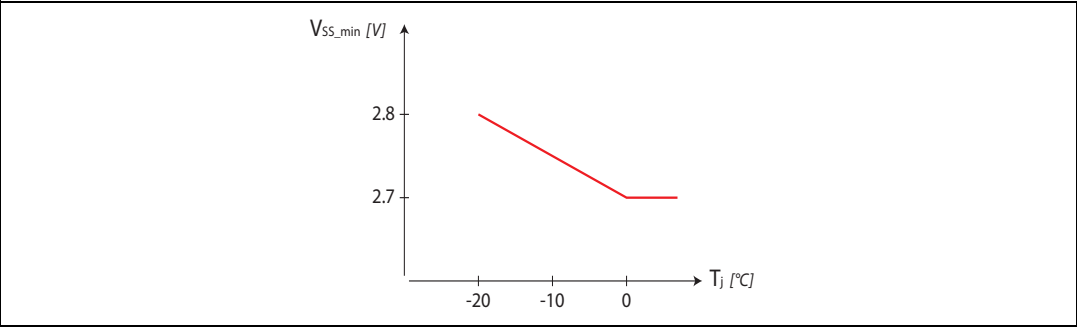


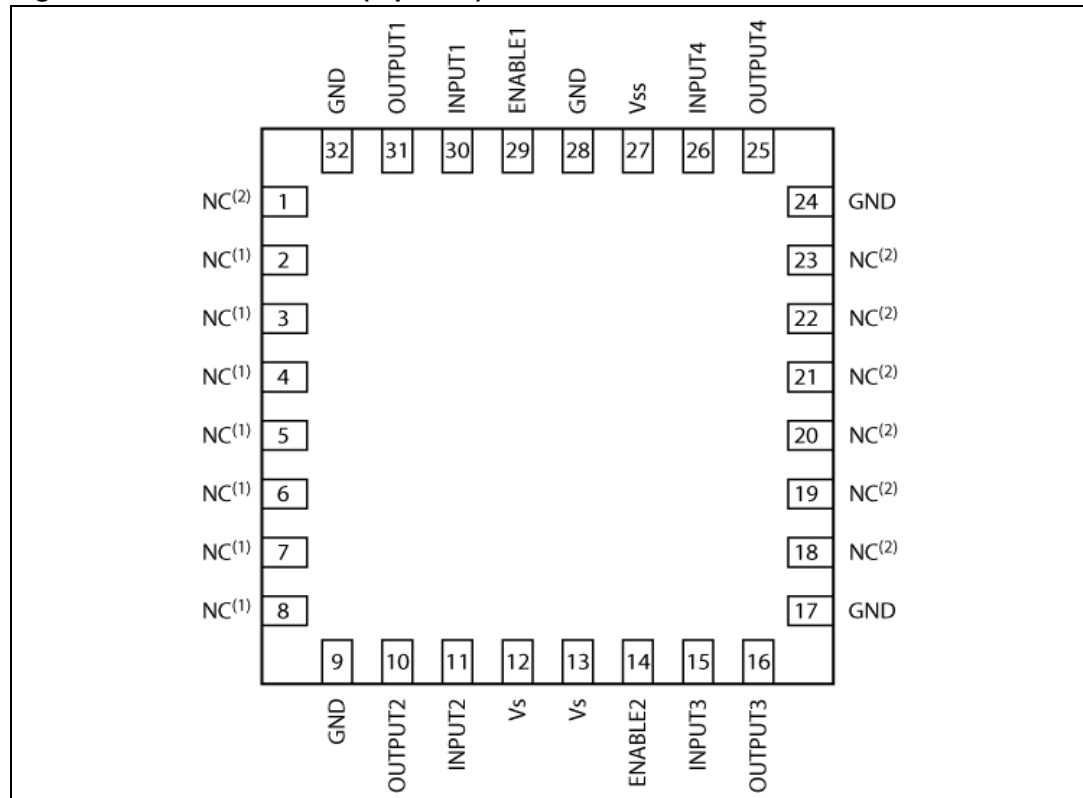
Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction-ambient max. <sup>(1)</sup>	42	$^{\circ}C/W$

1. Mounted on a double-layer FR4 PCB with a dissipating copper surface of 0.5 cm<sup>2</sup> on the top side plus 6 cm<sup>2</sup> ground layer connected through 18 via holes (9 below the IC).

## 2 Pin connection

Figure 2. Pin connection (top view)



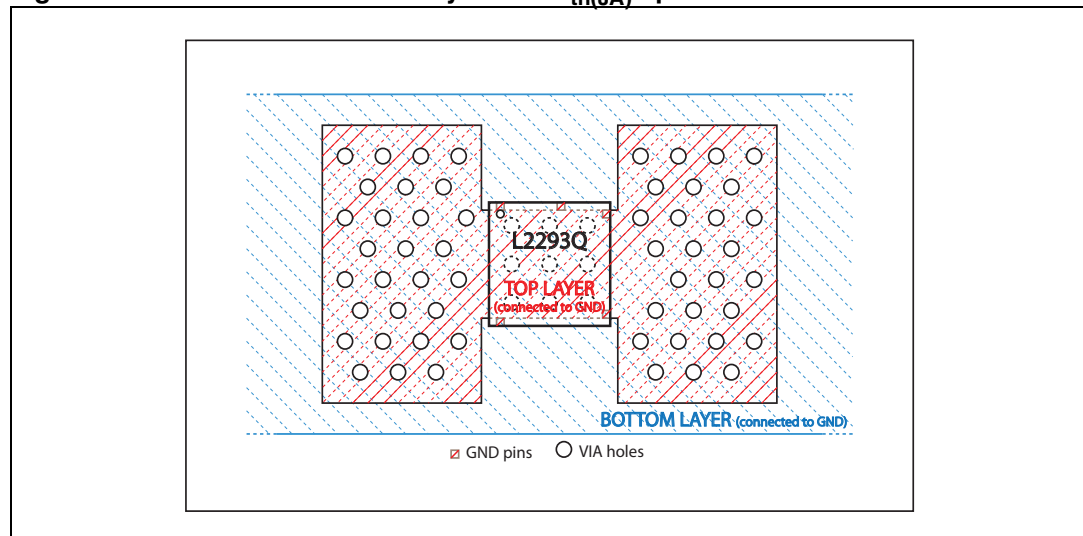
Note:

*NC<sup>(1)</sup> These NC pins are connected to the exposed PAD.*

*The exposed PAD must be connected to GND pins.*

*NC<sup>(2)</sup> These NC pins can be connected to GND pins and exposed PAD.*

Figure 3. Recommended PCB layout for  $R_{th(JA)}$  optimization



**Table 4. Pin description**

Pin n°	Name	Type	Function
1, 18, 19, 20, 21, 22, 23	NC		Not connected
2, 3, 4, 5, 6, 7,	NC		Pins connected to the exposed PAD
8, 9, 17, 24, 28, 32	GND		Ground
10	OUTPUT2	O	Output 2
11	INPUT2	I	Input 2
12, 13	V <sub>S</sub>		Supply voltage for the power output stages. A non-inductive 100 nF capacitor must be connected between these pins and ground.
14	ENABLE2	I	Enable 2 input, the LOW state disables the Output 3 and Output 4.
15	INPUT3	I	Input 3
16	OUTPUT3	O	Output 3
25	OUTPUT4	O	Output 4
26	INPUT4	I	Input 4
27	V <sub>SS</sub>		Supply voltage for the logic blocks. A 100 nF capacitor must be connected between this pin and ground.
29	ENABLE1	I	Enable 1 input, the LOW state disables the output 1 and Output 2.
30	INPUT1	I	Input 1
31	OUTPUT1	O	Output 1

### 3 Electrical characteristics

For each channel,  $V_S = 24\text{ V}$ ,  $V_{SS} = 5\text{ V}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

**Table 5. Electrical characteristics**

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
$I_S$	12, 13	Total quiescent supply current	$V_i = L; I_O = 0; V_{en} = H$		2	6	mA
			$V_i = H; I_O = 0; V_{en} = H$		16	24	mA
			$V_{en} = L$			4	mA
$I_{SS}$	27	Total quiescent logic supply current	$V_i = L; I_O = 0; V_{en} = H$		44	60	mA
			$V_i = H; I_O = 0; V_{en} = H$		16	22	mA
			$V_{en} = L$		16	24	mA
$V_{IL}$	11, 15, 26, 30	Input low voltage		-0.3		1.5	V
$V_{IH}$	11, 15, 26, 30	Input high voltage	$V_{SS} \leq 7\text{ V}$	2.3		$V_{SS}$	V
			$V_{SS} > 7\text{ V}$	2.3		7	V
$I_{IL}$	11, 15, 26, 30	Low voltage input current	$V_{IL} = 1.5\text{ V}$			-10	$\mu\text{A}$
$I_{IH}$	11, 15, 26, 30	High voltage input current	$2.3\text{ V} \leq V_{IH} \leq V_{SS} - 0.6\text{ V}$		30	100	$\mu\text{A}$
$V_{en L}$	14, 29	Enable low voltage		-0.3		1.5	V
$V_{en H}$	14, 29	Enable high voltage	$V_{SS} \leq 7\text{ V}$	2.3		$V_{SS}$	V
			$V_{SS} > 7\text{ V}$	2.3		7	V
$I_{en L}$	14, 29	Low voltage enable current	$V_{en L} = 1.5\text{ V}$		-30	-100	$\mu\text{A}$
$I_{en H}$	14, 29	High voltage enable current	$2.3\text{ V} \leq V_{en H} \leq V_{SS} - 0.6\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{CE(sat)H}$	10, 16, 25, 31	Source output saturation voltage	$I_O = -0.6\text{ A}$		1.4	1.8	V
$V_{CE(sat)L}$	10, 16, 25, 31	Sink output saturation voltage	$I_O = +0.6\text{ A}$		1.2	1.8	V
$V_F$		Clamp diode forward voltage	$I_O = 600\text{ nA}$		1.3		V

$V_S = 24\text{ V}$ ,  $V_{SS} = 5\text{ V}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ , unless otherwise specified.

Table 6. AC operation

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$t_r$	Rise time <sup>(1)</sup>	0.1 to 0.9 $V_O$		250		ns
$t_f$	Fall time <sup>(1)</sup>	0.9 to 0.1 $V_O$		250		ns
$t_{on}$	Turn-on delay <sup>(1)</sup>	0.5 $V_i$ to 0.5 $V_O$		750		ns
$t_{off}$	Turn-off delay <sup>(1)</sup>	0.5 $V_i$ to 0.5 $V_O$		200		ns

1. See [Figure 4](#)

Figure 4. Switching times

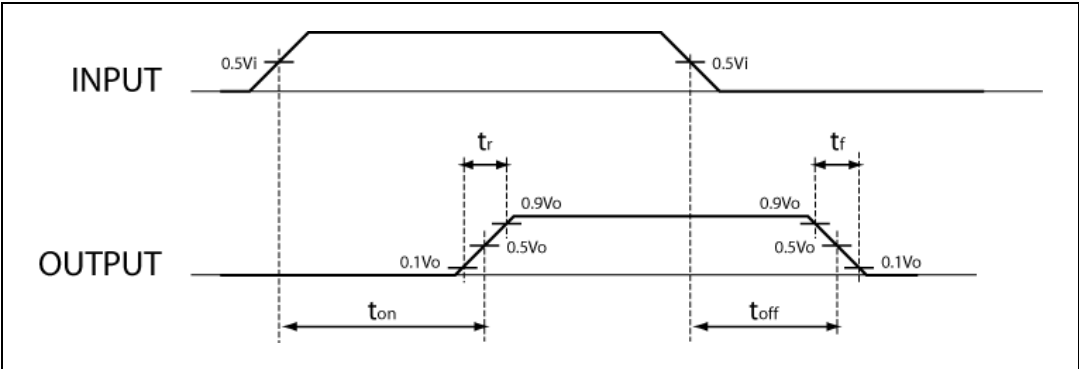


Table 7. Truth table (one channel)

Input	Enable <sup>(1)</sup>	Output
H	H	H
L	H	L
H	L	Z <sup>(2)</sup>
L	L	Z <sup>(2)</sup>

1. Relative to the considered channel  
2. Z = High output impedance

## 4 Package mechanical data

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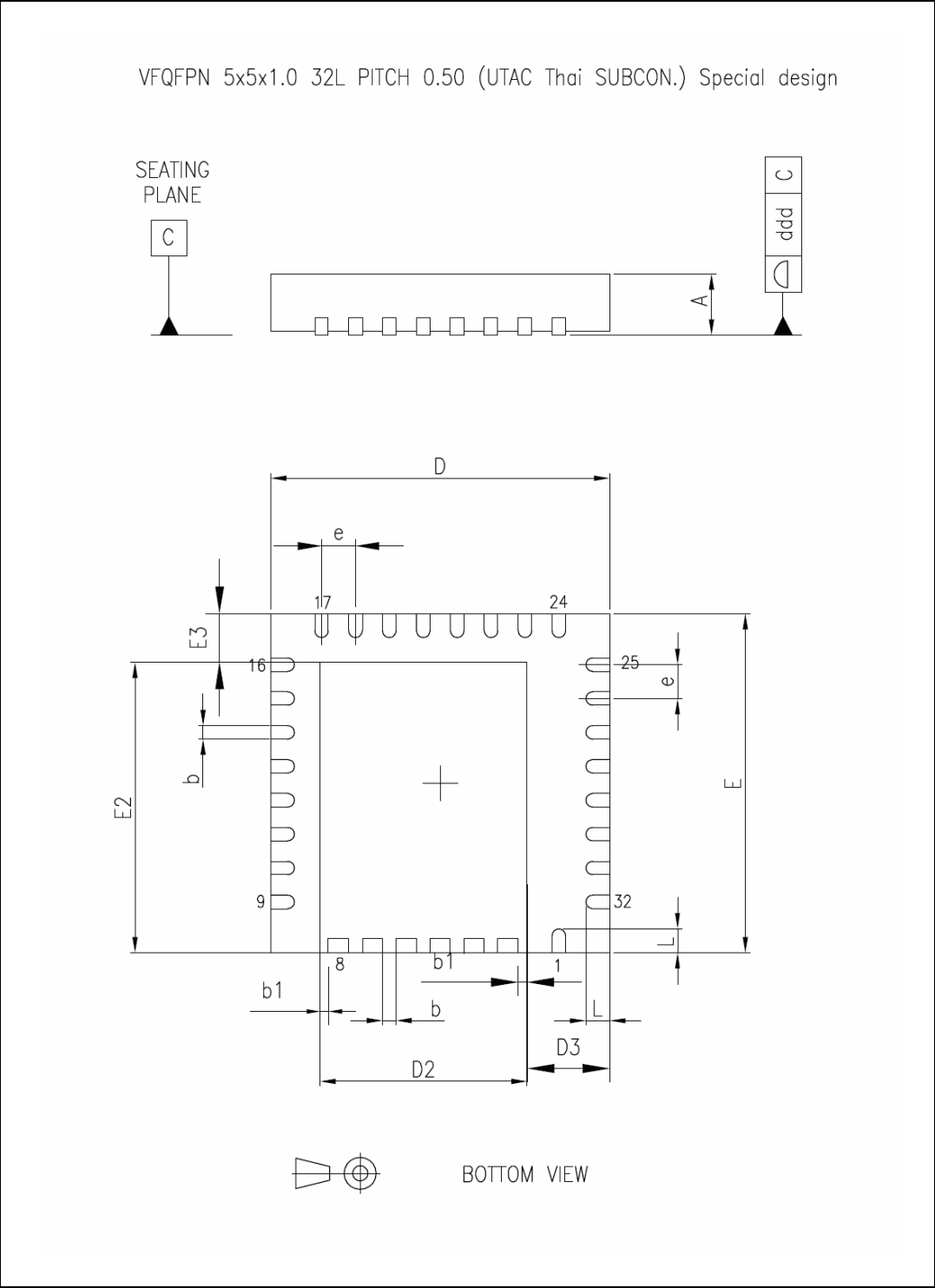
**Table 8. VFQFPN 5x5x1.0 32L pitch 0.50**

Dim.	Databook (mm)		
	Min	Typ	Max
A	0.80	0.85	0.95
b	0.18	0.25	0.30
b1	0.165	0.175	0.185
D	4.85	5.00	5.15
D2	3.00	3.10	3.20
D3	1.10	1.20	1.30
E	4.85	5.00	5.15
E2	4.20	4.30	4.40
E3	0.60	0.70	0.80
e		0.50	
L	0.30	0.40	0.50
ddd			0.08

- Note:**
- 1 VFQFPN stands for thermally enhanced very thin profile fine pitch quad flat package no lead. Very thin profile:  $0.80 < A \leq 1.00$  mm.
  - 2 Details of terminal 1 are optional but must be located on the top surface of the package by using either a mold or marked features.



Figure 5. Package dimensions



## 5 Order codes

**Table 9. Order code**

Order code	Package	Packaging
L2293Q	VFQFPN 5x5x1.0 32L	Tube

## 6 Revision history

**Table 10. Document revision history**

Date	Revision	Changes
10-Jul-2008	1	First release
26-Feb-2009	2	Updated <a href="#">Table 3 on page 4</a>
12-Aug-2009	3	Updated description in coverpage

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