

Figure 1. 8/20 us pulse waveform according to IEC 61000-4-5

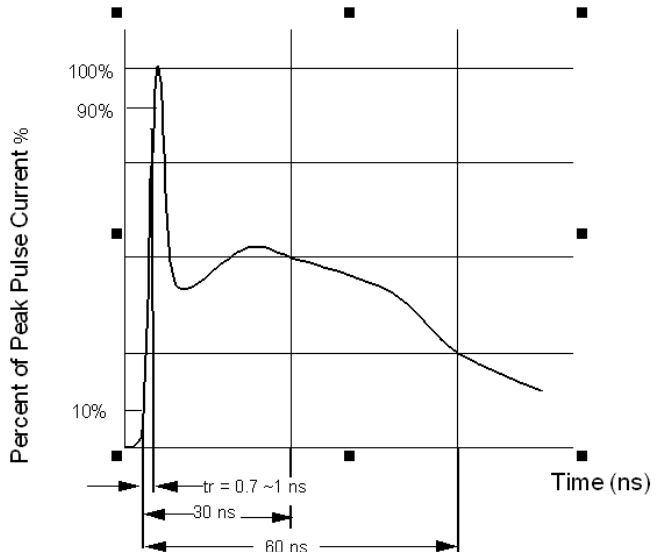


Figure 2. ESD pulse waveform according to IEC 61000-4-2

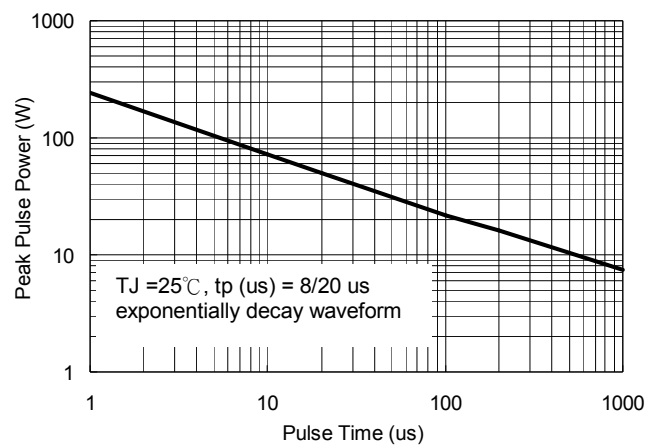


Figure 3. Power Dissipation versus Pulse Time

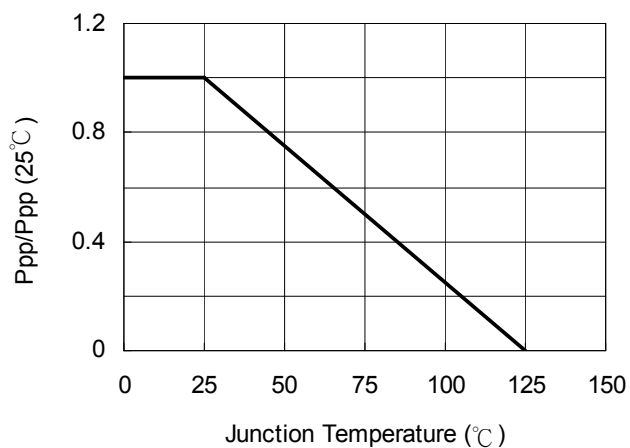


Figure 4. Peak pulse power versus T_J

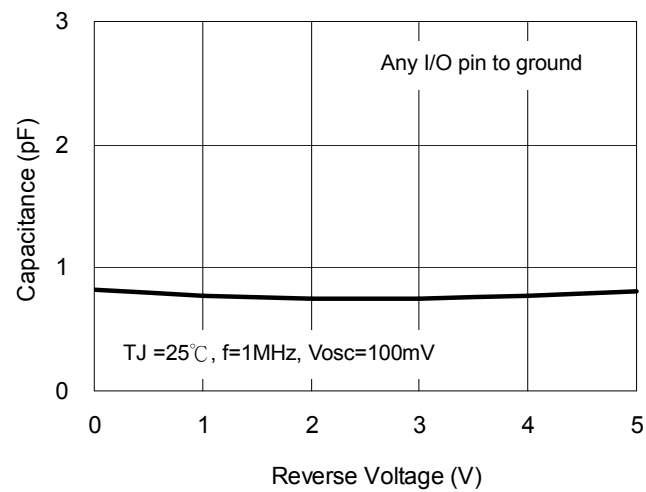


Figure 5. Typical Junction Capacitance

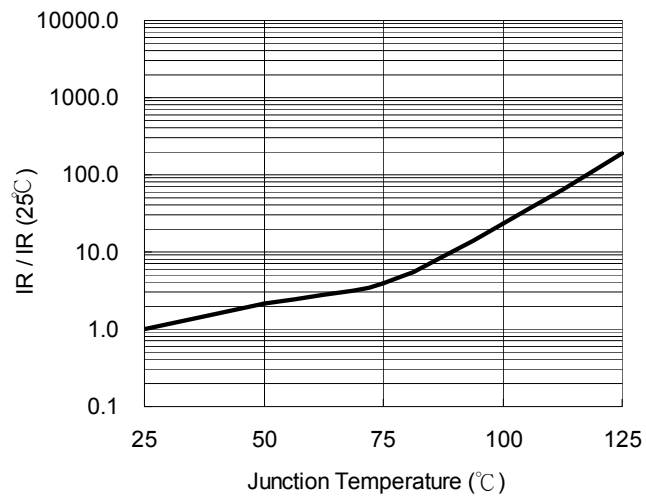


Figure 6. Reverse Leakage Current versus T_J

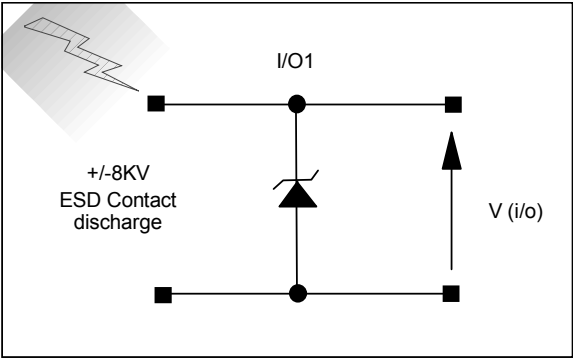


Figure 7. ESD Test Configuration

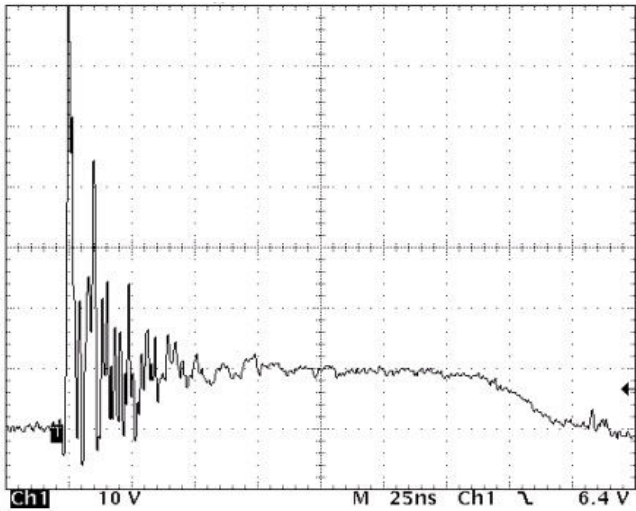


Figure 8. Clamped +8 kV ESD voltage waveform

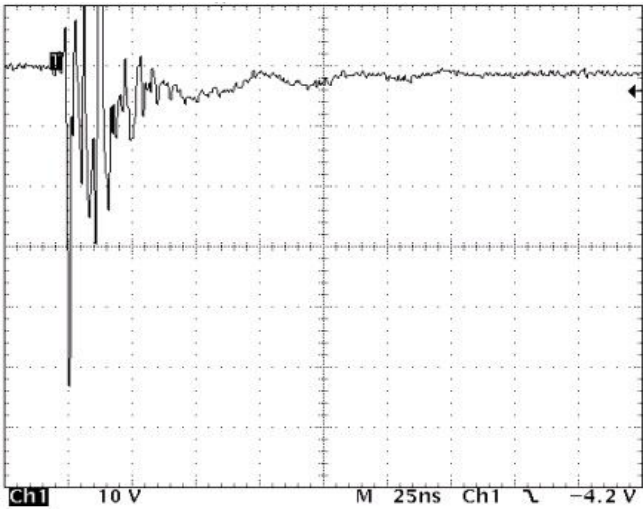


Figure 9. Clamped -8 kV ESD voltage waveform

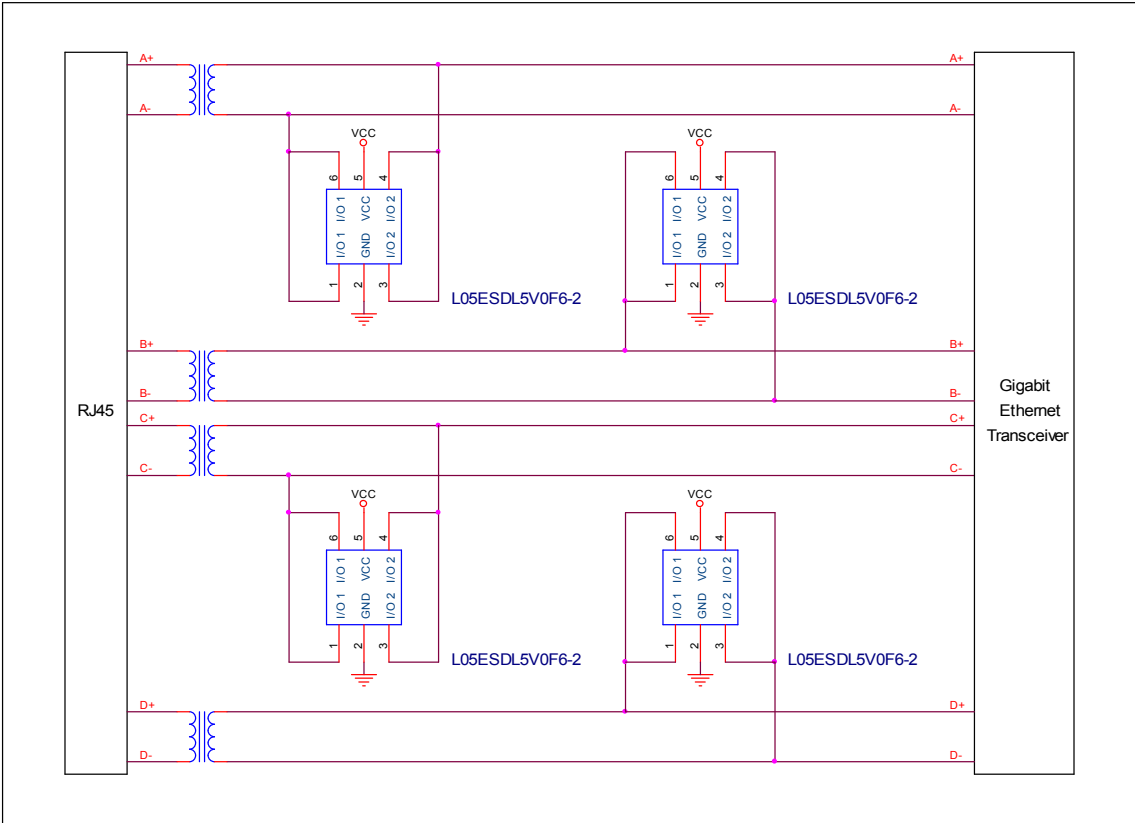


Figure 10. 10/100/1000 Ethernet ESD Protection

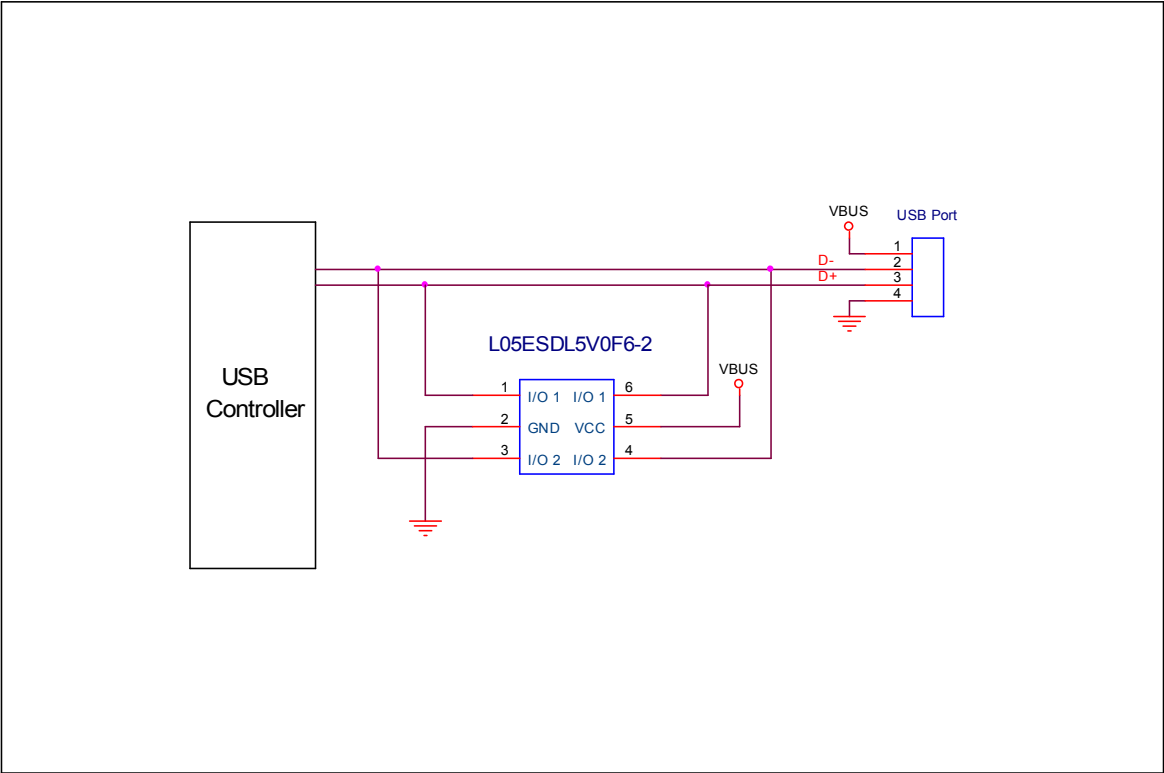


Figure 11. USB2.0 Interface ESD Protection

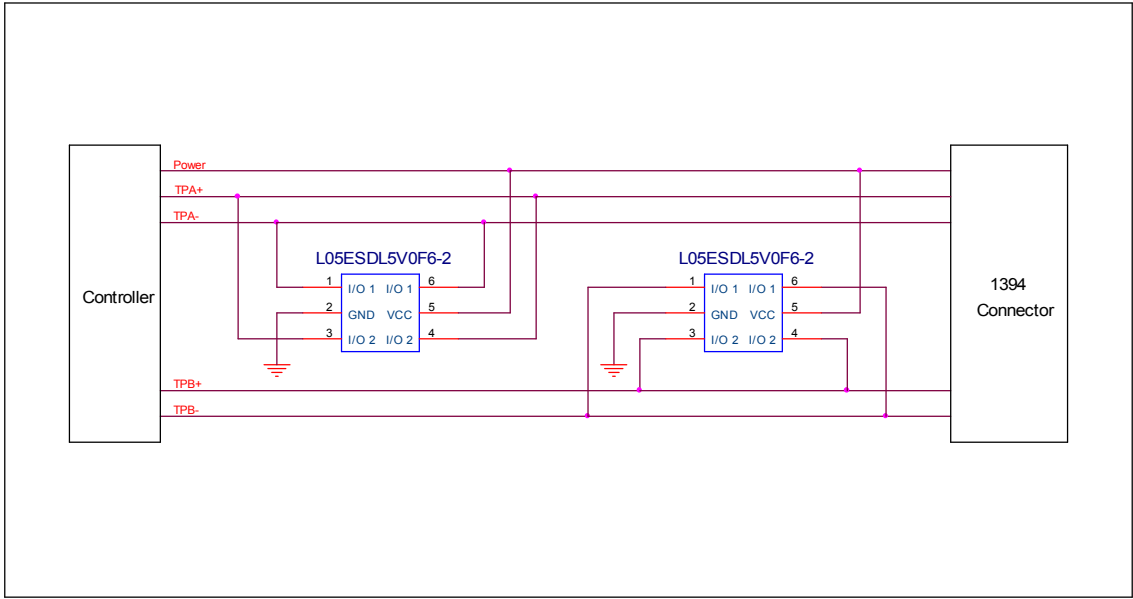
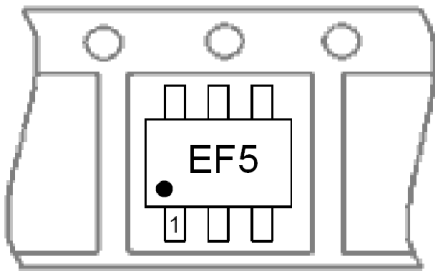


Figure 12. IEEE1394 Interface ESD Protection

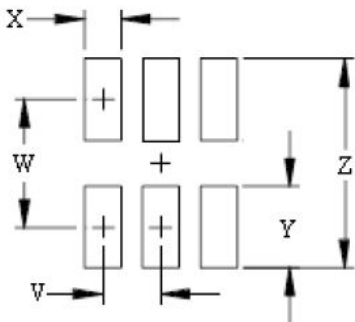
Marking & Orientation



Packaging Information

DEVICE	Q'TY/REEL (PCS)	REEL DIA. (INCH)	Q'TY/BOX (PCS)	Q'TY/CARTON (PCS)
L05ESDL5V0F6-2	3000	7	45000	90K/180K

SOT-563 Soldering Pad Layout



Dim.	Millimeters	Inches
Z	2.30	0.090
X	0.30	0.011
W	1.45	0.057
Y	0.85	0.033
V	0.50	0.019

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