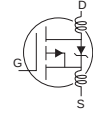


Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	—	—	V	$V_{GS} = 0V$, $I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.034	—	$V/^\circ\text{C}$	Reference to 25°C , $I_D = -1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.065	Ω	$V_{GS} = -10V$, $I_D = -16A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}$, $I_D = -250\mu A$
g_{fs}	Forward Transconductance	8.0	—	—	S	$V_{DS} = -25V$, $I_D = -16A$ ⑥
I_{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	$V_{DS} = -55V$, $V_{GS} = 0V$
		—	—	-250		$V_{DS} = -44V$, $V_{GS} = 0V$, $T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	63	nC	$I_D = -16A$
Q_{gs}	Gate-to-Source Charge	—	—	13		$V_{DS} = -44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	29		$V_{GS} = -10V$, See Fig. 6 and 13 ④ ⑥
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD} = -28V$
t_r	Rise Time	—	66	—		$I_D = -16A$
$t_{d(off)}$	Turn-Off Delay Time	—	39	—		$R_G = 6.8\Omega$
t_f	Fall Time	—	63	—		$R_D = 1.6\Omega$, See Fig. 10 ④ ⑥
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact ⑤
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1200	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	520	—		$V_{DS} = -25V$
C_{rss}	Reverse Transfer Capacitance	—	250	—		$f = 1.0MHz$, See Fig. 5 ⑥



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-31	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	-110		
V_{SD}	Diode Forward Voltage	—	—	-1.3	V	$T_J = 25^\circ\text{C}$, $I_S = -16A$, $V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	71	110	ns	$T_J = 25^\circ\text{C}$, $I_F = -16A$
Q_{rr}	Reverse Recovery Charge	—	170	250	nC	$di/dt = -100A/\mu s$ ④ ⑥

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② $V_{DD} = -25V$, starting $T_J = 25^\circ\text{C}$, $L = 2.1mH$, $R_G = 25\Omega$, $I_{AS} = -16A$. (See Figure 12)
- ③ $I_{SD} \leq -16A$, $di/dt \leq -280A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact.

⑥ Uses IRF5305 data and test conditions.

* When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

** Uses typical socket mount.

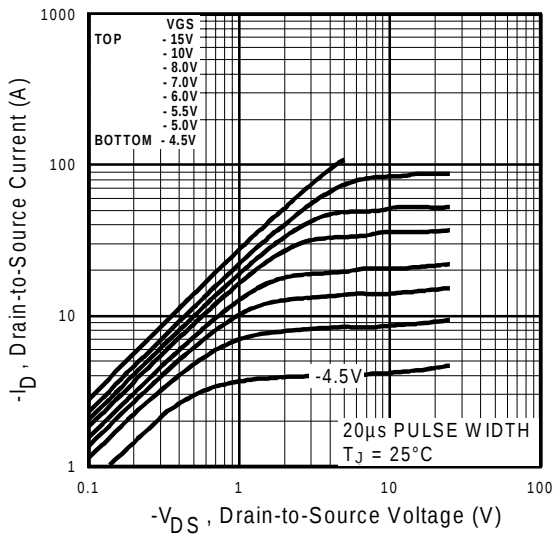


Fig 1. Typical Output Characteristics

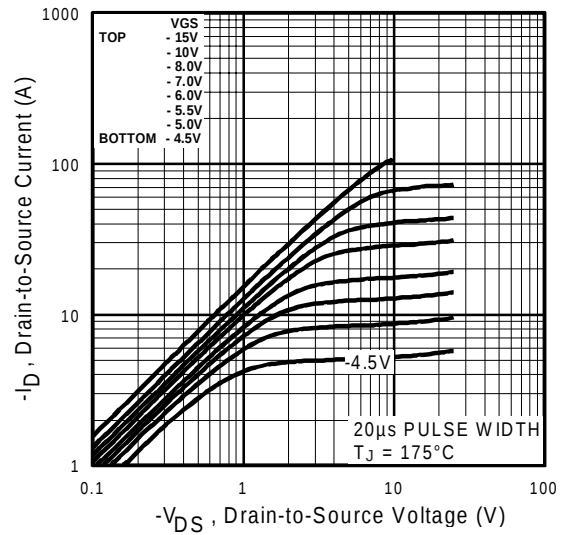


Fig 2. Typical Output Characteristics

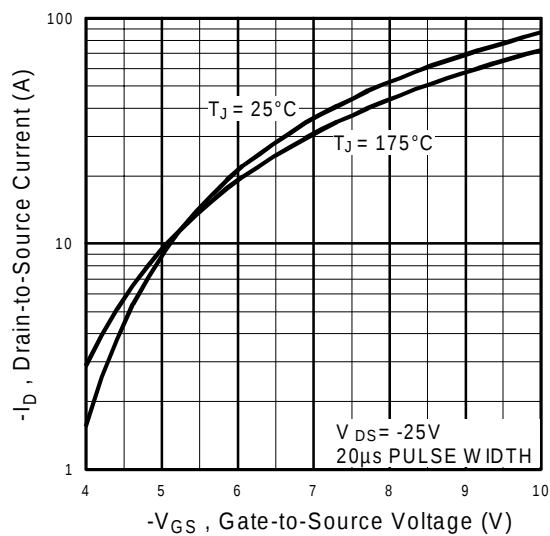


Fig 3. Typical Transfer Characteristics

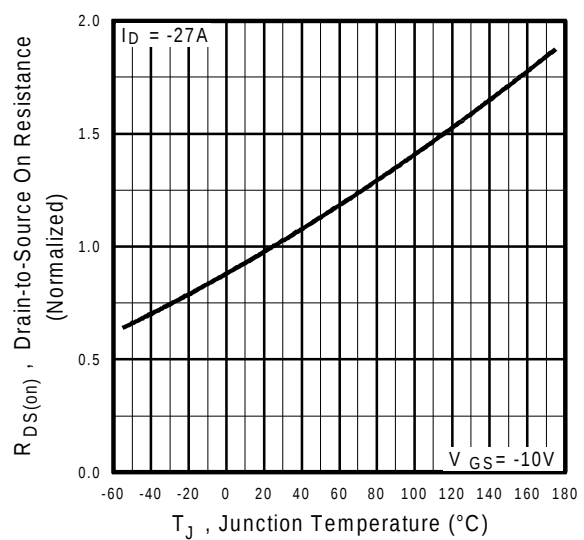


Fig 4. Normalized On-Resistance Vs. Temperature

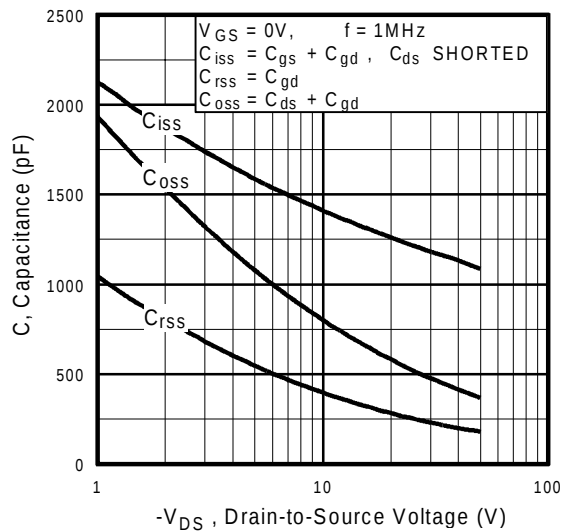


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

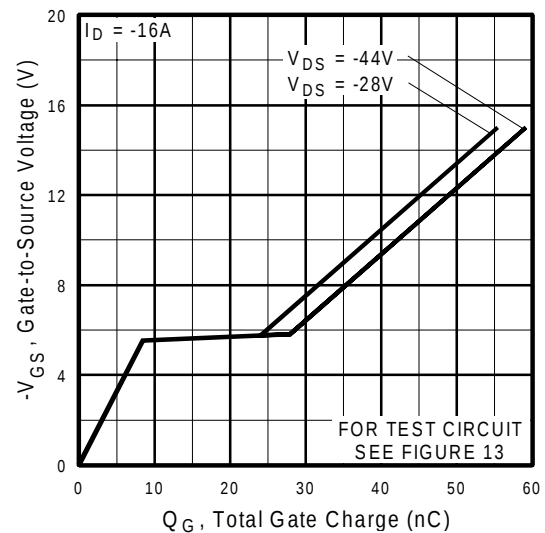


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

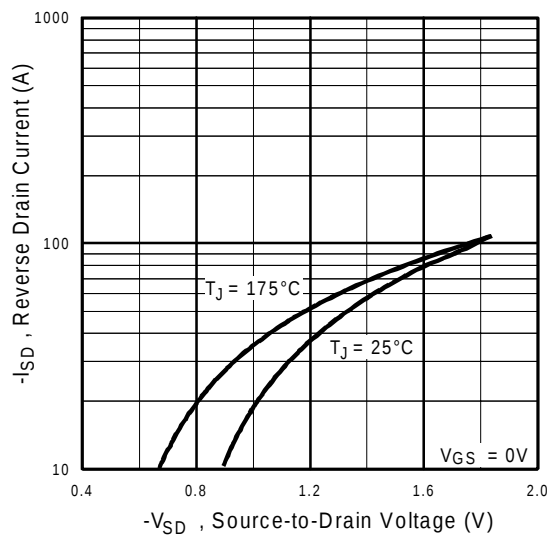


Fig 7. Typical Source-Drain Diode Forward Voltage

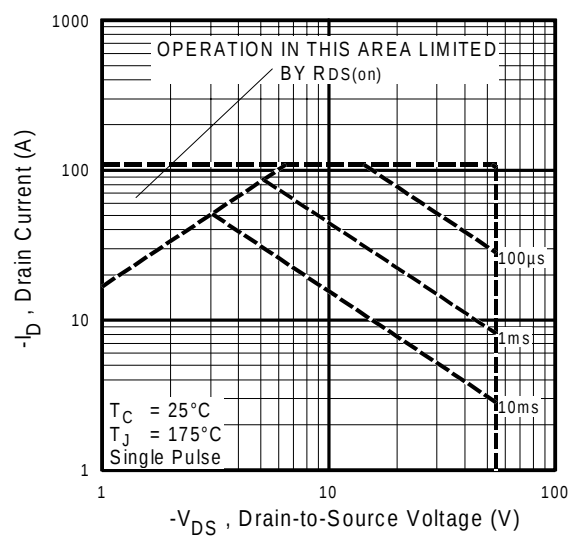


Fig 8. Maximum Safe Operating Area

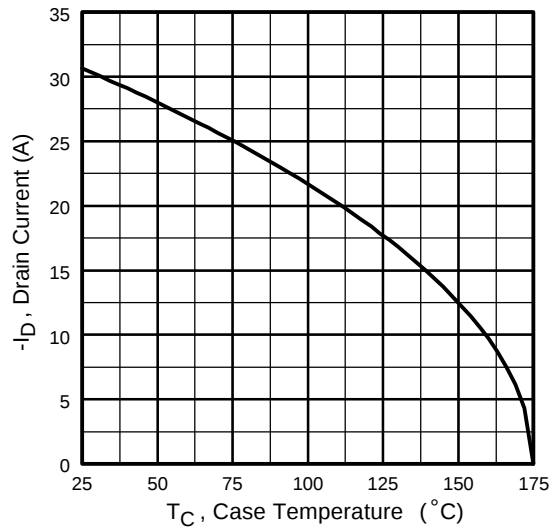


Fig 9. Maximum Drain Current Vs. Case Temperature

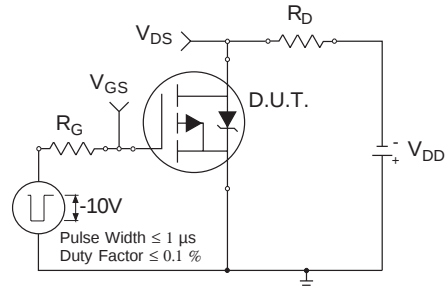


Fig 10a. Switching Time Test Circuit

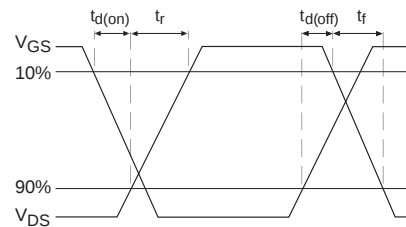


Fig 10b. Switching Time Waveforms

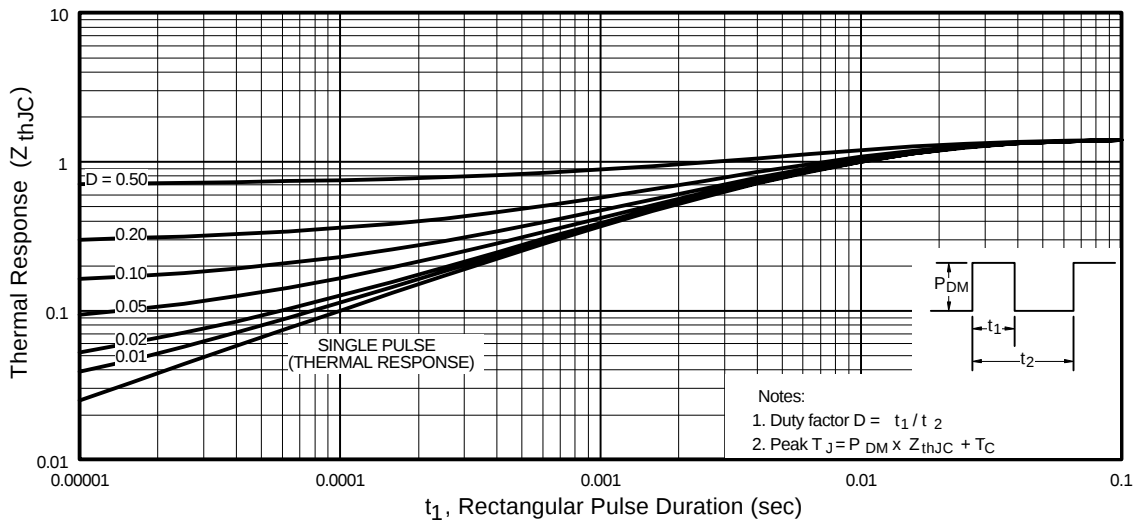


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

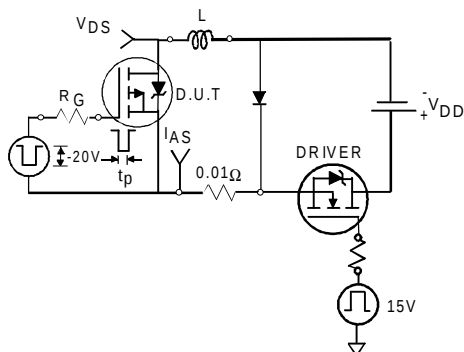


Fig 12a. Unclamped Inductive Test Circuit

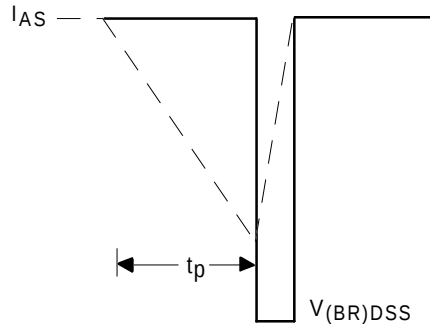


Fig 12b. Unclamped Inductive Waveforms

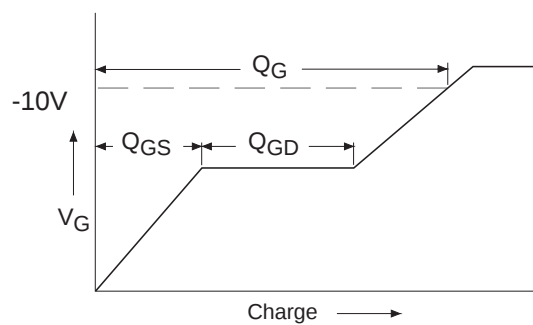


Fig 13a. Basic Gate Charge Waveform

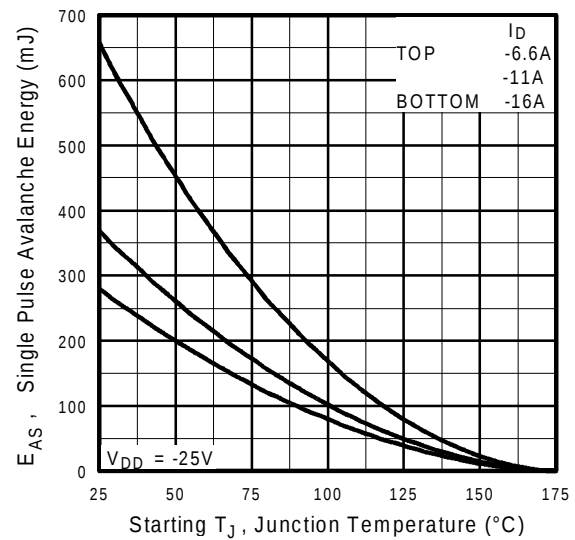


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

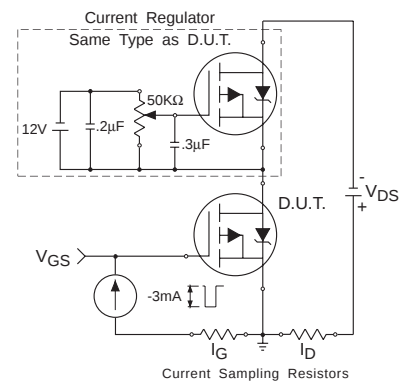
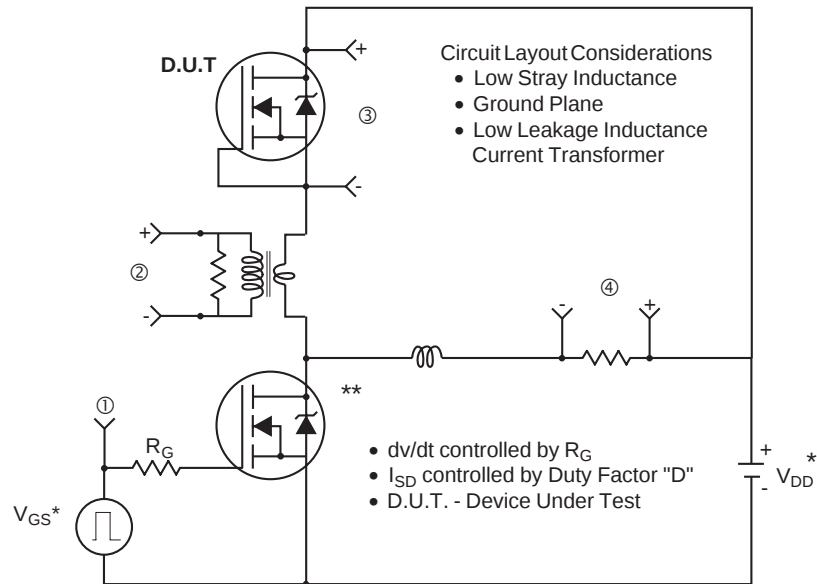


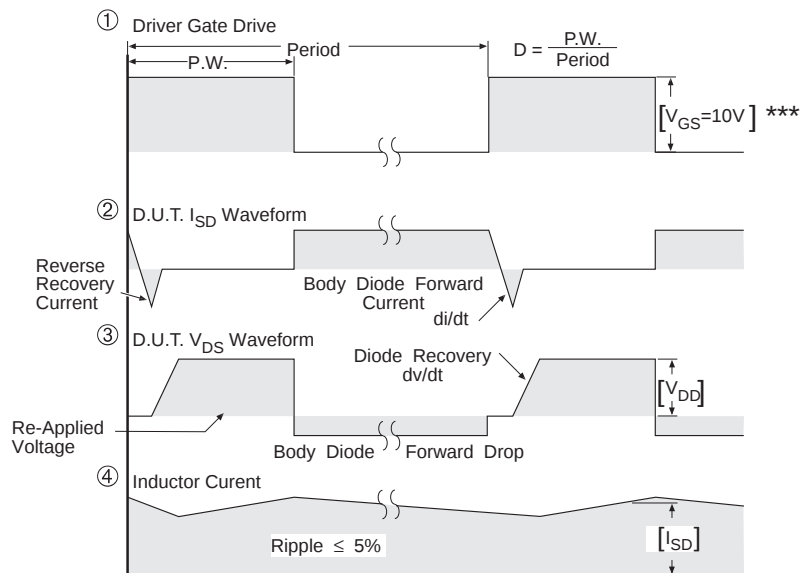
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

**** Use P-Channel Driver for P-Channel Measurements**

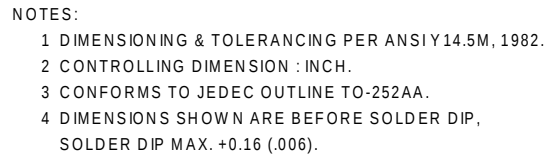


*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

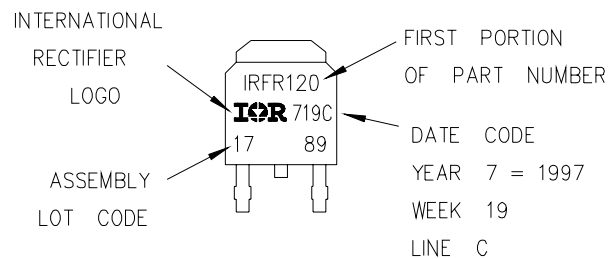
Fig 14. For P-Channel HEXFETS

International
IOR Rectifier

Dimensions are shown in millimeters (inches)

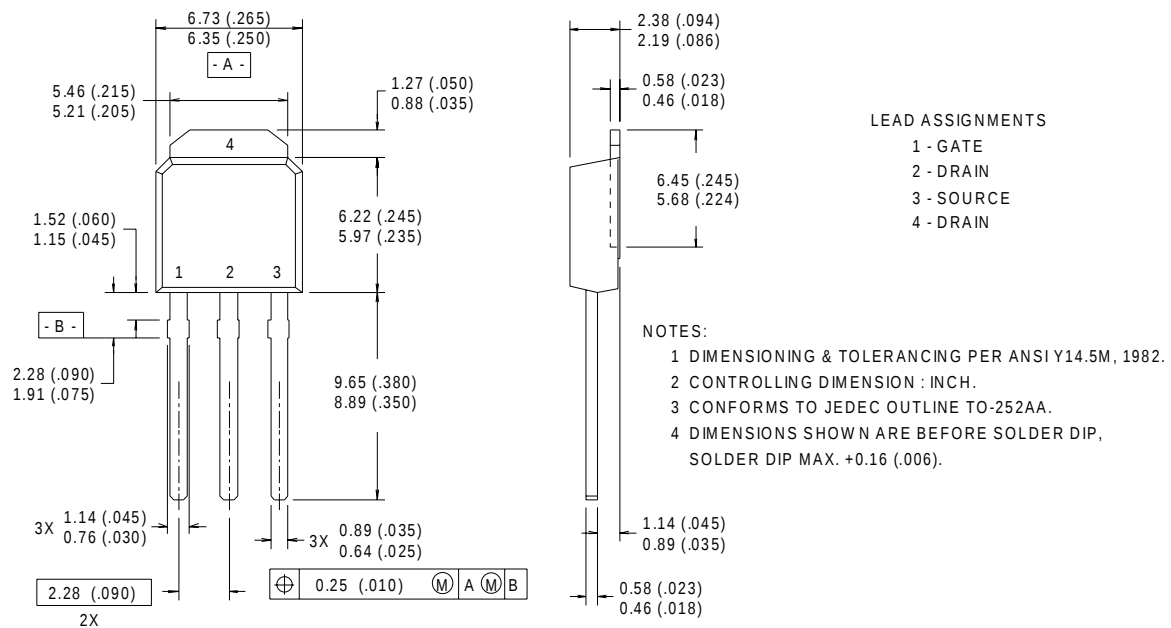


EXAMPLE: THIS IS AN IRFR120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



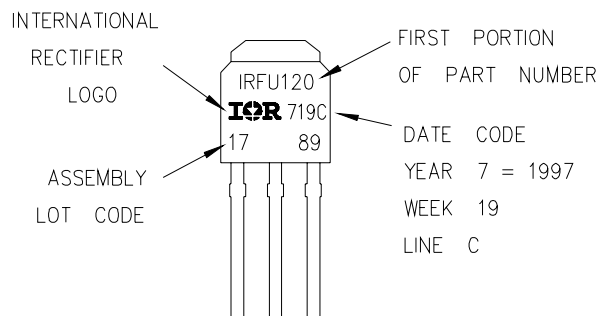
I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



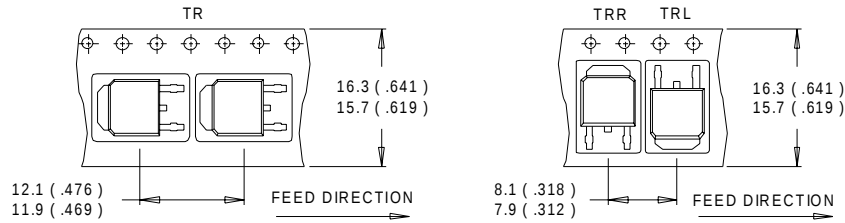
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



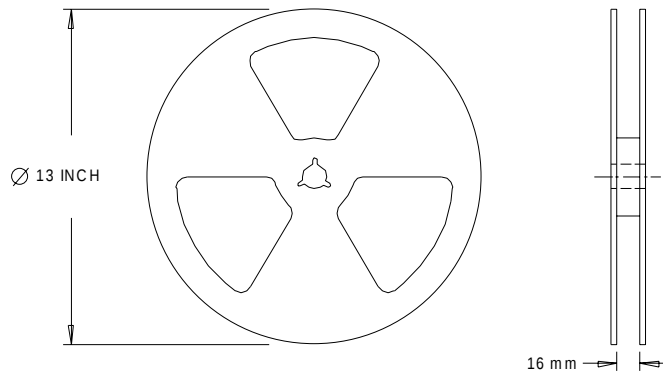
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>