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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	17 10.6	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	45	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	43	mJ	$I_D=2.2\text{A}$; $V_{DD}=50\text{V}$
Avalanche energy, repetitive	E_{AR}	-	-	0.36	mJ	$I_D=2.2\text{A}$; $V_{DD}=50\text{V}$
Avalanche current, repetitive	I_{AR}	-	-	2.2	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0$ to 400V
Gate source voltage	V_{GS}	-20 -30	-	20 30	V	static; AC ($f > 1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	30	W	$T_C=25^\circ\text{C}$
Operating and storage temperature	T_j, T_{stg}	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screw
Continuous diode forward current	I_S	-	-	7	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	45	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	1	V/ns	$V_{DS}=0$ to 400V, $I_{SD} \leq 3.6\text{A}$, $T_j=25^\circ\text{C}$
Maximum diode commutation speed ³⁾	di/dt	-	-	50	A/ μs	$V_{DS}=0$ to 400V, $I_{SD} \leq 3.6\text{A}$, $T_j=25^\circ\text{C}$
Insulation withstand voltage	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	4.1	$^\circ\text{C/W}$	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	$^\circ\text{C/W}$	lead
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	$^\circ\text{C/W}$	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sld}	-	-	260	$^\circ\text{C}$	1.6 mm (0.063 in.) from case for 10s

¹⁾ TO220 equivalent. Limited by $T_{j,max}$. Maximum duty cycle $D=0.5$

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ $V_{DClk}=400\text{V}$; $V_{DS,peak} < V_{(BR)DSS}$; identical low side and high side switch with identical R_G ; $t_{cond} < 2\mu\text{s}$

3 Electrical characteristics

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	800	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{GS(th)}$	2.5	3	3.5	V	$V_{DS}=V_{GS}$, $I_D=0.36mA$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=800V$, $V_{GS}=0V$, $T_j=25^\circ\text{C}$ $V_{DS}=800V$, $V_{GS}=0V$, $T_j=150^\circ\text{C}$
Gate-source leakage current incl. zener diode	I_{GSS}	-	-	1	μA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.24 0.62	0.28 -	Ω	$V_{GS}=10V$, $I_D=7.2A$, $T_j=25^\circ\text{C}$ $V_{GS}=10V$, $I_D=7.2A$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	1	-	Ω	$f=250kHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1200	-	pF	$V_{GS}=0V$, $V_{DS}=500V$, $f=250kHz$
Output capacitance	C_{oss}	-	20	-	pF	$V_{GS}=0V$, $V_{DS}=500V$, $f=250kHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	38	-	pF	$V_{GS}=0V$, $V_{DS}=0$ to $500V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	490	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0$ to $500V$
Turn-on delay time	$t_{d(on)}$	-	10	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=7.2A$, $R_G=4.7\Omega$
Rise time	t_r	-	6	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=7.2A$, $R_G=4.7\Omega$
Turn-off delay time	$t_{d(off)}$	-	40	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=7.2A$, $R_G=4.7\Omega$
Fall time	t_f	-	5	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=7.2A$, $R_G=4.7\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	5	-	nC	$V_{DD}=640V$, $I_D=7.2A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	15	-	nC	$V_{DD}=640V$, $I_D=7.2A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	36	-	nC	$V_{DD}=640V$, $I_D=7.2A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	4.5	-	V	$V_{DD}=640V$, $I_D=7.2A$, $V_{GS}=0$ to $10V$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 500V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 500V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=7.2A, T_f=25^{\circ}C$
Reverse recovery time	t_{rr}	-	1200	-	ns	$V_R=400V, I_F=3.6A, di_F/dt=50A/\mu s$
Reverse recovery charge	Q_{rr}	-	15	-	μC	$V_R=400V, I_F=3.6A, di_F/dt=50A/\mu s$
Peak reverse recovery current	I_{rrm}	-	24	-	A	$V_R=400V, I_F=3.6A, di_F/dt=50A/\mu s$

4 Electrical characteristics diagrams

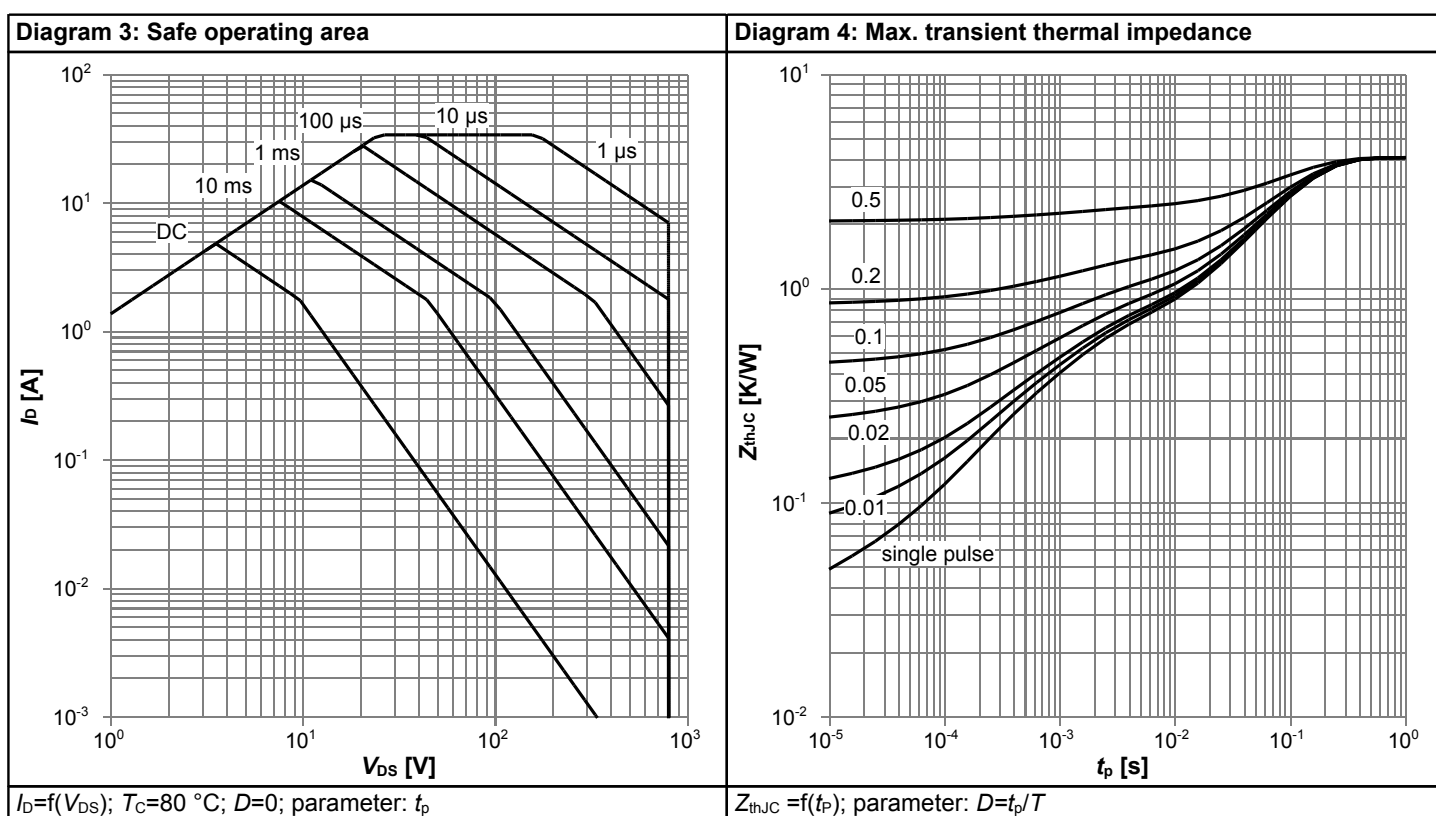
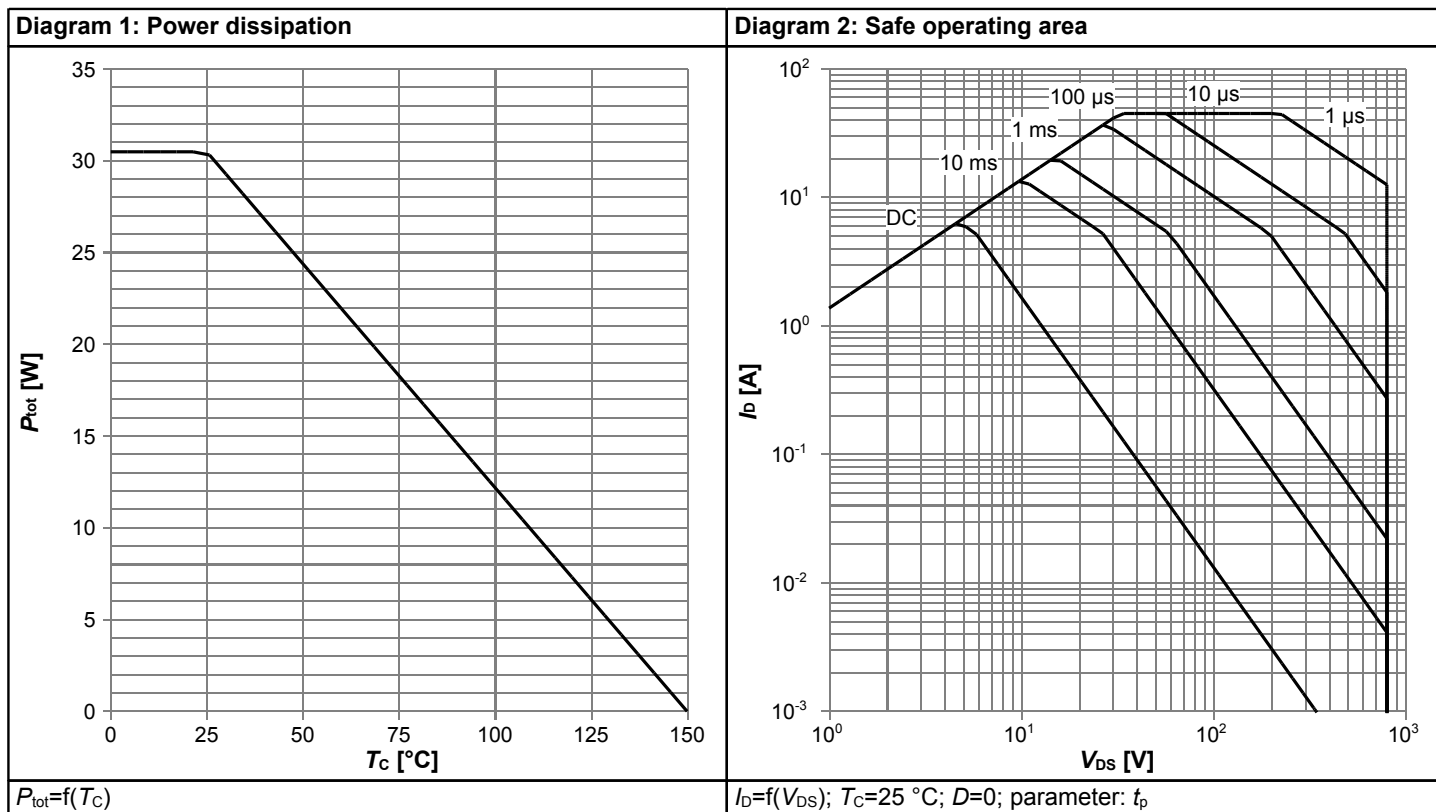
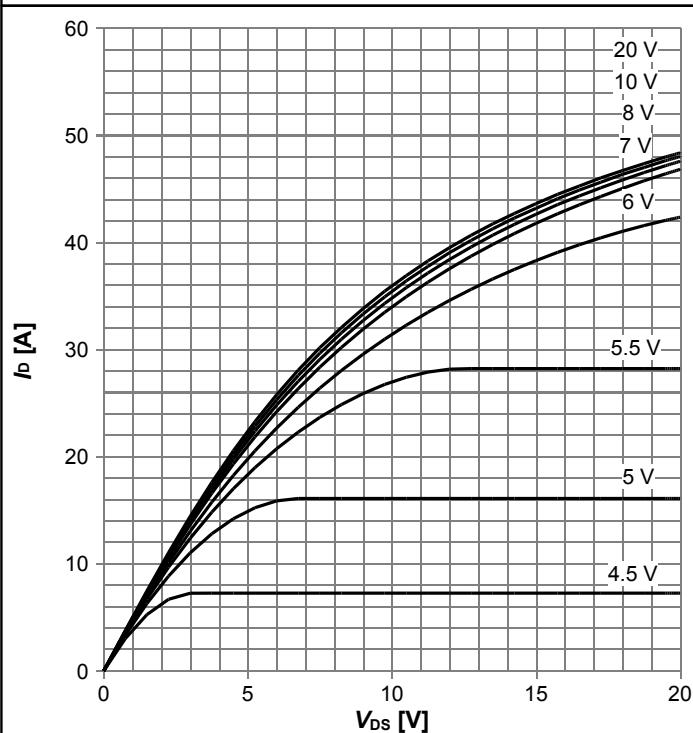
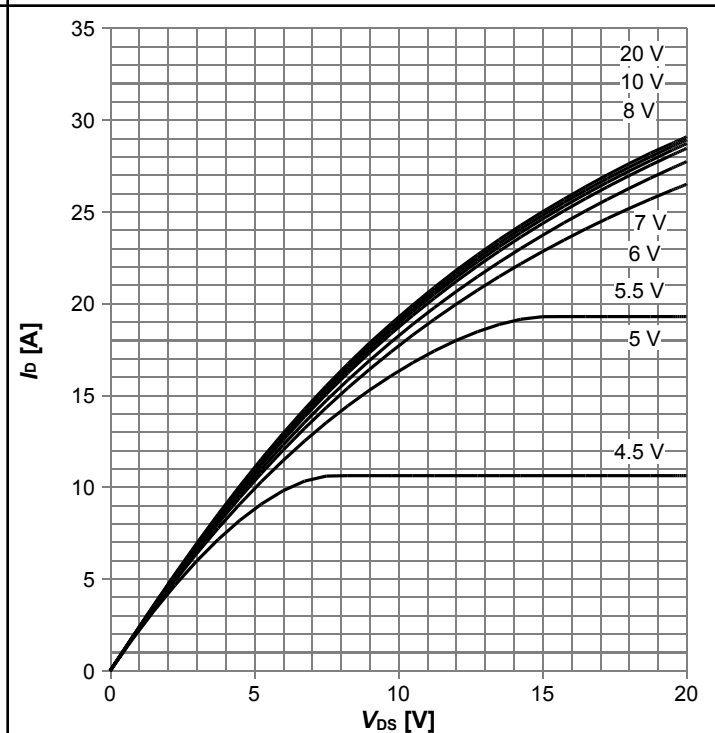


Diagram 5: Typ. output characteristics



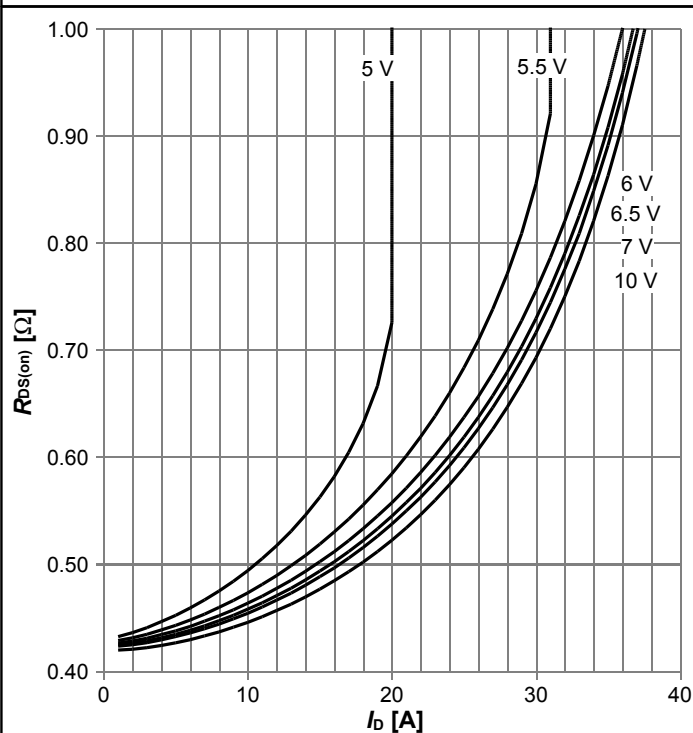
$I_D = f(V_{DS})$; $T_J = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



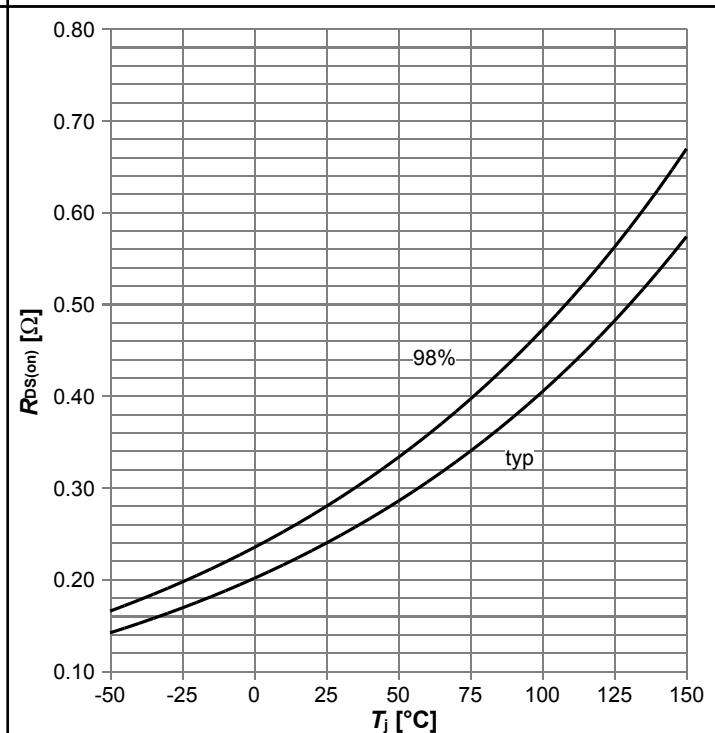
$I_D = f(V_{DS})$; $T_J = 125\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



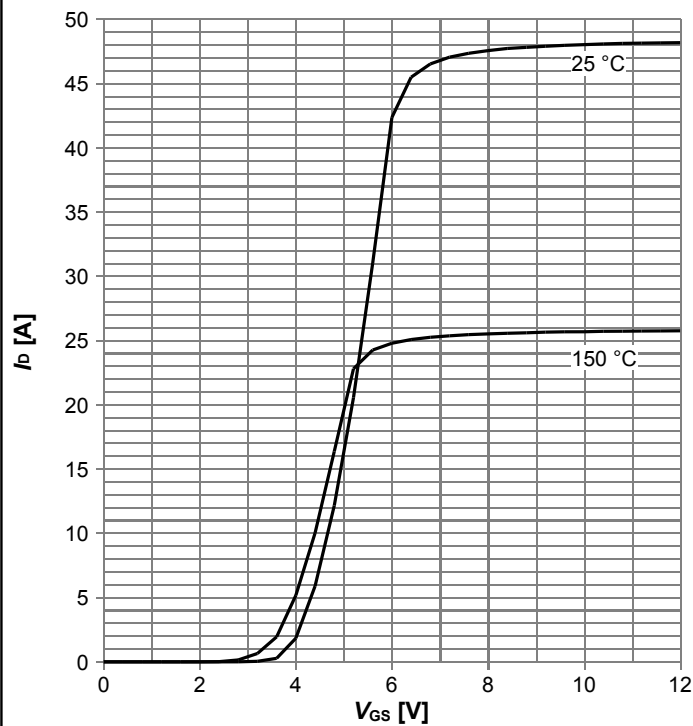
$R_{DS(on)} = f(I_D)$; $T_J = 125\text{ °C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



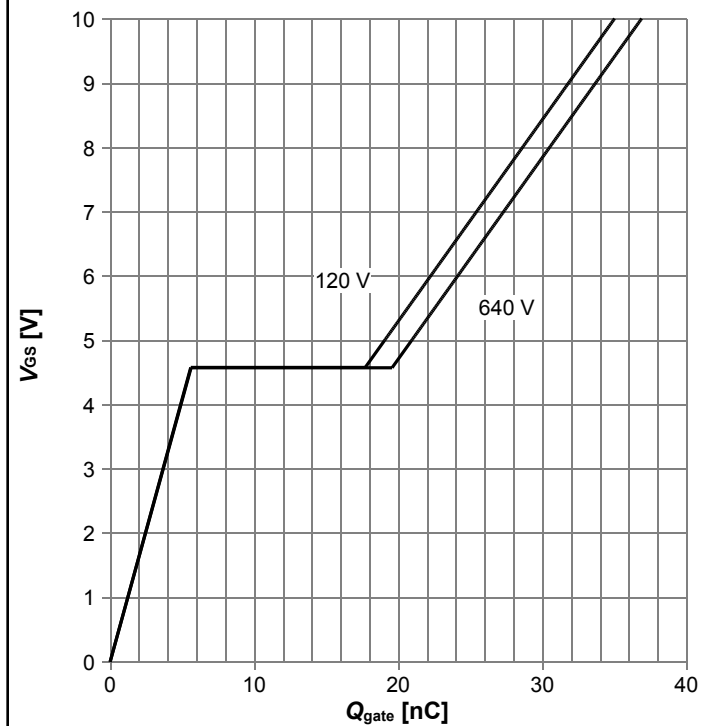
$R_{DS(on)} = f(T_J)$; $I_D = 7.2\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



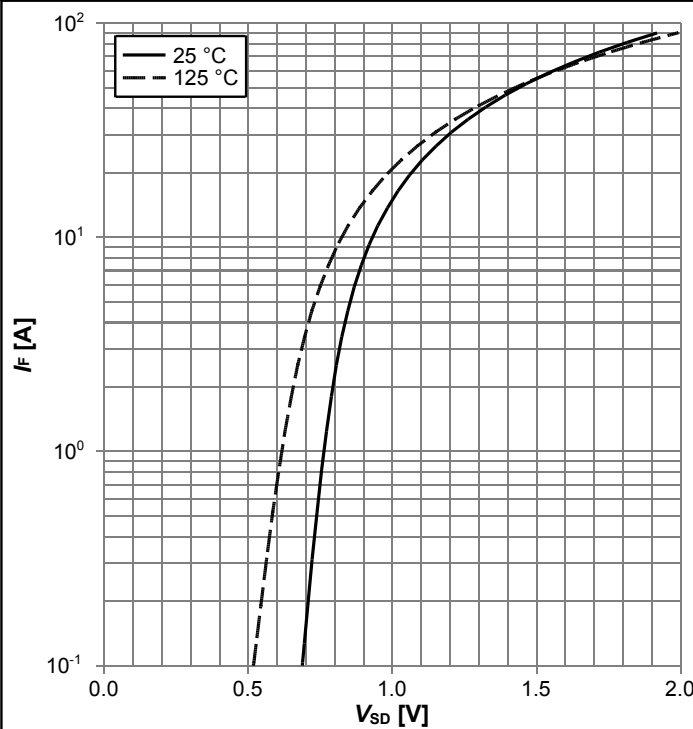
$I_D = f(V_{GS})$; $V_{DS} = 20$ V; parameter: T_j

Diagram 10: Typ. gate charge



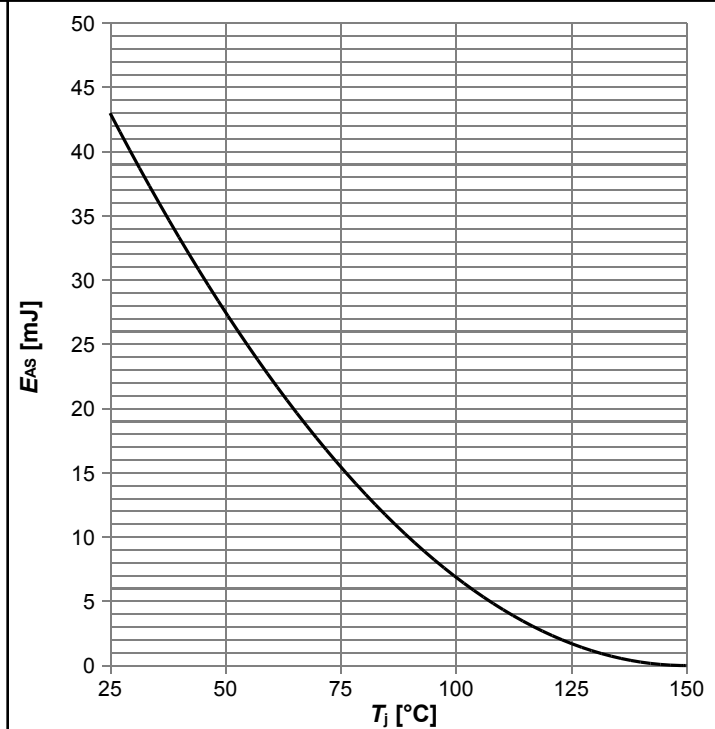
$V_{GS} = f(Q_{gate})$; $I_D = 7.2$ A pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



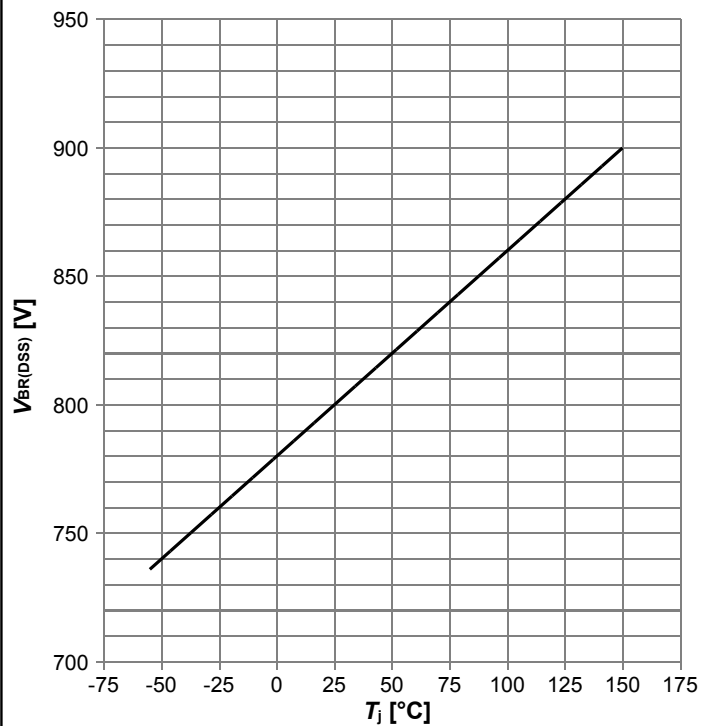
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



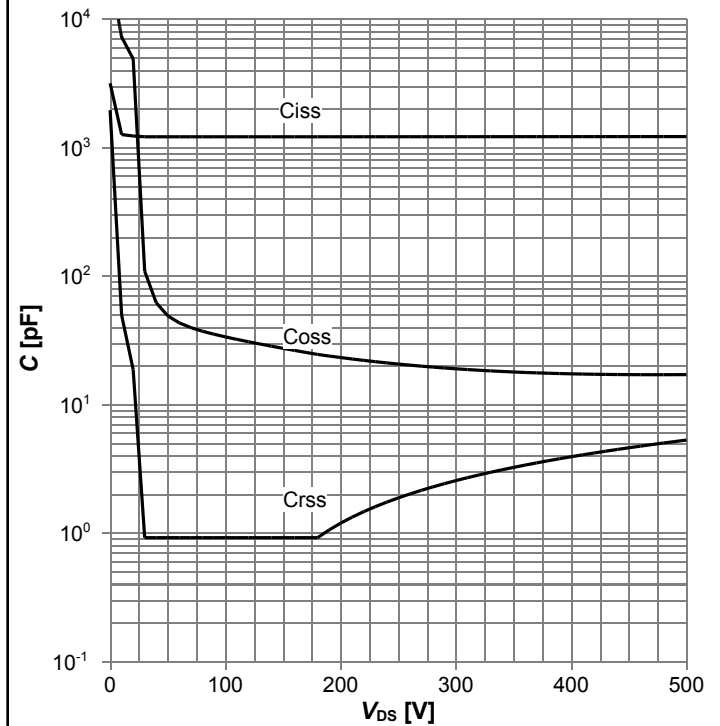
$E_{AS} = f(T_j)$; $I_D = 2.2$ A; $V_{DD} = 50$ V

Diagram 13: Drain-source breakdown voltage



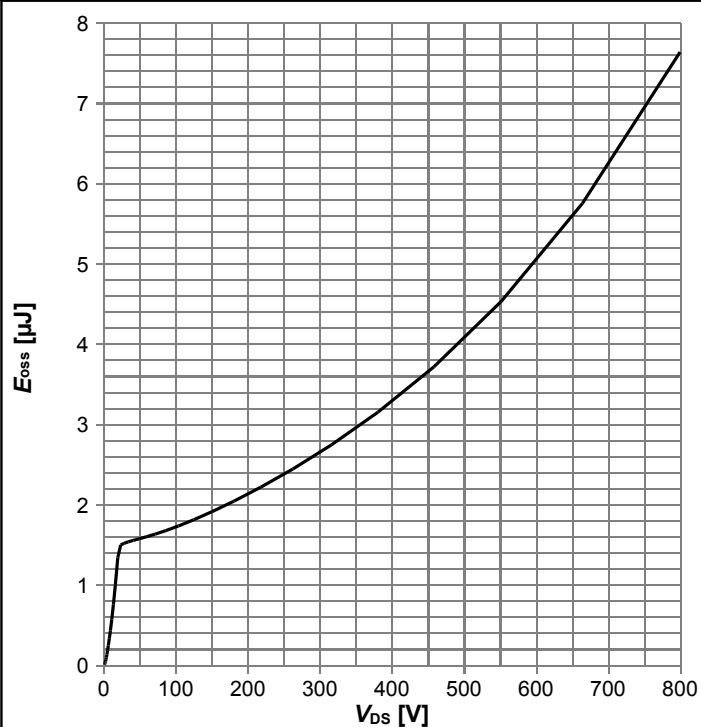
$V_{BR(DSS)} = f(T_J); I_D = 1 \text{ mA}$

Diagram 14: Typ. capacitances



$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 250 \text{ kHz}$

Diagram 15: Typ. C_{oss} stored energy



$E_{oss} = f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics

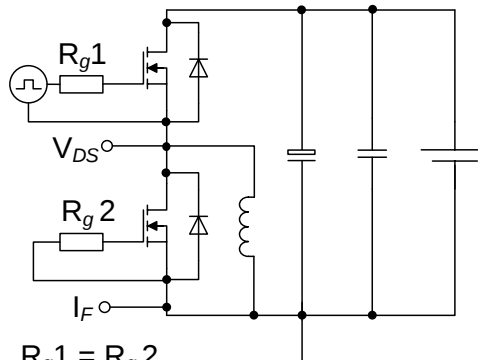
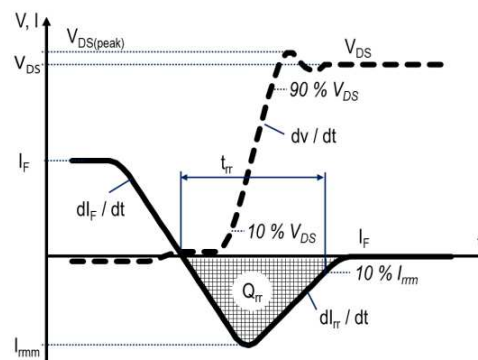
Test circuit for diode characteristics	Diode recovery waveform
 $R_{g1} = R_{g2}$	

Table 9 Switching times

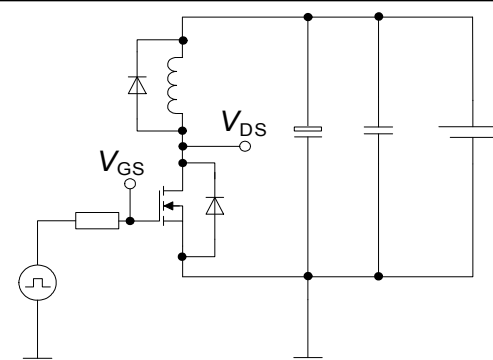
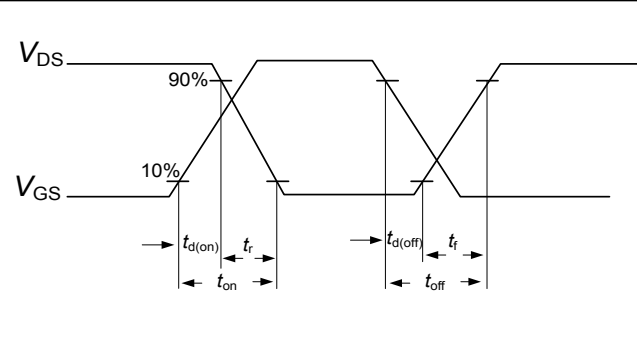
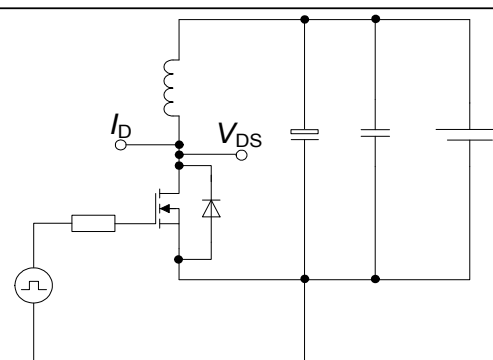
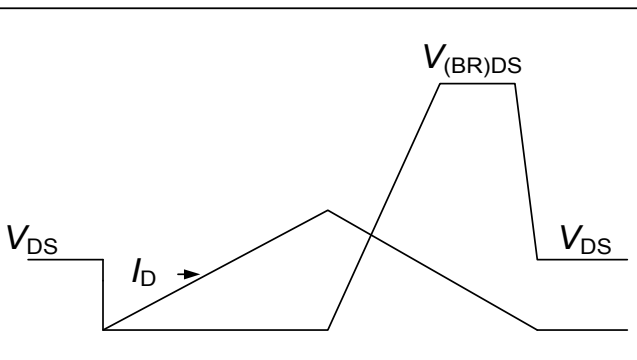
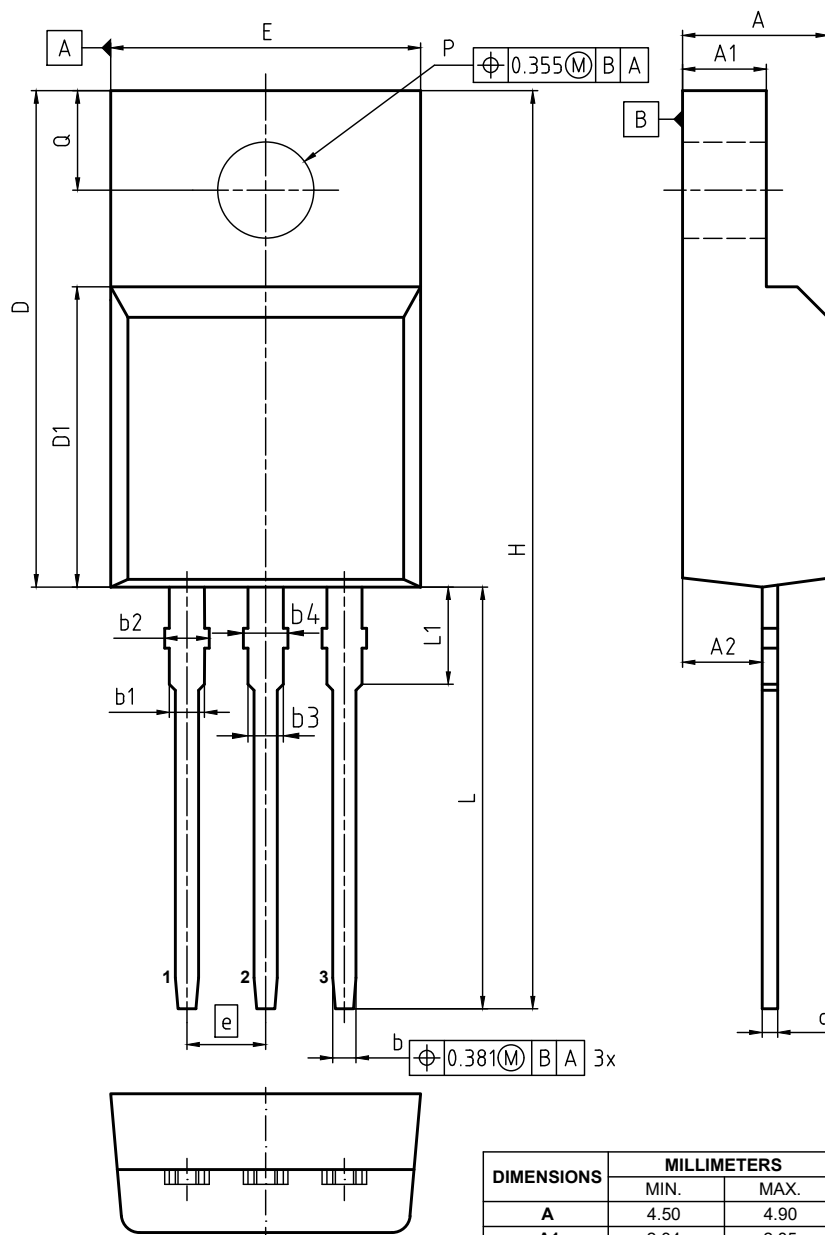
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

6 Package Outlines



NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PRO-
TRUSIONS OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.85
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	0.95	1.51
b3	0.65	1.38
b4	0.65	1.51
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
øP	3.00	3.30
Q	3.15	3.50

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REVISION 10
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SCALE 5:1 0 1 2 3 4 5mm
EUROPEAN PROJECTION

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm

7 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infineon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPA80R280P7

Revision: 2020-01-27, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2016-07-05	Release of final version
2.1	2018-02-07	Corrected front page text
2.2	2020-01-27	Updated package drawing, symbol ID and product validation

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