

HUF76629D3, HUF76629D3S

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 12)	100	-	-	V	
		I _D = 250μA, V _{GS} = 0V , T _C = -40°C (Figure 12)	90	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 95V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 90V, V _{GS} = 0V, T _C = 150°C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 11)	1	-	3	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 20A, V _{GS} = 10V (Figures 9, 10)	-	0.0415	0.052	Ω	
		I _D = 20A, V _{GS} = 5V (Figure 9)	-	0.046	0.054	Ω	
		I _D = 20A, V _{GS} = 4.5V (Figure 9)	-	0.047	0.055	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	TO-251AA and TO-252AA	-	-	1.36	°C/W	
Thermal Resistance Junction to Ambient	R _{θJA}		-	-	100	°C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 4.5V)							
Turn-On Time	t _{ON}	V _{DD} = 50V, I _D = 20A V _{GS} = 4.5V, R _{GS} = 6.8Ω (Figures 15, 21, 22)	-	-	190	ns	
Turn-On Delay Time	t _{d(ON)}		-	11	-	ns	
Rise Time	t _r		-	114	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	38	-	ns	
Fall Time	t _f		-	60	-	ns	
Turn-Off Time	t _{OFF}		-	-	145	ns	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 50V, I _D = 20A V _{GS} = 10V,R _{GS} = 8.2Ω (Figures 16, 21, 22)	-	-	50	ns	
Turn-On Delay Time	t _{d(ON)}		-	6.8	-	ns	
Rise Time	t _r		-	28	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	67	-	ns	
Fall Time	t _f		-	60	-	ns	
Turn-Off Time	t _{OFF}		-	-	190	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 10V	V _{DD} = 50V, I _D = 20A, I _{g(REF)} = 1.0mA (Figures 14, 19, 20)	-	38	46	nC
Gate Charge at 5V	Q _{g(5)}	V _{GS} = 0V to 5V		-	21	25	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 1V		-	1.2	1.6	nC
Gate to Source Gate Charge	Q _{gs}			-	3.3	-	nC
Gate to Drain "Miller" Charge	Q _{gd}			-	10	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 13)	-	1285	-	pF	
Output Capacitance	C _{OSS}		-	270	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	65	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 20\text{A}$	-	-	1.25	V
		$I_{SD} = 10\text{A}$	-	-	1.00	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 20\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	110	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 20\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	370	nC

Typical Performance Curves

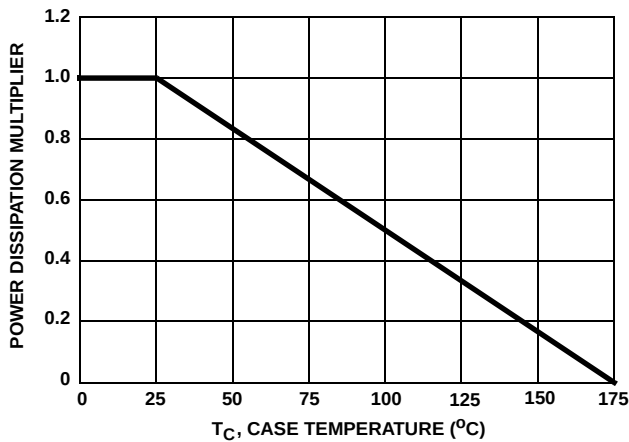


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

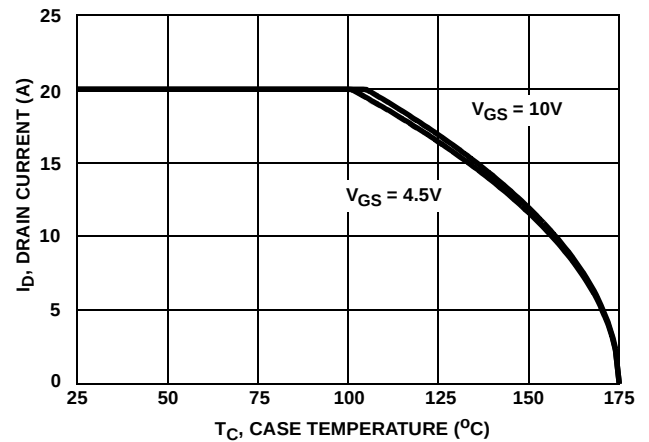


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

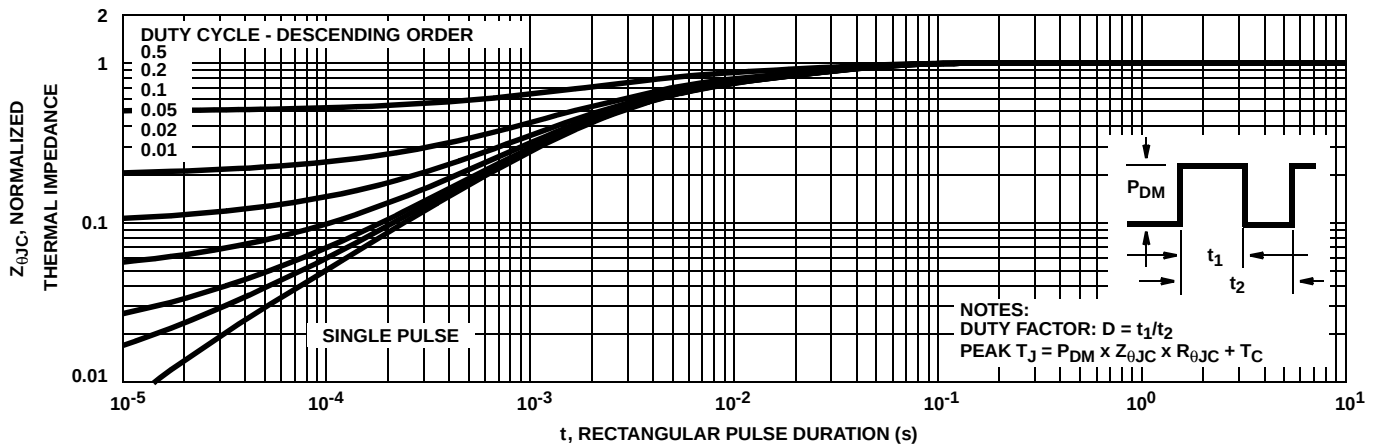


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

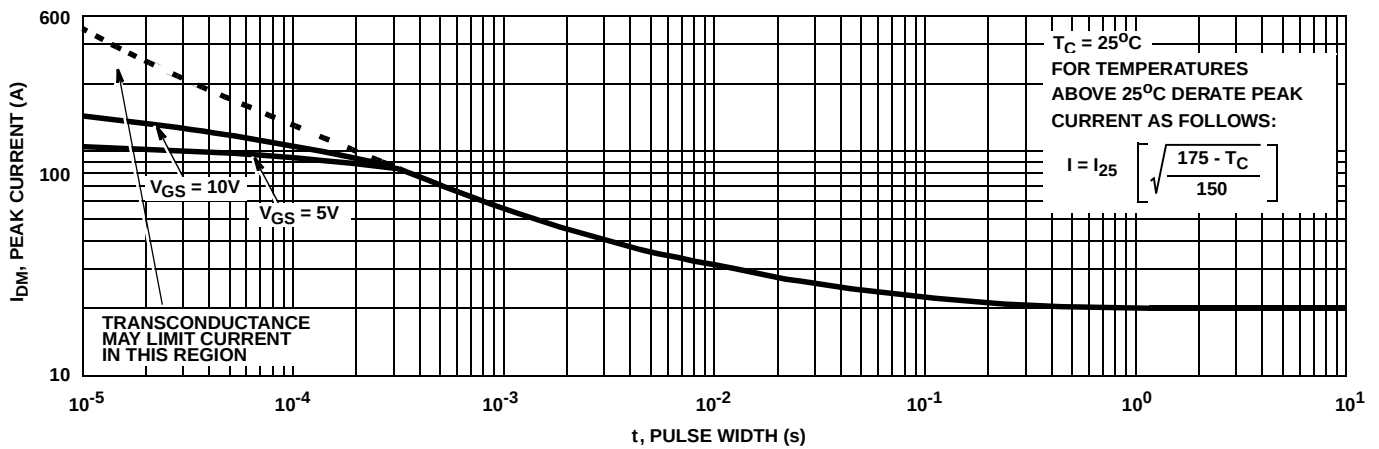


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

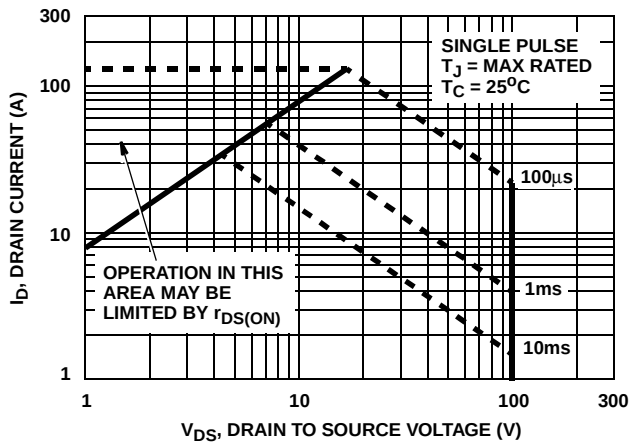
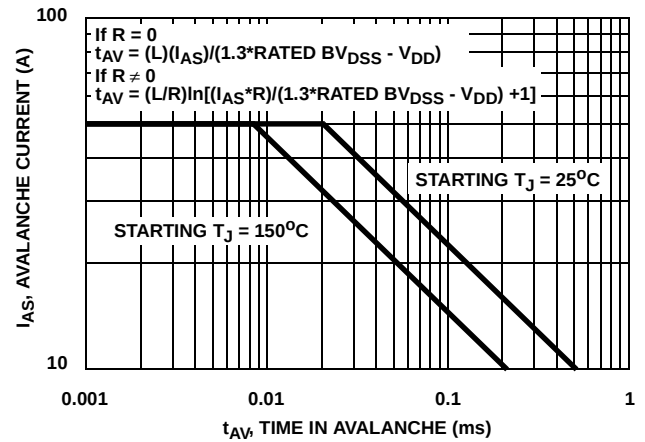


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

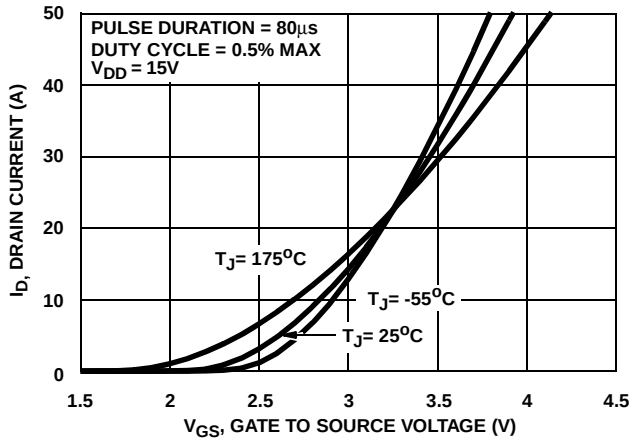


FIGURE 7. TRANSFER CHARACTERISTICS

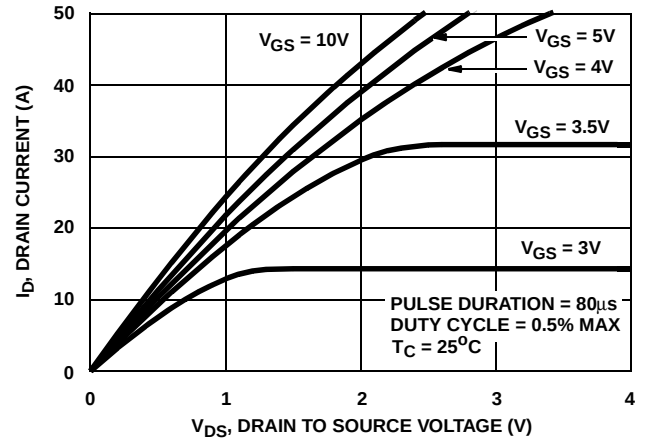


FIGURE 8. SATURATION CHARACTERISTICS

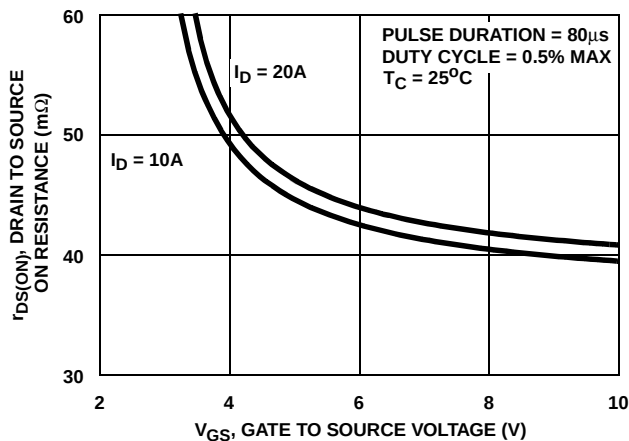


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

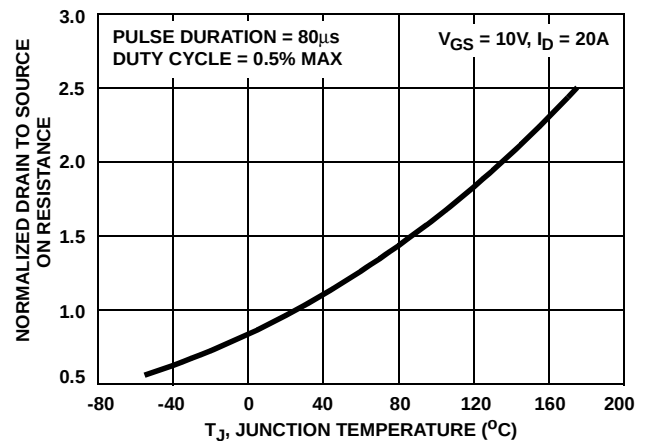


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

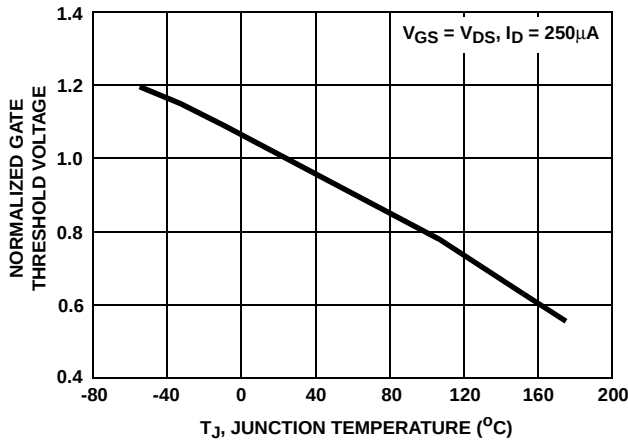


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

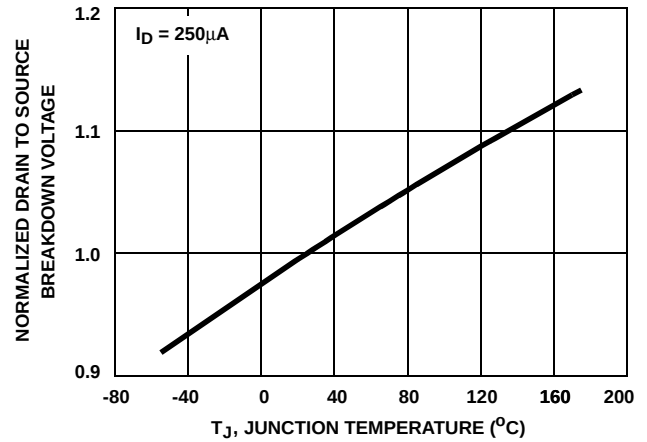


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

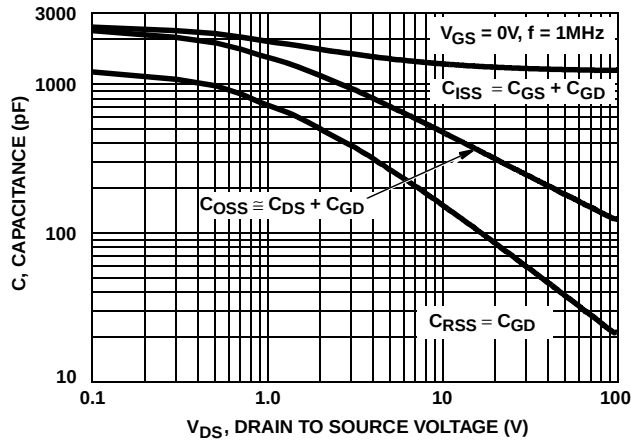
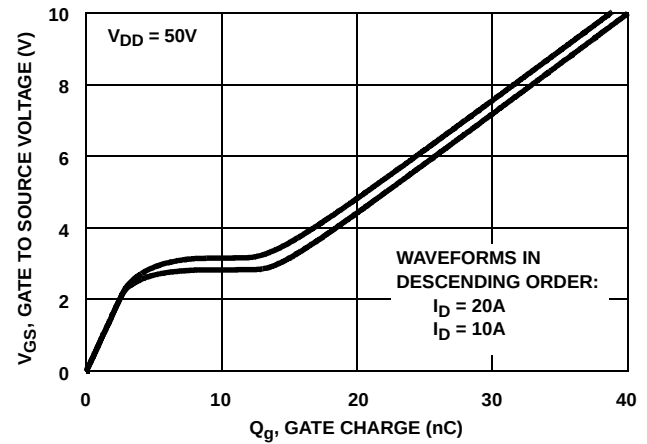


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

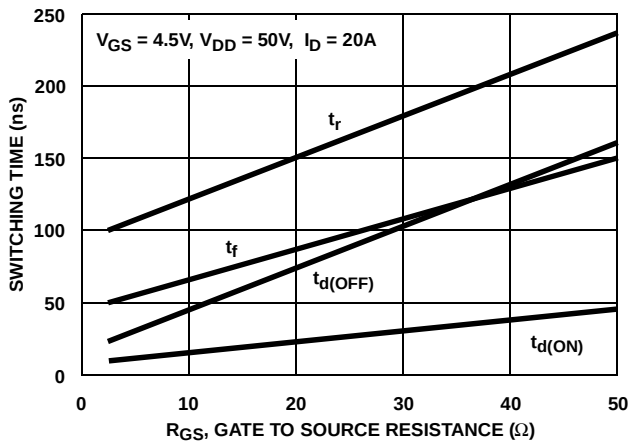


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

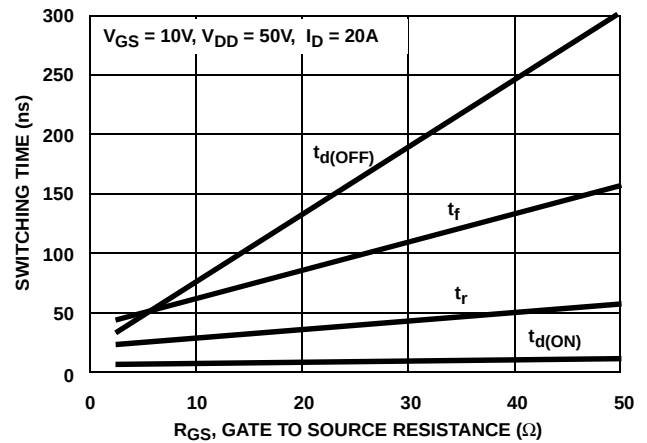


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

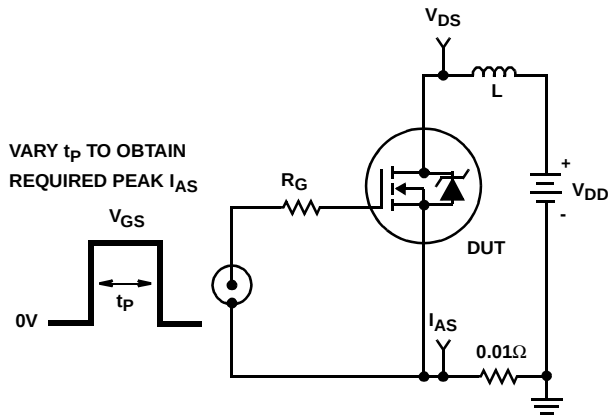


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

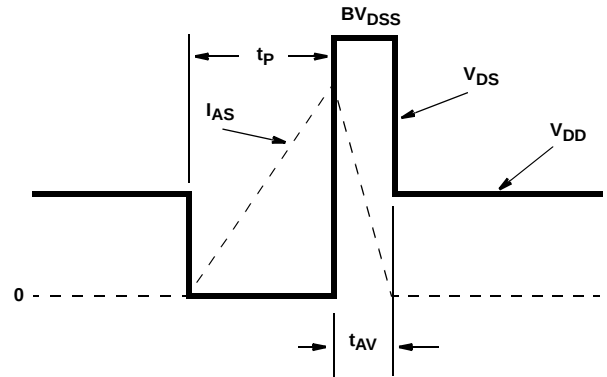


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

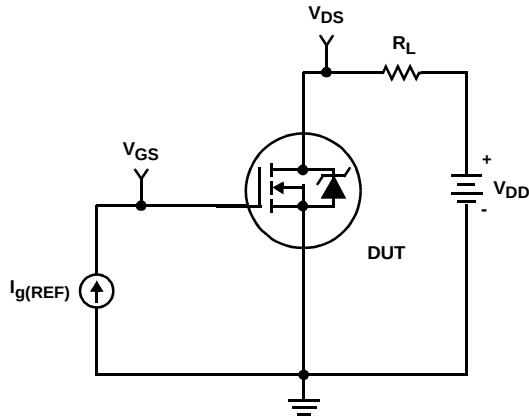


FIGURE 19. GATE CHARGE TEST CIRCUIT

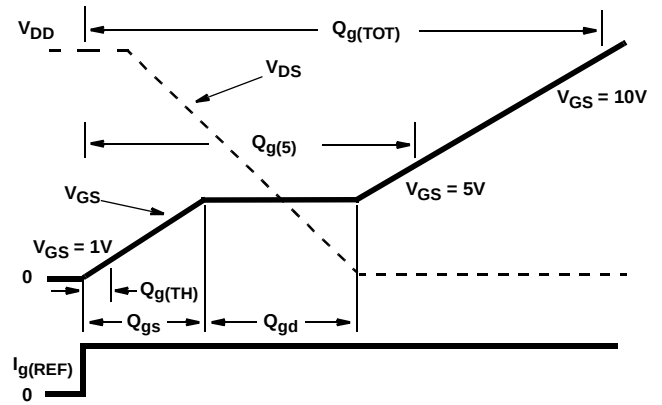


FIGURE 20. GATE CHARGE WAVEFORMS

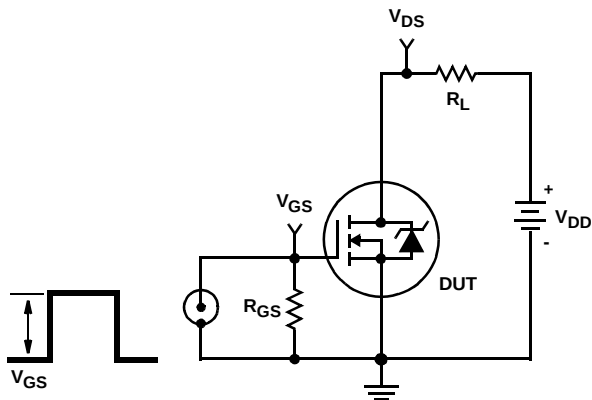


FIGURE 21. SWITCHING TIME TEST CIRCUIT

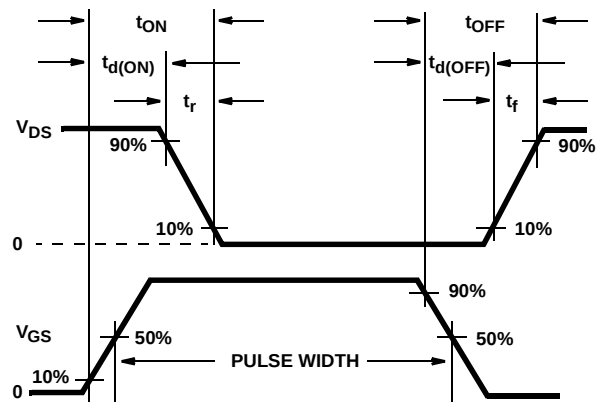


FIGURE 22. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

.SUBCKT HUF76629D3 2 1 3 ; rev 30 July 1999

CA 12 8 2.32e-9
CB 15 14 2.32e-9
CIN 6 8 1.22e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 117.89
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 3.11e-9
LSOURCE 3 7 3.72e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 2.97e-2
RGATE 9 20 2.81
RLDRAIN 2 5 10
RLGATE 1 9 54.2
RLSOURCE 3 7 41.6
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 6.5e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

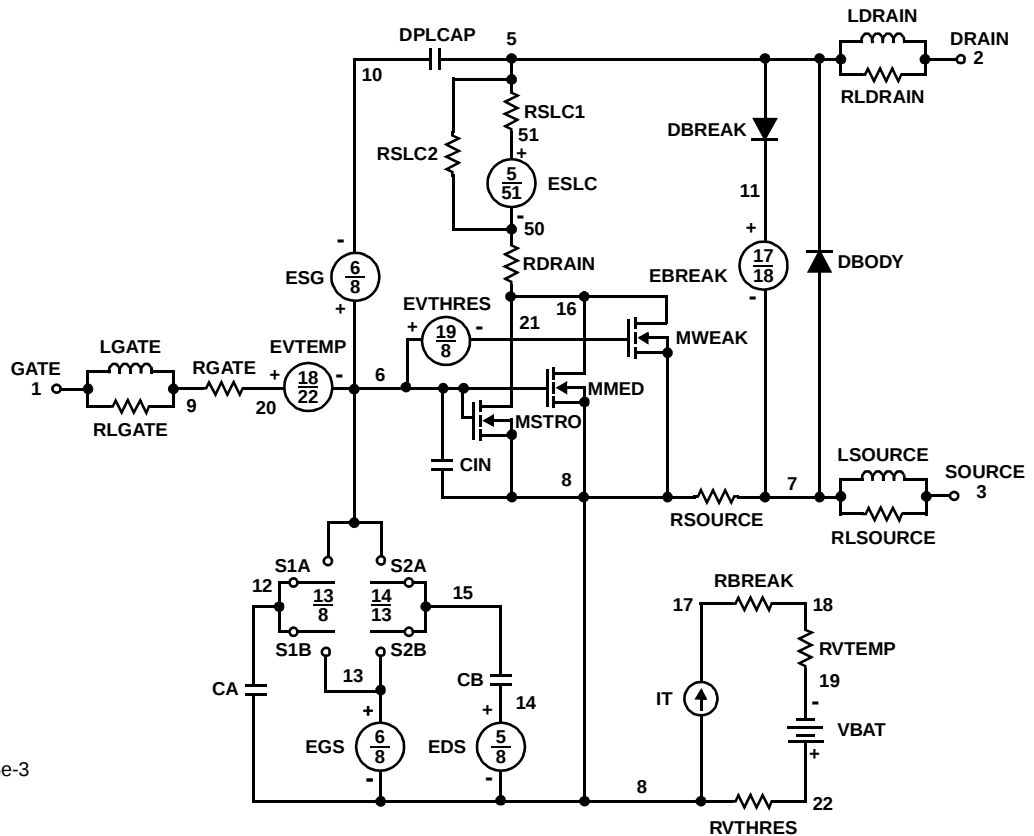
ESLC 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) * (PWR(V(5,51)/(1e-6*61),3)) }

.MODEL DBODYMOD D (IS = 1.15e-12 IKF = 4.3 RS = 7.45e-3 TRS1 = 2.40e-3 TRS2 = 5.15e-7 CJO = 1.14e-9 TT = 5.86e-8 M = 0.52 XTI = 3.65)
.MODEL DBREAKMOD D (RS = 3.78e-1 TRS1 = 1e-3 TRS2 = -1e-6)
.MODEL DPLCAPMOD D (CJO = 1.37e-9 IS = 1e-3 ON = 10 M = 0.94)
.MODEL MMEDMOD NMOS (VTO = 1.84 KP = 2.6 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 2.81)
.MODEL MSTROMOD NMOS (VTO = 2.13 KP = 42.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.58 KP = 0.07 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 28.1 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 9.88e-4 TC2 = -5.40e-7)
.MODEL RDRAINMOD RES (TC1 = 7.85e-3 TC2 = 1.95e-5)
.MODEL RSLCMOD RES (TC1 = 4.97e-3 TC2 = 5.05e-6)
.MODEL RSOURCEMOD RES (TC1 = 1.5e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = -1.85e-3 TC2 = -4.48e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.72e-3 TC2 = 6.00e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.5 VOFF = -2.2)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.2 VOFF = -5.5)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.1 VOFF = 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -1.1)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SABER Electrical Model

REV 30 July 1999

template huf76629d3 n2,n1,n3

electrical n2,n1,n3

```
{
var i iscl
d..model dbodymod = (is = 1.15e-12, cjo = 1.14e-9, tt = 5.86e-8, xti = 3.65, m = 0.52)
d..model dbreakmod = ()
d..model dplcapmod = (cjo = 1.37e-9, is = 1e-30, n = 10, m = 0.94)
m..model mmedmod = (type=_n, vto = 1.84, kp = 2.6, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.13, kp = 42.5, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.58, kp = 0.07, is = 1e-30, tox = 1)
sw_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -5.5, voff = -2.2)
sw_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -2.2, voff = -5.5)
sw_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -1.1, voff = 0.5)
sw_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 0.5, voff = -1.1)
```

c.ca n12 n8 = 2.32e-9

c.cb n15 n14 = 2.32e-9

c.cin n6 n8 = 1.22e-9

d.dbody n7 n71 = model=dbodymod

d.dbreak n72 n11 = model=dbreakmod

d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9

l.lgate n1 n9 = 3.11e-9

l.lsource n3 n7 = 3.72e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u

m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u

m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1 = 9.88e-4, tc2 = -5.40e-7

res.rbody n71 n5 = 7.45e-3, tc1 = 2.40e-3, tc2 = 5.15e-7

res.rdbreak n72 n5 = 3.78e-1, tc1 = 1.00e-3, tc2 = -1.00e-6

res.rdrain n50 n16 = 2.97e-2, tc1 = 7.85e-3, tc2 = 1.95e-5

res.rgate n9 n20 = 2.81

res.rldrain n2 n5 = 10

res.rlgate n1 n9 = 54.2

res.rlsource n3 n7 = 41.6

res.rslc1 n5 n51 = 1e-6, tc1 = 4.97e-3, tc2 = 5.05e-6

res.rslc2 n5 n50 = 1e3

res.rsource n8 n7 = 6.5e-3, tc1 = 1.5e-3, tc2 = 1e-6

res.rvtemp n18 n19 = 1, tc1 = -1.72e-3, tc2 = 6.00e-7

res.rvthres n22 n8 = 1, tc1 = -1.85e-3, tc2 = -4.48e-6

spe.ebreak n11 n7 n17 n18 = 117.89

spe.eds n14 n8 n5 n8 = 1

spe.egs n13 n8 n6 n8 = 1

spe.esg n6 n10 n6 n8 = 1

spe.evtemp n20 n6 n18 n22 = 1

spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod

sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod

sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod

sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

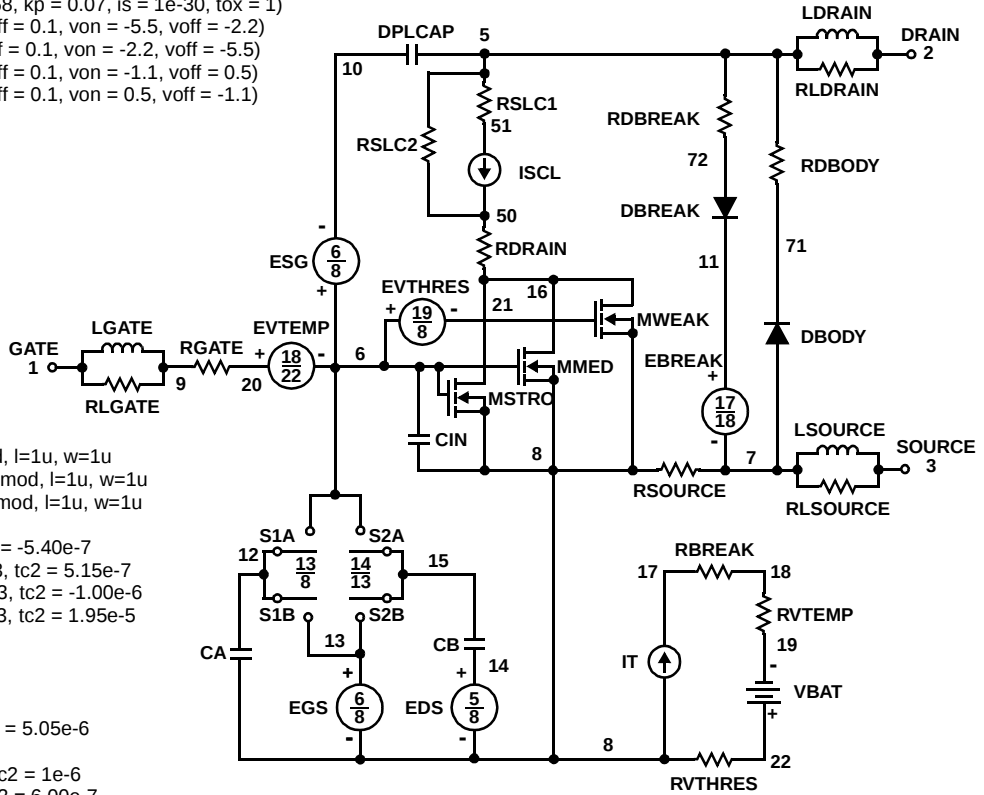
equations {

i (n51->n50) +=iscl

iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/61))** 3))

}

}



SPICE Thermal Model

REV 26 July 1999

HUF76629D3

CTHERM1 th 6 2.45e-3
 CTHERM2 6 5 8.15e-3
 CTHERM3 5 4 7.40e-3
 CTHERM4 4 3 7.45e-3
 CTHERM5 3 2 1.01e-2
 CTHERM6 2 tl 7.49e-2

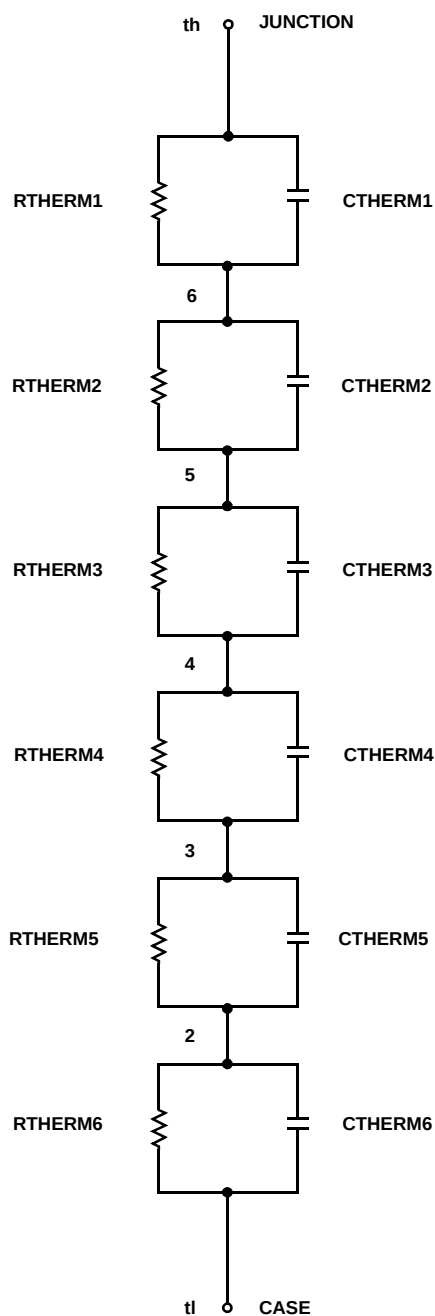
R THERM1 th 6 9.00e-3
 R THERM2 6 5 1.80e-2
 R THERM3 5 4 9.15e-2
 R THERM4 4 3 2.43e-1
 R THERM5 3 2 3.50e-1
 R THERM6 2 tl 3.62e-1

SABER Thermal Model

SABER thermal model HUF76629D3

```
template thermal_model th tl
thermal_c th, tl
{
    ctherm.ctherm1 th 6 = 2.45e-3
    ctherm.ctherm2 6 5 = 8.15e-3
    ctherm.ctherm3 5 4 = 7.40e-3
    ctherm.ctherm4 4 3 = 7.45e-3
    ctherm.ctherm5 3 2 = 1.01e-2
    ctherm.ctherm6 2 tl = 7.49e-2
```

```
    rtherm.rtherm1 th 6 = 9.00e-3
    rtherm.rtherm2 6 5 = 1.80e-2
    rtherm.rtherm3 5 4 = 9.15e-2
    rtherm.rtherm4 4 3 = 2.43e-1
    rtherm.rtherm5 3 2 = 3.50e-1
    rtherm.rtherm6 2 tl = 3.62e-1
}
```



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DenseTrench [™]	GTO [™]	Power247 [™]	SuperSOT [™] -6	
DOME [™]	HiSeC [™]	PowerTrench [®]	SuperSOT [™] -8	
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EnSigna [™]	MicroFET [™]	QT Optoelectronics [™]	TruTranslation [™]	
FACT [™]	MicroPak [™]	Quiet Series [™]	UHC [™]	
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Definition of Terms

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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