Application Support Information

The Application Engineering group in Lite-On Technology is available to assist you with the technical understanding associated with HSDL-3208 infrared transceiver module. You can contact them through your local Lite-On sales representatives for additional details.

Order Information

Part Number	Packaging Type	Package	Quantity
HSDL-3208-021	Tape and Reel	Front View	2500

Marking Information

The unit is marked with 'YWL' on the back of the PCB for front option without shield.
Y = year
W = work week
L = lot information

I/O Pins Configuration Table

Pin	Symbol	Description	I/O Type	Notes
1	LED A	LED Anode	Input	1
2	LED C	LED Cathode		2
3	TXD	Transmit Data	Input, Active High	3
4	RXD	Receive Data	Output, Active Low	4
5	SD/Mode	Shutdown	Input, Active High	5
6	V_{CC}	Supply Voltage	Supply Voltage	6
7	GND	Ground	Ground	7

Notes:
1. This pin can be connected directly to V_{CC} (i.e. without series resistor) at less than 3 V.
2. Leave this pin unconnected.
3. This pin is used to transmit serial data when SD pin is low. Do not float the pin. This pin has an internal 500 kΩ pulldown with a typical input capacitance of 2 pF.
4. This pin is capable of driving a standard CMOS or TTL load. No external pull-up or pull down resistor is required. It is in tri-state mode when the transceiver is in shutdown mode. This pin tristates with a weak 500 kΩ pullup resistor.
5. The transceiver is in shutdown mode if this pin is high. Do not float the pin.
6. Regulated, 2.4 to 3.6 volts.
7. Connect to system ground.

Recommended Application Circuit Components

Component	Recommended Value	Notes
R1	30 Ω ± 5%, 0.25 Watt for 2.4 <= V_{CC} <= 3.6 V	
CX1	0.47 µF ± 20%, X7R Ceramic	8
CX2	6.8 µF ± 20%, Tantalum	9

Notes:
8. CX1 must be placed within 0.7 cm of the HSDL-3208 to obtain optimum noise immunity.
9. In environments with noisy power supplies, supply rejection performance can be enhanced by including CX2, as shown in "Figure 1: HSDL-3208 Functional Block Diagram" in Page 1.

TX Power Mode Switching

The transceiver is in default High TX Power Mode upon powered on. User needs to apply the following programming sequence to both SD and TXD inputs to switch the module to Low TX Power Mode. Both settings of High TX Power and Low TX Power Mode can be achieved as follows:

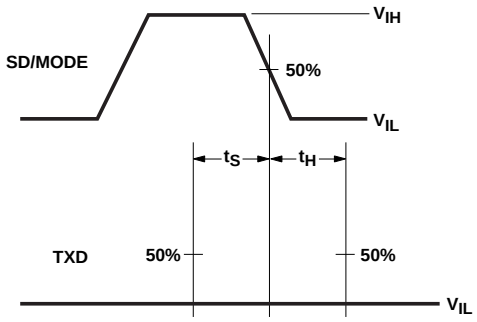


Figure 3. High power mode selection timing diagram.

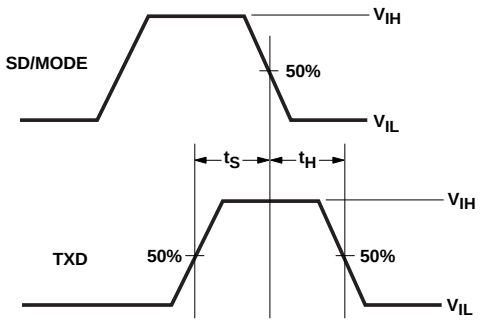


Figure 4. Low power mode selection timing diagram.

1. Set SD/Mode input to logic High.
2. TXD input should remain at logic Low.
3. After waiting for $t_s \geq 25$ ns, set SD/Mode to logic Low. The High to Low negative edge transition will determine the TX Power Mode.
4. Ensure that TXD input remains low for $t_H \geq 100$ ns. The transmitter is now in High mode.
5. SD input pulse width for mode selection should be > 50 ns.

1. Set SD/Mode input to logic High.
2. After SD/Mode input remains High at > 25 ns, set TXD input to logic High, wait $t_s \geq 25$ ns (from 50% of TXD rising edge until 50% of SD falling edge).
3. Then set SD/Mode to logic Low. The High to Low negative edge transition will determine the TX Power Mode.
4. After waiting for $t_H \geq 100$ ns, set the TXD input to logic Low.
5. SD input pulse width for mode selection should be > 50 ns.

CAUTIONS: The BiCMOS inherent to the design of this component increases the component's susceptibility to damage from the electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Absolute Maximum Ratings

For implementations where case to ambient thermal resistance is ≤ _50°C/W.

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	-40	+100	°C	
Operating Temperature	T_A	-25	+85	°C	
LED Anode Voltage	V_{LEDA}	0	6.5	V	
Supply Voltage	V_{CC}	0	6.5	V	
Input Voltage: TXD, SD/Mode	V_I	0	6.5	V	
Output Voltage: RXD	V_O	0	6.5	V	
DC LED Transmit Current	I_{LED} (DC)		50	mA	
Peak LED Transmit Current	I_{LED} (PK)		250	mA	10

Note:

10. ≤ 20% duty cycle, ≤ 90 µs pulse width.

Recommended Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Operating Temperature		T_A	-25		70	°C	
Supply Voltage		V_{CC}	2.4		3.6	V	
Logic Input Voltage for TXD, SD/Mode	Logic High	V_{IH}	2/3 V_{CC}		V_{CC}	V	
	Logic Low	V_{IL}	0		1/3 V_{CC}	V	
Receiver Input Irradiance	Logic High	EI_H	0.0081		500	mW/cm^2	For in-band signals ≤ 115.2kbit/s[11]
	Logic Low	EI_L			1	µW/cm^2	For in-band signals[11]
LED (Logic High) Current Pulse Amplitude		I_{LEDA}		50		mA	
Receiver Data Rate			9.6		115.2	kbit/s	

Note:

11. An in-band optical signal is a pulse/sequence where the peak wavelength, λp, is defined as 850 ≤ λp ≤ 900 nm, and the pulse characteristics are compliant with the IrDA Serial Infrared Physical Layer Link Specification v1.4.

Electrical & Optical Specifications

Specifications (Min. & Max. values) hold over the recommended operating conditions unless otherwise noted. Unspecified test conditions may be anywhere in their operating range. All typical values (Typ.) are at 25°C with V_{CC} set to 3.0 V unless otherwise noted.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions
Receiver							
Viewing Angle		2θ	30			°	
Peak Sensitivity Wavelength		λ_p		880		nm	
RXD Output Voltage	Logic High	V_{OH}	V_{CC}-0.2		V_{CC}	V	I_{OH} = -200 µA, EI ≤ 1 µW/cm^2
	Logic Low	V_{OL}	0		0.4	V	I_{OL} = 200 µA, EI ≥ 8.1 µW/cm^2
RXD Pulse Width (SIR)		t_{PW} (SIR)	1		4.0	µs	$\theta \leq 15^{\circ}$, C_L =12 pF
RXD Rise and Fall Times		t_r, t_f		50		ns	C_L =12 pF
Receiver Latency Time		t_L		70		µs	
Receiver Wake Up Time		t_W		90		µs	
Transmitter							
Radiant Intensity	High Power	IE_H	4	8		mW/sr	I_{LEDA} = 50 mA, $\theta \leq 15^{\circ}$, $V_{TXD} \geq V_{IH}$ T = 25°C
	Low Power	IE_H	2.4	4.8		mW/sr	I_{LEDA} = 30 mA, $\theta \leq 15^{\circ}$, $V_{TXD} \geq V_{IH}$ T = 70°C, V_{CC} = 2.4 V
Viewing Angle		2θ	30		60	°	
Peak Wavelength		λ_p		875		nm	
Spectral Line Half Width		$\Delta\lambda$		35		nm	
TXD Input Current	High	I_H		0.02	10	µA	$V_I \geq V_{IH}$
	Low	I_L	-10	-0.02	10	µA	$0 \leq V_I \_ \leq V_{IL}$
LED Current	On	I_{VLED}		50		mA	V_I (TXD) ≥ V_{IH}, V_I (SD) ≤ V_{IL}
	Shutdown	I_{VLED}		20	100	nA	V_I (SD) ≥ V_{IH}
Optical Pulse Width (SIR)		t_{PW} (SIR)	1.5	1.6	1.8	µs	t_{PW} (TXD) = 1.6 µs at 115.2 kbit/s
Maximum Optical PW	$t_{PW(max.)}$		25	100	µs		
TXD Rise and Fall Time (Optical)		t_r, t_f			600	ns	tpw (TXD) = 1.6 µs
LED Anode on State Voltage	High Power	V_{ON}(LEDA)		1.7	1.8	V	I_{LEDA} = 50 mA, V_I(TXD) ≥ V_{IH}
	Low Power	V_{ON}(LEDA)		2.1	2.25	V	I_{LEDA} = 30 mA, V_I(TXD) ≥ V_{IH} T = 70°C, V_{CC} = 2.4 V
LED Anode Current	Low Power	I_{LEDA}		32	42	mA	max. current measured at V_{LED} = 4.3 V and R = 33 Ω
Transceiver							
Supply Current	Shutdown	I_{CC1}		0.001	1	µA	$V_{SD} \geq V_{CC}$ -0.5, T_A = 25°C
	Idle	I_{CC2}		100	200	µA	V_I (TXD) ≤ V_{IL}, EI = 0
	Active Receiver	I_{CC3}		0.8	3.1	mA	V_{CC} = 3.6 V, V_I(TXD)≤ 1/3 V_{CC}[12]

Notes:
12. Typical value is at EI = 10 mW/cm^2, maximum value is at EI = 500 mW/cm^2.

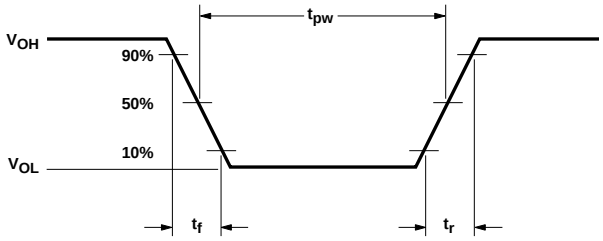


Figure 5. RXD output waveform.

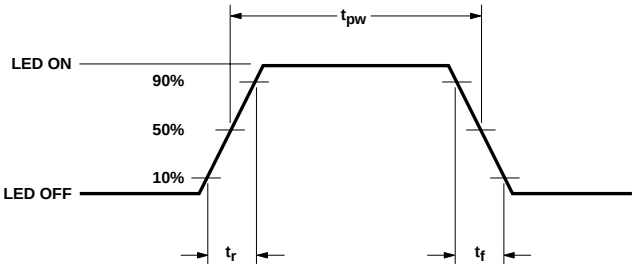


Figure 6. LED optical waveform.

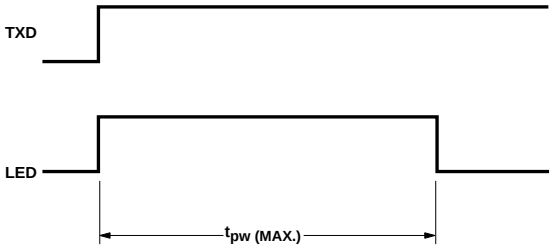


Figure 7. TXD "stuck on" protection waveform.

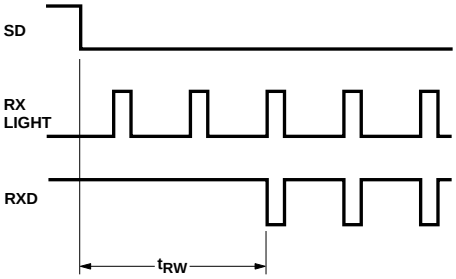


Figure 8. Receiver wakeup time waveform.

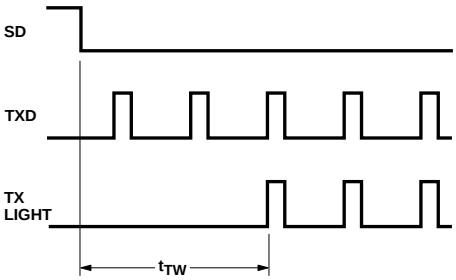


Figure 9. TXD wakeup time waveform.

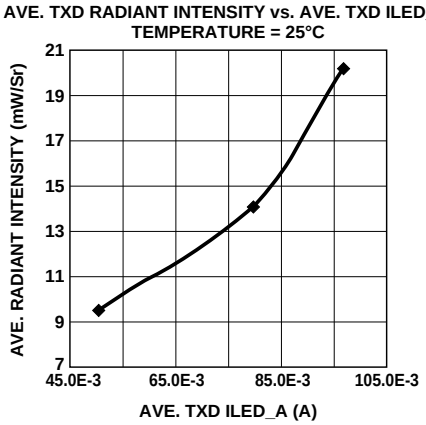


Figure 10. LOP vs. I_{LED}.

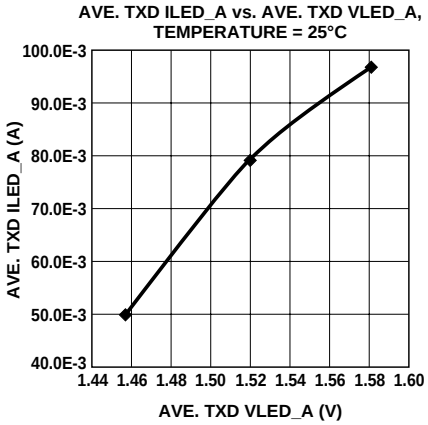


Figure 11. V_{LED} vs. I_{LED}.

HSDL-3208 (Unshielded) Package Dimensions

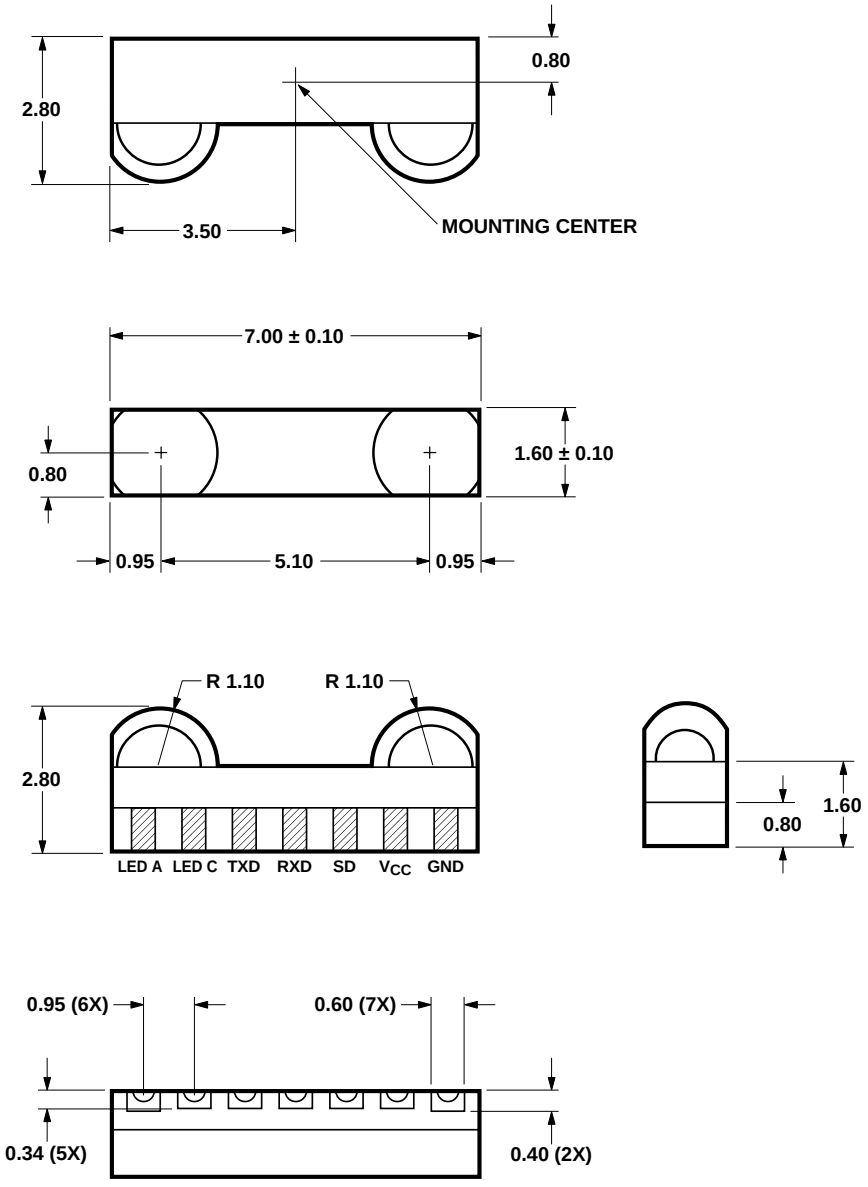


Figure 12. Package outline dimensions. (Unit: mm, Tolerance: ± 0.2 mm)

HSDL-3208 (Unshielded) Tape and Reel Dimensions

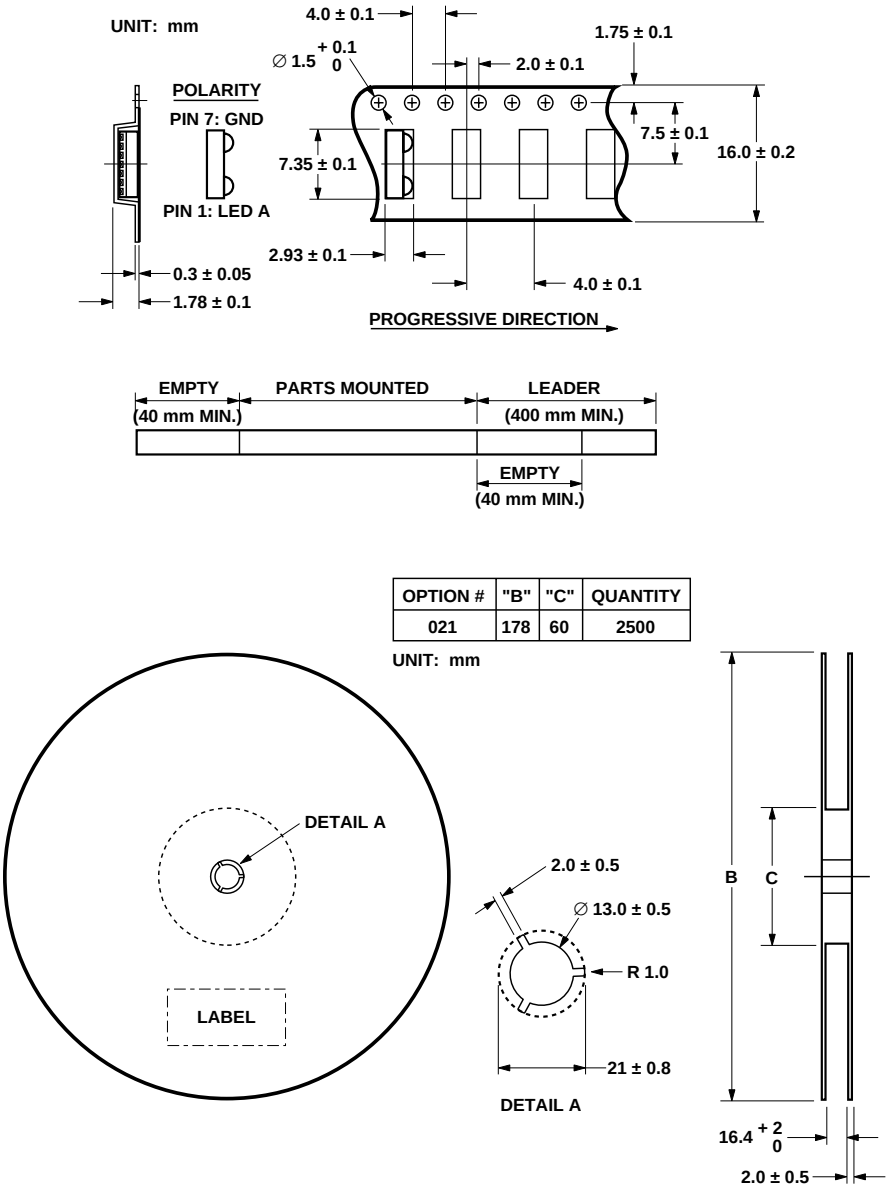


Figure 13. Tape and reel dimensions.

HSDL-3208 (Shielded) Package Dimensions

1. Unless otherwise stated, dimension tolerance: ±0.2 mm.
2. Castellation length, mentioned below, is the minimum value i.e., 0.6 mm.
   The specification is: 0.63 ± 0.03 mm.

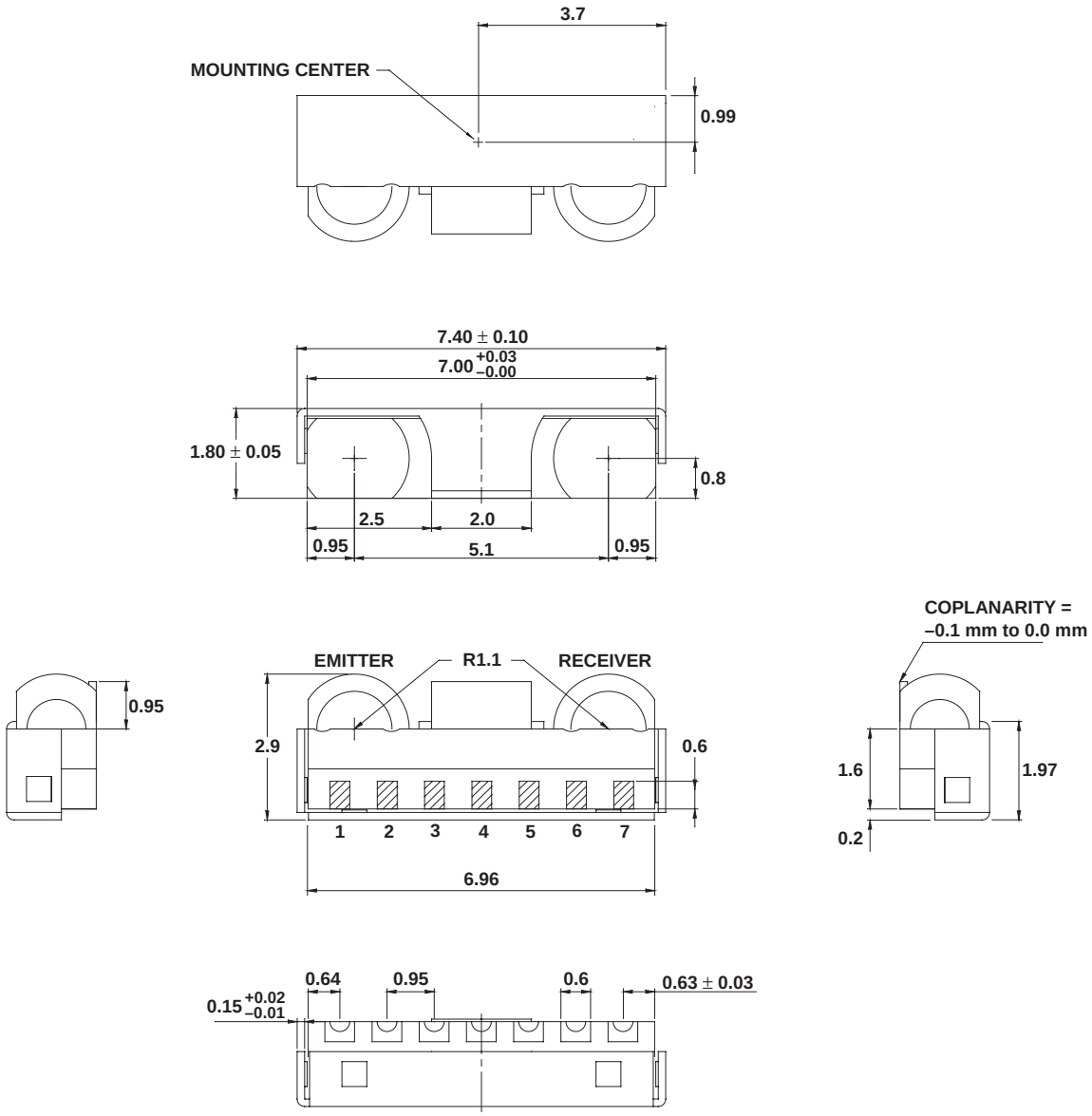
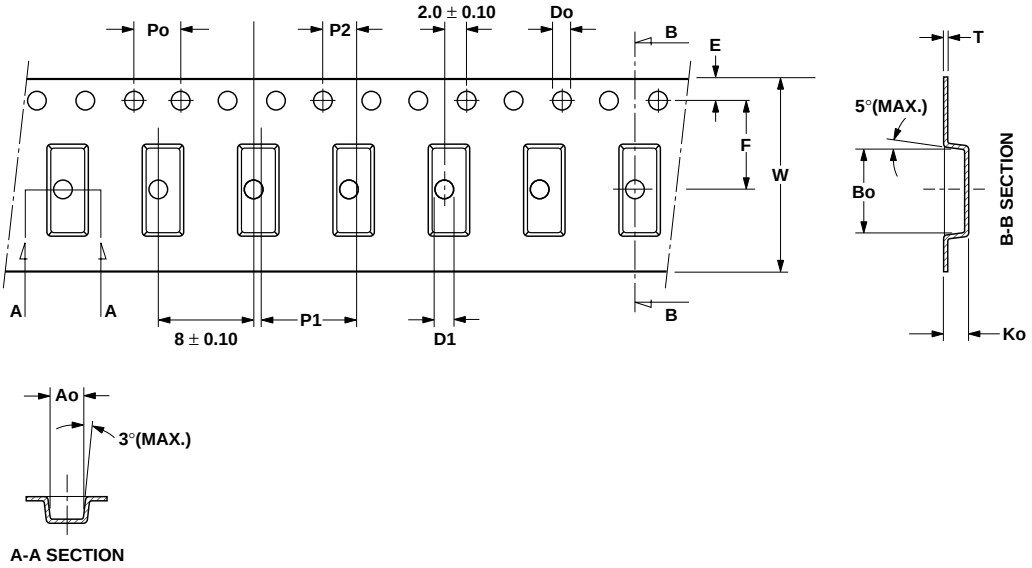


Figure 14a. Package outline dimensions.

HSDL-3208 (Shielded) Tape Dimensions



UNIT: mm

SYMBOL	Ao	Bo	Ko	Po	P1	P2	T
SPEC	3.15 ± 0.10	7.70 ± 0.10	1.95 ± 0.10	4.00 ± 0.10	8.00 ± 0.10	2.35 ± 0.10	0.30 ± 0.10
SYMBOL	E	F	Do	D1	W	10Po	
SPEC	1.75 ± 0.10	7.50 ± 0.10	1.55 ± 0.05	1.50 ± 0.10	16.00 ± 0.30	40.00 ± 0.20	

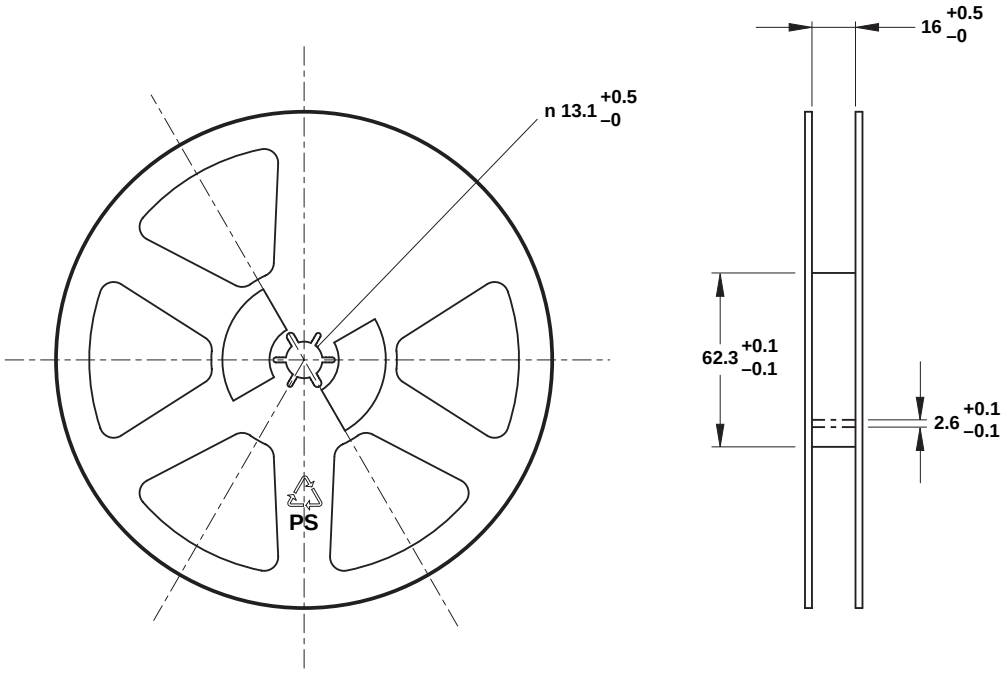


Figure 15. Tape dimensions.

Moisture Proof Packaging

All HSDL-3208 options are shipped in moisture proof package. Once opened, moisture absorption begins.

This part is compliant to JEDEC Level 4.

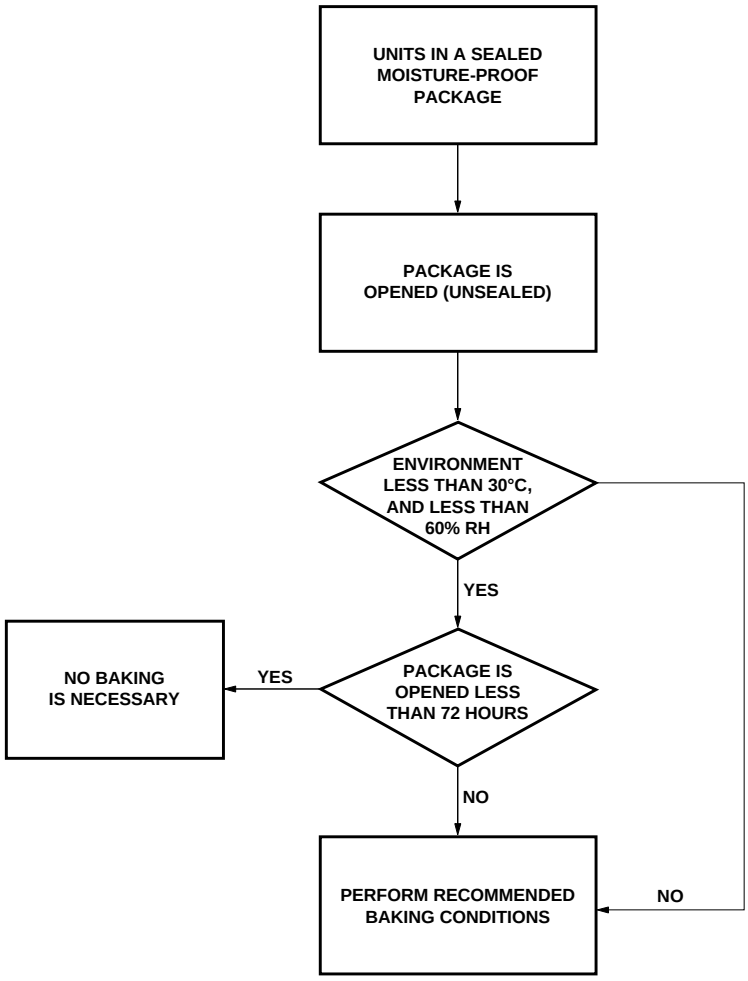


Figure 16. Baking conditions chart.

Baking Conditions

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Package	Temp.	Time
In reels	60°C	≥ 48 hours
In bulk	100°C	≥ 4 hours
	125°C	≥ 2 hours
	150°C	≥ 1 hour

Baking should only be done once.

Recommended Storage Conditions

Storage Temperature	10°C to 30°C
Relative Humidity	below 60% RH

Time from Unsealing to Soldering

After removal from the bag, the parts should be soldered within three days if stored at the recommended storage conditions.

Recommended Reflow Profile

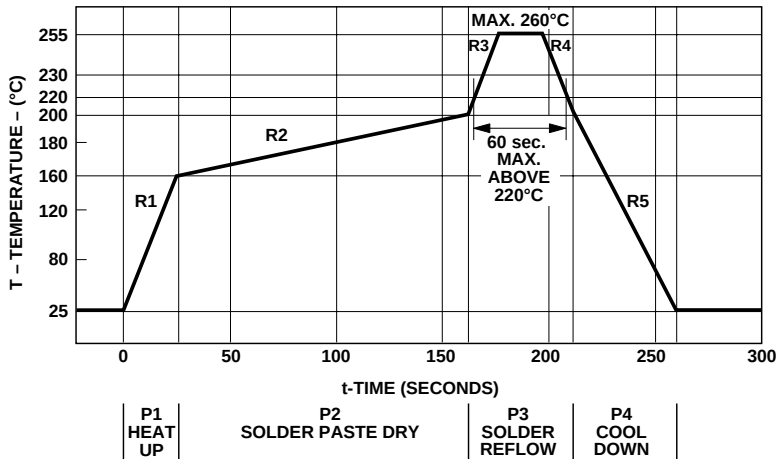


Figure 17. Reflow graph.

Process Zone	Symbol	ΔT	Maximum ΔT/Δtime
Heat Up	P1, R1	25°C to 160°C	4°C/s
Solder Paste Dry	P2, R2	160°C to 200°C	0.5°C/s
Solder Reflow	P3, R3	200°C to 255°C (260°C at 10 seconds max.)	4°C/s
	P3, R4	255°C to 200°C	–6°C/s
Cool Down	P4, R5	200°C to 25°C	–6°C/s

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different ΔT/Δtime temperature change rates. The ΔT/Δtime rates are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In **process zone P1**, the PC board and HSDL-3208 castellation I/O pins are heated to a temperature of 160°C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 4°C per second to allow for even heating of both the PC board and HSDL-3208 castellation I/O pins.

Process zone P2 should be of sufficient time duration (60 to 120 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder, usually 200°C (392°F).

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of solder to 255°C (491°F) for optimum results. The dwell time above the liquidus point of solder should be between 20 and 60 seconds. It usually takes about 20 seconds to assure proper coalescing of the solder balls into liquid solder and the formation of good solder connections. Beyond a dwell time of 60 seconds, the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder, usually 200°C (392°F), to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25°C (77°F) should not exceed 6°C per second maximum. This limitation is necessary to allow the PC board and HSDL-3208 castellation I/O pins to change dimensions evenly, putting minimal stresses on the HSDL-3208 transceiver.

HSDL-3208 (Unshielded)

1.0 Solder Pad, Mask and Metal Stencil Aperture

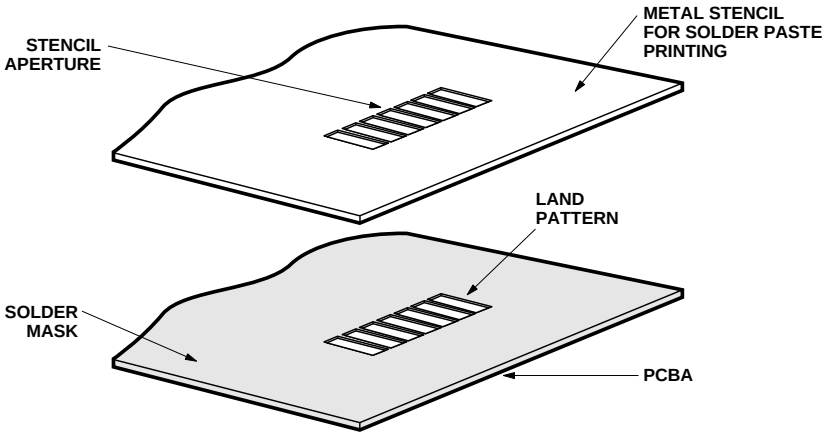


Figure 18. Stencil and PCBA.

1.1 Recommended Land Pattern

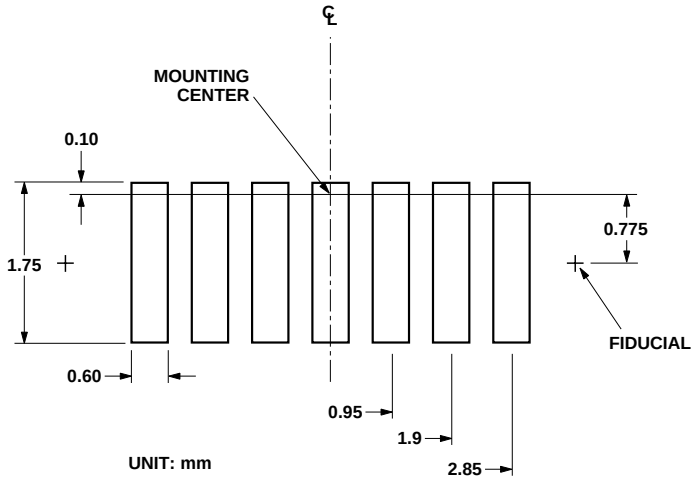


Figure 19. Stencil and PCBA.

1.2 Recommended Metal Solder Stencil Aperture

It is recommended that only a 0.152 mm (0.006 inches) or a 0.127 mm (0.005 inches) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. See the table below the drawing for combinations of metal stencil aperture and metal stencil thickness that should be used.

Aperture opening for shield pad is 2.7 mm x 1.25 mm as per land pattern.

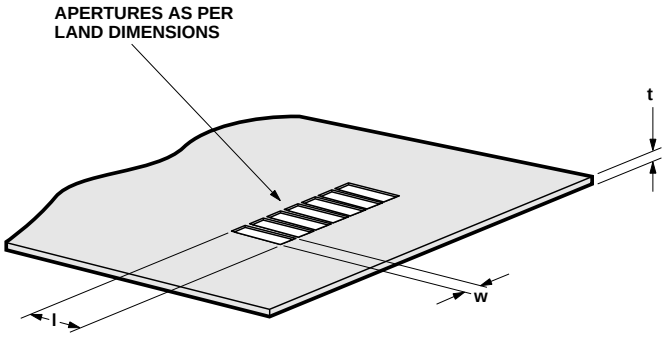


Figure 20. Solder stencil aperture.

	Aperture size(mm)	
Stencil thickness, t (mm)	**length, l**	**width, w**
0.152 mm	2.60 ± 0.05	0.55 ± 0.05
0.127 mm	3.00 ± 0.05	0.55 ± 0.05

1.3 Adjacent Land Keepout and Solder Mask Areas

Adjacent land keep-out is the **maximum space** occupied by the unit relative to the land pattern. There should be no other SMD components within this area.

The minimum solder resist strip width required to avoid solder bridging adjacent pads is **0.2 mm.** It is recommended that two fiducial crosses be placed at mid-length of the pads for unit alignment.

Note: Wet/Liquid Photo-Imageable solder resist/mask is recommended.

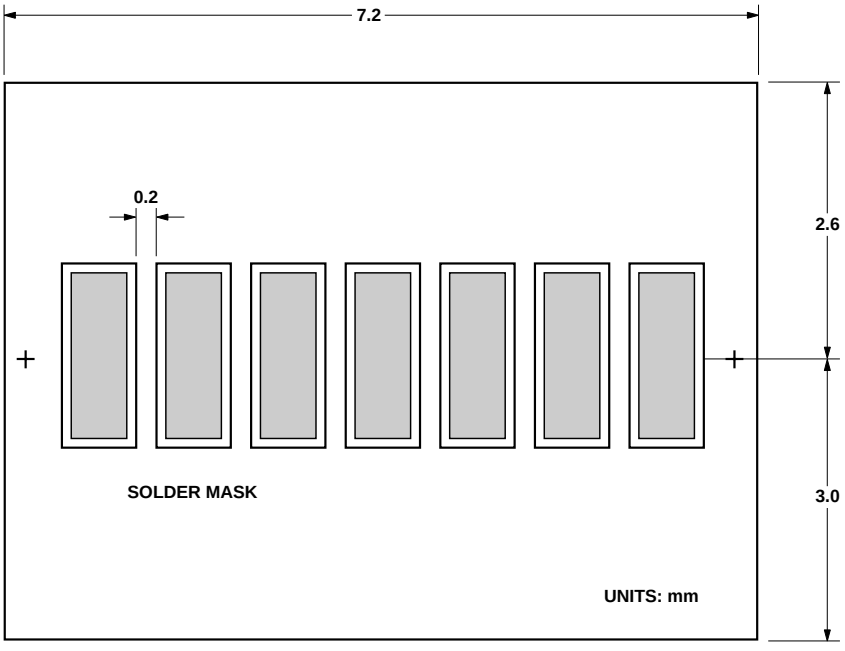


Figure 21. Adjacent land keepout and solder mask areas.

Appendix A : SMT Assembly Application Note HSDL-3208 (Shielded)

2.0 Solder Pad, Mask and Metal Stencil Aperture

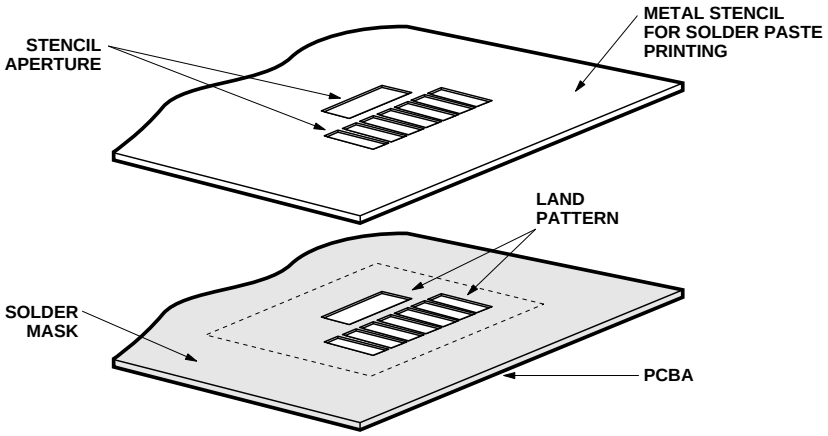


Figure 22. Stencil and PCBA.

2.1 Recommended Land Pattern

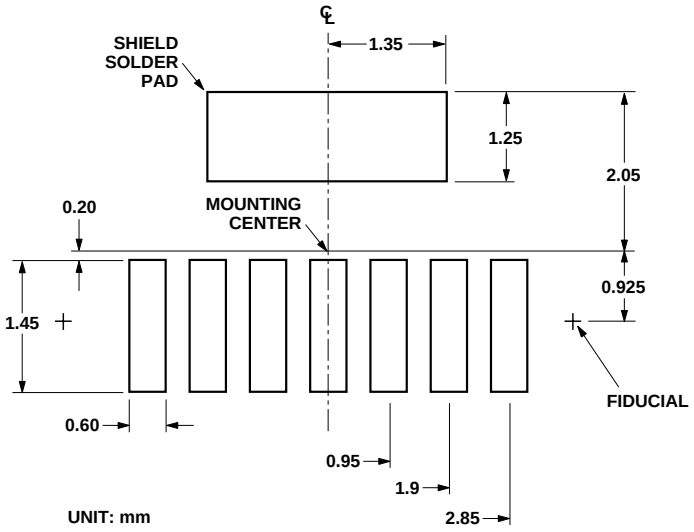


Figure 23. Land Pattern.

2.2 Recommended Metal Solder Stencil Aperture

It is recommended that only a 0.152 mm (0.006 inches) or a 0.127 mm (0.005 inches) thick stencil be used for solder paste printing. This is to ensure adequate printed solder paste volume and no shorting. See the table below the drawing for combinations of metal stencil aperture and metal stencil thickness that should be used.

Aperture opening for shield pad is 2.7 mm x 1.25 mm as per land pattern.

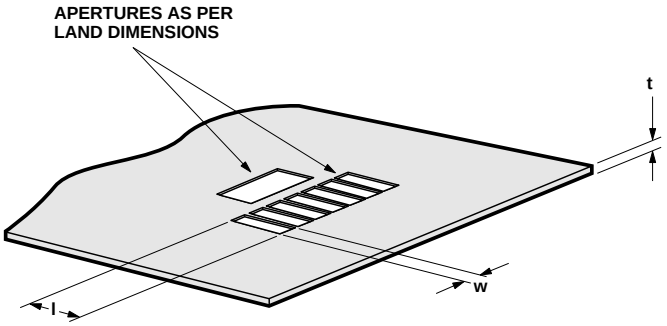


Figure 24. Solder stencil aperture.

	Aperture size(mm)	
Stencil thickness, t (mm)	**length, l**	**width, w**
0.152 mm	1.45 ± 0.05	0.55 ± 0.05
0.127 mm	1.45 ± 0.05	0.55 ± 0.05

2.3 Adjacent Land Keepout and Solder Mask Areas

Adjacent land keep-out is the **maximum space** occupied by the unit relative to the land pattern. There should be no other SMD components within this area.

The minimum solder resist strip width required to avoid solder bridging adjacent pads is **0.2 mm.** It is recommended that two fiducial crosses be placed at mid-length of the pads for unit alignment.

Note: Wet/Liquid Photo-Imageable solder resist/mask is recommended.

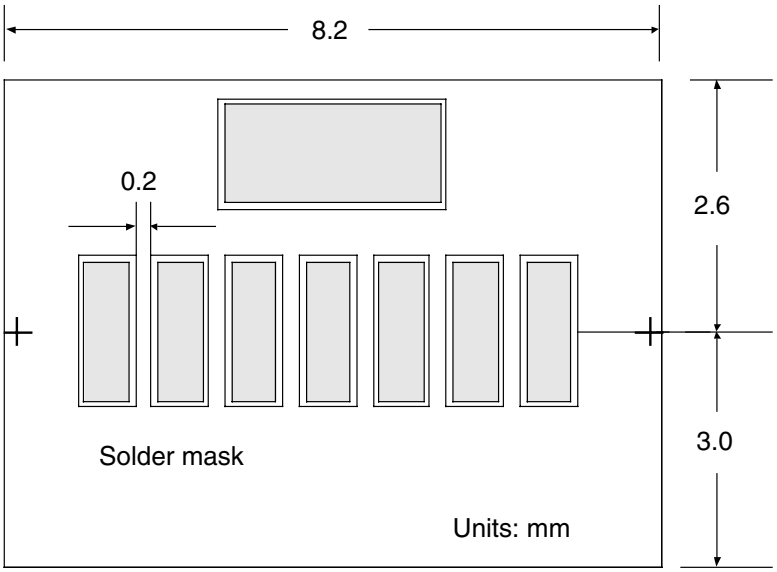


Figure 25. Adjacent land keepout and solder mask areas.

Appendix B: PCB Layout Suggestion

The HSDL-3208 is a shieldless part and hence does not contain a shield trace, unlike the other transceivers. The following PCB layout guidelines should be followed to obtain a good PSRR and EM immunity, resulting in good electrical performance. Things to note:

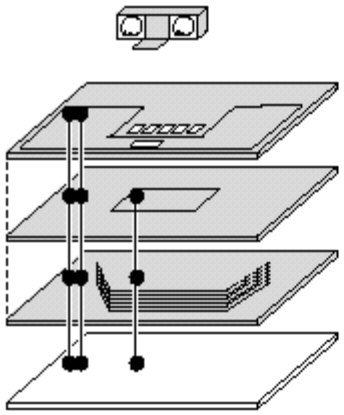
1. The AGND pin should be connected to the ground plane.

2. C1 and C2 are optional supply filter capacitors; they may be left out if a clean power supply is used.

3. VLED can be connected to either unfiltered or unregulated power supply. If VLED and V_{CC} share the same power supply and C1 is used, the connection should be before the current limiting resistor R2. In a noisy environment, including capacitor C2 can enhance supply rejection. C1 is generally a ceramic capacitor of low inductance providing a wide frequency response while C2 is a tantalum capacitor of big volume and fast frequency response. The use of a tantalum capacitor is more critical on the V_{LED} line, which carries a high current.

4. Preferably a multi-layered board should be used to provide sufficient ground plane. Use the layer underneath and near the transceiver module as V_{CC}, and sandwich that layer between ground connected board layers. Refer to the diagram below for an example of a 4-layer board.

The area underneath the module at the second layer, and 3 cm in all directions around the module, is defined as the critical ground plane zone. The ground plane should be maximized in this zone. Refer to application note AN1114 or the *Lite-On IrDA Data Link Design Guide* for details. The layout below is based on a 2-layer PCB.

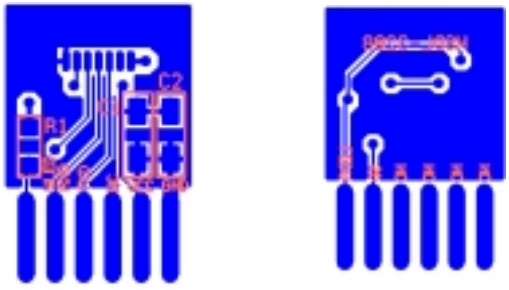


TOP LAYER
CONNECT THE METAL SHIELD AND MODULE GROUND PIN TO BOTTOM GROUND LAYER.

LAYER 2
CRITICAL GROUND PLANE ZONE. DO NOT CONNECT DIRECTLY TO THE MODULE GROUND PIN.

LAYER 3
KEEP DATA BUS AWAY FROM CRITICAL GROUND PLANE ZONE.

BOTTOM LAYER (GND)



Top View

Bottom View

Figure 26. PCB layout suggestion.

Appendix C : General Application Guide for the HSDL-3208 Infrared IrDA® Compliant 115.2 kb/s Transceiver

Description

The HSDL-3208 is an ultra-small low-cost infrared transceiver module that provides the interface between logic and infrared (IR) signals for through air, serial, half-duplex IR data link. The device is designed to address the mobile computing market such as PDAs, as well as small embedded mobile products such as digital cameras and cellular phones. It is fully compliant to IrDA 1.4 low power specification from 9.6 kb/s to 115.2 kb/s, and supports HP-SIR and TV Remote modes. The design of the HSDL-3208 also includes the following unique features:

- Low passive component count
- Shutdown mode for low power consumption requirement

Selection of Resistor R1

Resistor R1 should be selected to provide the appropriate peak pulse LED current over different ranges of V_{CC} as shown in the table below.

Recommended R1	V_{CC}	Intensity	Minimum Peak Pulse LED Current
30 Ω	3.3 V	9 mW/Sr	50 mA

Interface to Recommended I/O Chips

The HSDL-3208's TXD data input is buffered to allow for CMOS drive levels. No peaking circuit or capacitor is required.

Data rate from 9.6 kb/s up to 115.2 kb/s is available at the RXD pin.

The diagram below shows how the IR port fits into the mobile phone platform and PDA platform.

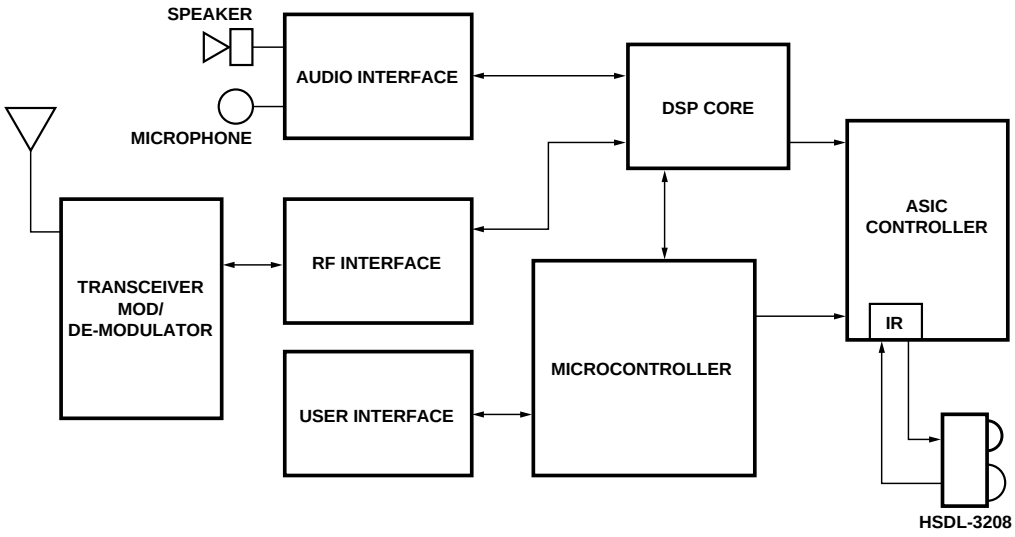


Figure 27. IR layout in mobile phone platform.

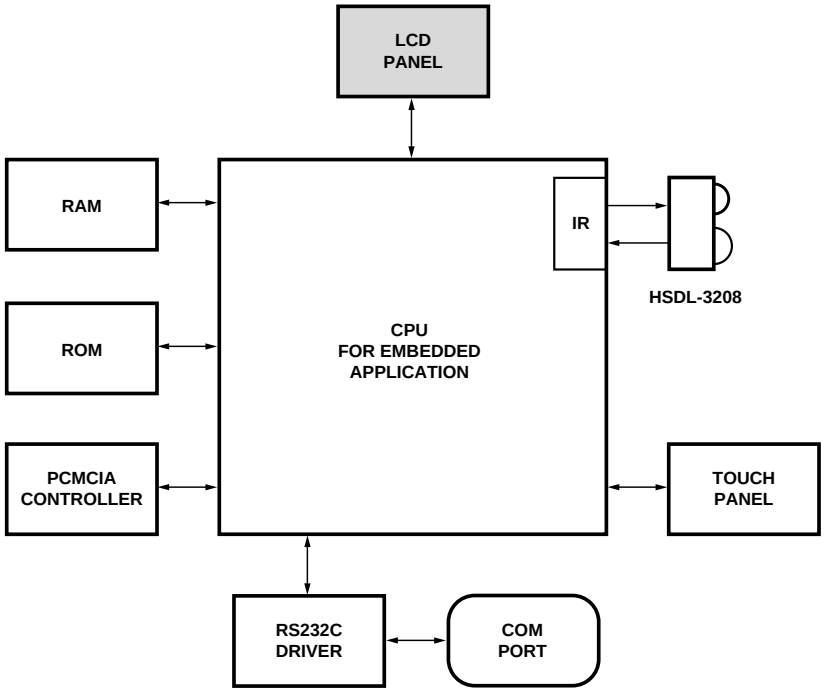


Figure 28. IR layout in PDA platform.

The link distance testing is done using typical HSDL-3208 units with National Semiconductor's PC87109 3V Super I/O Controller and SMC's FDC37C669 and FDC37N769 Super I/O controllers. An 115.2 kb/s datarate IR link distance of up to 40 cm has been demonstrated.

Appendix D: Window Designs for HSDL-3208

Optical port dimensions for HSDL-3208:

To ensure IrDA compliance, some constraints on the height and width of the window exist. The minimum dimensions ensure that the IrDA cone angles are met without vignetting. The maximum dimensions minimize the effects of stray light. The minimum size corresponds to a cone angle of 30° and the maximum size corresponds to a cone angle of 60°.

In the figure below, X is the width of the window, Y is the height of the window and Z is the distance from the HSDL-3208 to the back of the window. The distance from the center of the LED lens to the center of the photodiode lens, K, is 5.1 mm. The equations for computing the window dimensions are as follows:

$$X = K + 2*(Z + D)*\tan A$$

$$Y = 2*(Z + D)*\tan A$$

The above equations assume that the thickness of the window is negligible compared to the distance of the module from the back of the window (Z). If they are comparable, Z' replaces Z in the above equation. Z' is defined as

$$Z' = Z + t/n$$

where 't' is the thickness of the window and 'n' is the refractive index of the window material.

The depth of the LED image inside the HSDL-3208, D, is 3.17 mm. 'A' is the required half angle for viewing. For IrDA compliance, the minimum is 150 and the maximum is 300. Assuming the thickness of the window to be negligible, the equations result in the following tables and graphs:

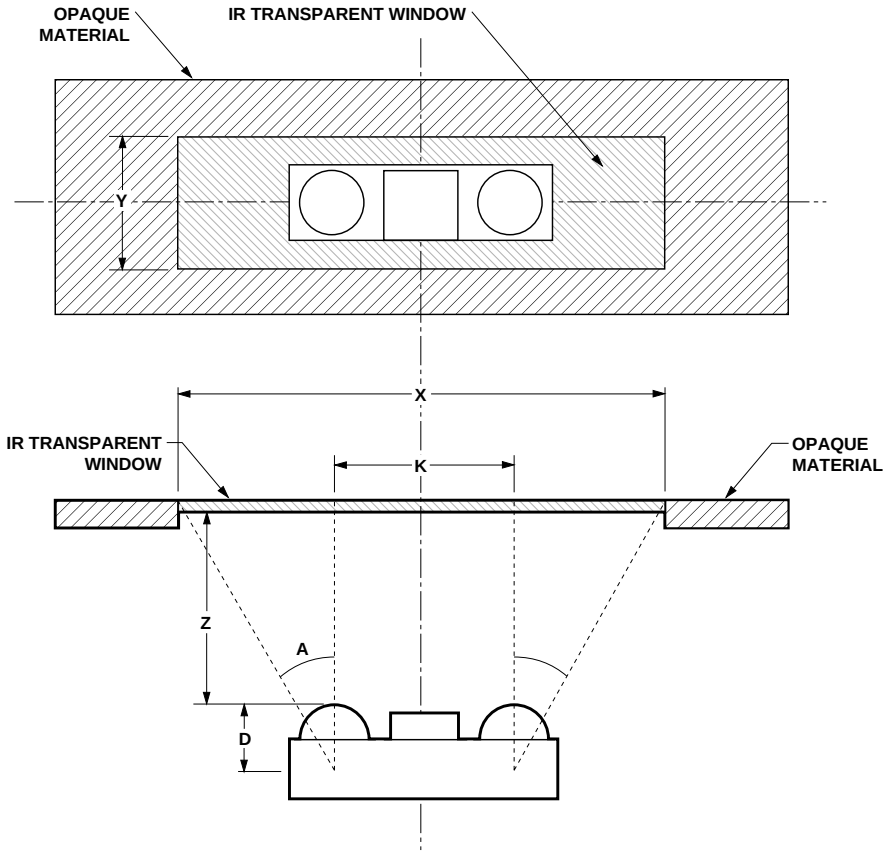


Figure 29. Window design diagram.

Module Depth	Aperture Width (x, mm)		Aperture Height (y, mm)	
(z) mm	Max.	Min.	Max.	Min.
0	8.76	6.80	3.66	1.70
1	9.92	7.33	4.82	2.33
2	11.07	7.87	5.97	2.77
3	12.22	8.41	7.12	3.31
4	13.38	8.94	8.28	3.84
5	14.53	9.48	9.43	4.38
6	15.69	10.01	10.59	4.91
7	16.84	10.55	11.74	5.45
8	18.00	11.09	12.90	5.99
9	19.15	11.62	14.05	6.52

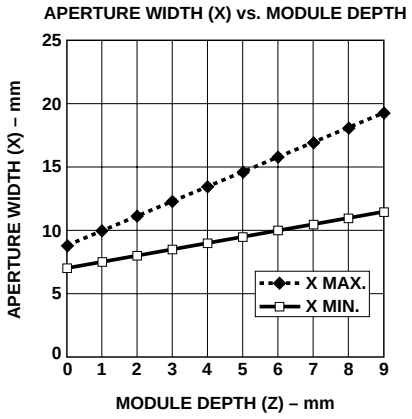


Figure 30. Aperture width (X) vs. module depth.

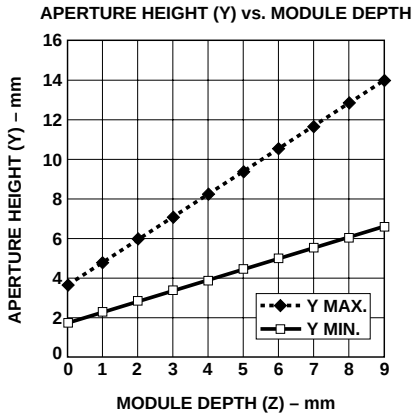


Figure 31. Aperture height (Y) vs. module depth.

Window Material

Almost any plastic material will work as a window material. Polycarbonate is recommended. The surface finish of the plastic should be smooth, without any texture. An IR filter dye may be used in the window to make it look black to the eye, but the total optical loss of the window should be 10% or less for best optical performance. Light loss should be measured at 875 nm.

The recommended plastic materials for use as a cosmetic window are available from General Electric Plastics.

Recommended Plastic Materials:

Material Number	Light Transmission	Haze	Refractive Index
Lexan 141L	88%	1%	1.586
Lexan 920A	85%	1%	1.586
Lexan 940A	85%	1%	1.586

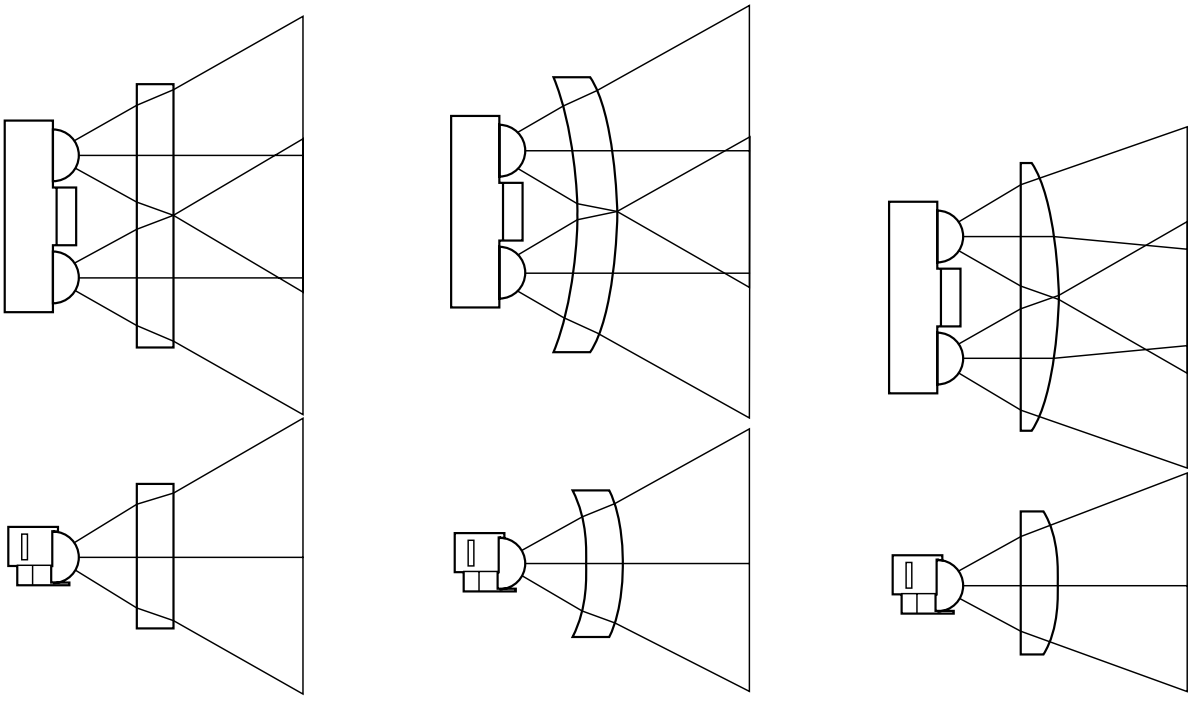
Note: 920A and 940A are more flame retardant than 141L.
Recommended Dye: Violet #21051 (IR transmissant above 625 nm).

Shape of the Window

From an optics standpoint, the window should be flat. This ensures that the window will not alter either the radiation pattern of the LED, or the receive pattern of the photodiode.

If the window must be curved for mechanical or industrial design reasons, place the same curve on the back side of the window that has an identical radius as the front side. While this will not completely eliminate the lens effect of the front curved surface, it will significantly reduce the effects. The amount of change in the radiation pattern is dependent upon the material chosen for the window, the radius of the front and back curves, and the distance from the back surface to the transceiver. Once these items are known, a lens design can be made which will eliminate the effect of the front surface curve.

The following drawings show the effects of a curved window on the radiation pattern. In all cases, the center thickness of the window is 1.5 mm, the window is made of polycarbonate plastic, and the distance from the transceiver to the back surface of the window is 3 mm.



Flat Window (First Choice)

Curved Front and Back (Second Choice)

Curved Front, Flat Back (Do Not Use)

Figure 32. Shape of windows.

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