ORDERING INFORMATION

Part Number	Package Markings	T_J Rating	Package Description
EP53F8QI	APXX	-40°C to +125°C	16-pin (3mm x 3mm x 1.1mm) QFN
EVB-EP53F8QI		QFN Evaluation Board	

Packing and Marking Information: https://www.Intel.com/support/quality-and-reliability/packing.html

PIN FUNCTIONS

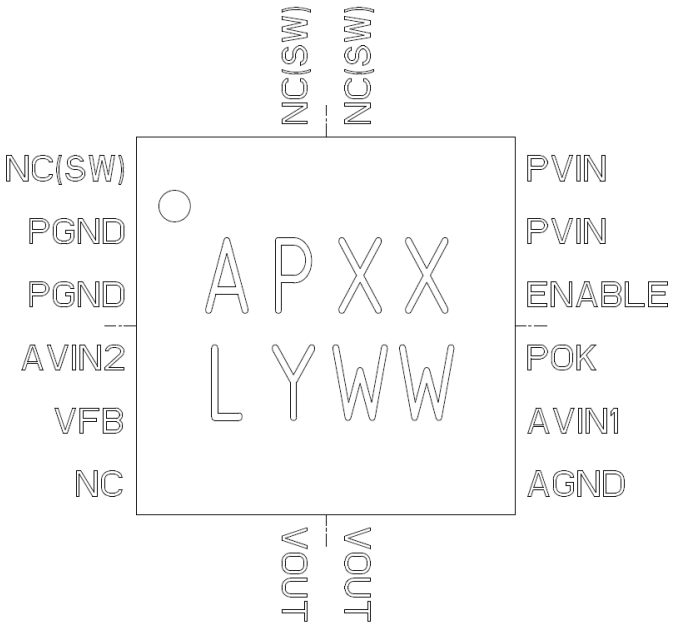


Figure 3. Pin Out Diagram (Top View)

NOTE A: NC pins are not to be electrically connected to each other or to any external signal, ground or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage.

NOTE B: White 'dot' on top left is pin 1 indicator on top of the device package.

PIN DESCRIPTIONS

PIN	NAME	TYPE	FUNCTION
1, 15, 16	NC(SW)	-	NO CONNECT – These pins are internally connected to the common switching node of the internal MOSFETs. NC (SW) pins are not to be electrically connected to any external signal, ground, or voltage. However, they must be soldered to the PCB. Failure to follow this guideline may result in part malfunction or damage to the device.
2, 3	PGND	Ground	Input/Output Power Ground. Connect these pins to the ground electrode of the input and output filter capacitors. Refer to Layout Considerations section for details.
4	AVIN2	Power	Analog input voltage. Connect to AVIN1 only.
5	VFB	Analog	Feedback Pin for External Voltage Divider Network. Connect a resistor divider to this pin to set the output voltage. Use 237 kΩ, 1% or better for the upper resistor.
6	NC	-	No Connect.
7,8	VOUT	Power	Voltage and Power Output. Connect these pins to output capacitor(s).
9	AGND	Ground	Analog Ground for the Controller Circuits
10	AVIN1	Power	Analog Voltage Input for the Controller Circuits. Connect this pin to PVIN with a 10Ω resistor. Connect a 1 µF capacitor between this pin and AGND. Connect AVIN2 to this pin.
11	POK	Digital	Power OK with an Open Drain Output. Refer to Power OK section.
12	ENABLE	Analog	Input Enable. A logic high signal on this pin enables the output and initiates a soft start. A logic low signal disables the output and discharges the output to GND. The ENABLE pin should not be left floating as it could be in an unknown and random state. It is recommended to enable the device after both PVIN and AVIN is in regulation. See ENABLE operation for details.
13-14	PVIN	Power	Input Power Supply. Connect to input supply. Decouple with input capacitor(s) to PGND.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS
Voltages on: PVIN, AVIN, VOUT		-0.3	6.5	V
Voltages on: ENABLE, POK		-0.3	V_{IN}	V
Voltage on: VFB		-0.3	2.7	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Ambient Operating Range		-40	+85	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	2.4	5.5	V
Output Voltage Range	V_{OUT}	0.6	V_{IN} - V_{DO}(1)	V
Output Current	I_{LOAD}	0	1500	mA
Operating Ambient Temperature Range	T_A	-40	+85	°C
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Resistance: Junction to Ambient –0 LFM (2)	θ_{JA}	55	°C/W
Thermal Shutdown (Junction Temperature)	T_{SD}	155	°C
Thermal Shutdown Hysteresis	T_{SDH}	15	°C

(1) $V_{DROPOUT}$ is defined as (I_{LOAD} x Dropout Resistance) including temperature effect
(2) Based on a 2 oz. copper board and proper thermal design in line with JEDEC EIJ/JESD51 standards

ELECTRICAL CHARACTERISTICS

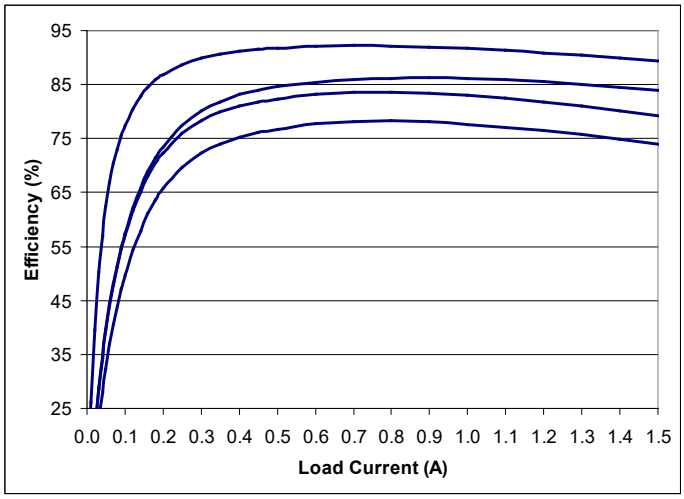
NOTE: T_A = -40°C to +85°C unless otherwise noted. Typical values for V_{IN} = 5V and T_A =25°C, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}		2.4		5.5	V
Under Voltage Lock-Out – V_{IN} Rising	V_{UVLOR}			2.2		V
Under Voltage Lock-Out – V_{IN} Falling	V_{UVLOF}			2.1		V/ms
VFB Voltage Initial Accuracy	V_{FB}	T_A = 25 °C; V_{IN} = 5V I_{LOAD} = 100 mA	0.588	0.600	0.612	V
Line Regulation		2.4 V ≤ V_{IN} ≤ 5.5V		0.31		%/V
Load Regulation		I_{LOAD} = 0 to 1.5A		0.420		%/A
Temperature Variation		-40°C ≤ T_A ≤ +85°C		0.0012		%/°C
Typical Accuracy		-40°C ≤ T_A ≤ +85°C; 0.5A ≤ I_{LOAD} ≤ 1.0A; 4.5V ≤ V_{IN} ≤ 5.5V; 0.95V ≤ V_{OUT} ≤ 1.5V;		1.5		%
V_{OUT} Rise Time	T_{RISE}	From time ENABLE goes high	0.78	1.2	1.62	mS
VFB, ENABLE, Pin Input Current [3]		-40°C ≤ T_A ≤ +85°C	-40		+40	nA
ENABLE Voltage Threshold		Logic Low	0.0		0.4	V
VFB Pin Voltage (Load and Temperature)	V_{VFB}	Logic High	1.4		V_{IN}	V
Continuous Output Current					1500	mA
Peak Output Current		1.0V ≤ V_{OUT} ≤ 1.5V; <21ms			1800	mA
POK Upper Threshold		V_{OUT} Rising		111		%
POK Upper Threshold		V_{OUT} Falling		102		%
POK Lower Threshold		V_{OUT} Rising; percent of V_{OUT} Nominal		92		%
POK Lower Threshold		V_{OUT} Falling; percent of V_{OUT} Nominal		90		%

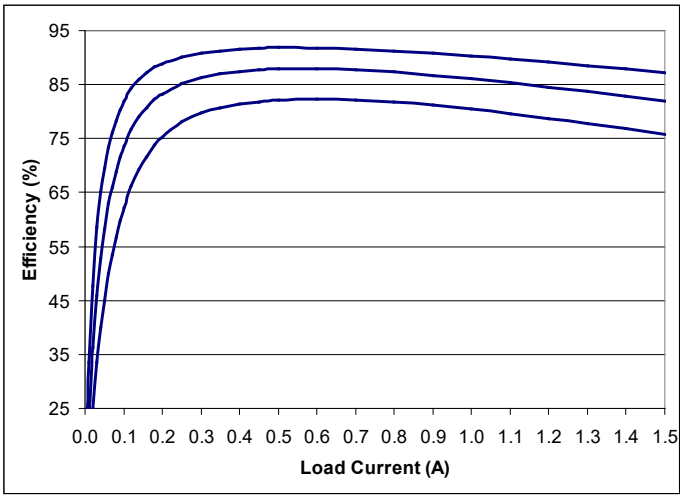
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POK Low Voltage		I_{SINK} = 5 mA, -40°C ≤ T_A ≤ +85°C		0.15	0.4	V
POK Pin V_{OH} Leakage Current		POK High, -40°C ≤ T_A ≤ +85°C			500	nA
Shutdown Current		ENABLE Low		14		µA
Current Limit Threshold		2.4 V ≤ V_{IN} ≤ 5.5 V, -40°C ≤ T_A ≤ +85°C	2.0	3.2		A
Dropout Resistance				250	360	mΩ
Operating Frequency	F_{OSC}			4		MHz

(3) VFB, ENABLE pin input current specification is guaranteed by design.

TYPICAL PERFORMANCE CURVES

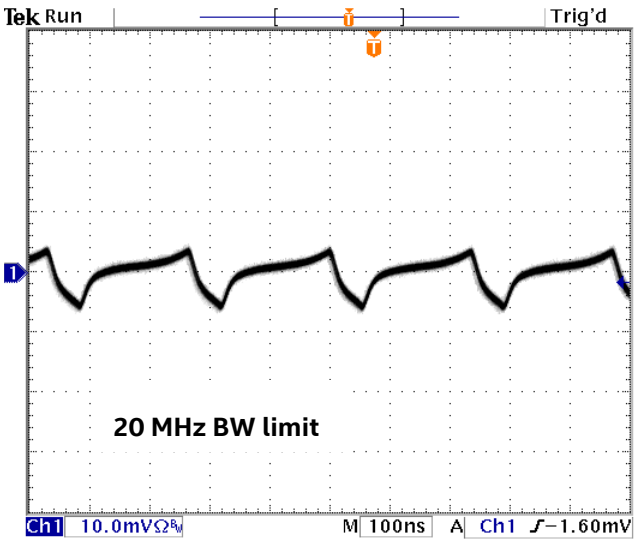


Efficiency vs. Load Current: V_{IN} = 5.0V, V_{OUT} (from top to bottom) = 3.7, 2.5V, 1.8V, 1.2V

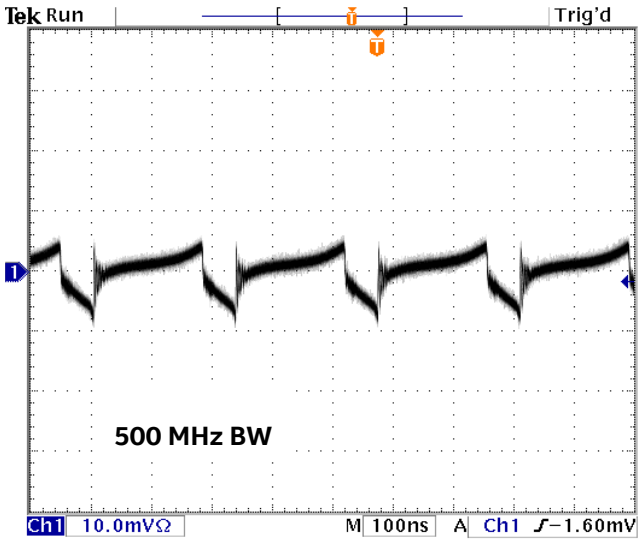


Efficiency vs. Load Current: V_{IN} = 3.3V, V_{OUT} (from top to bottom) = 2.5V, 1.8V, 1.2V

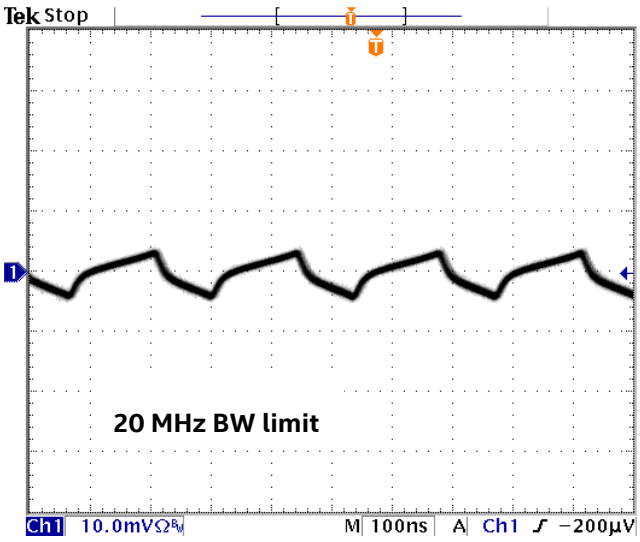
TYPICAL PERFORMANCE CHARACTERISTICS



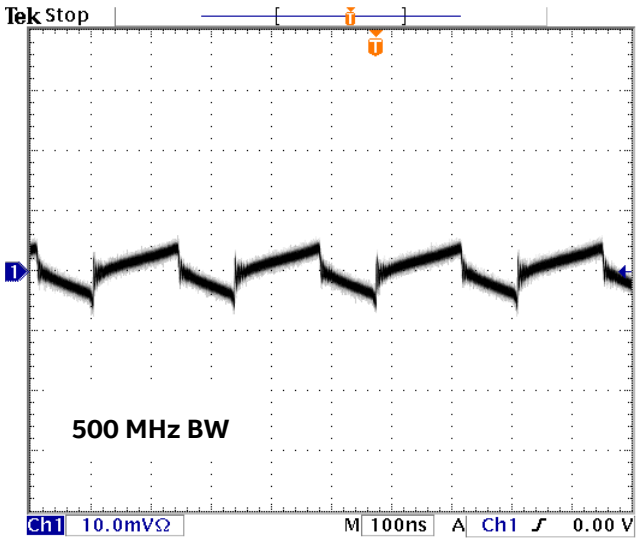
Output Ripple: V_{IN} = 5V, V_{OUT} = 3.7V, I_{LOAD} = 900mA



Output Ripple: V_{IN} = 5V, V_{OUT} = 3.7V, I_{LOAD} = 900mA

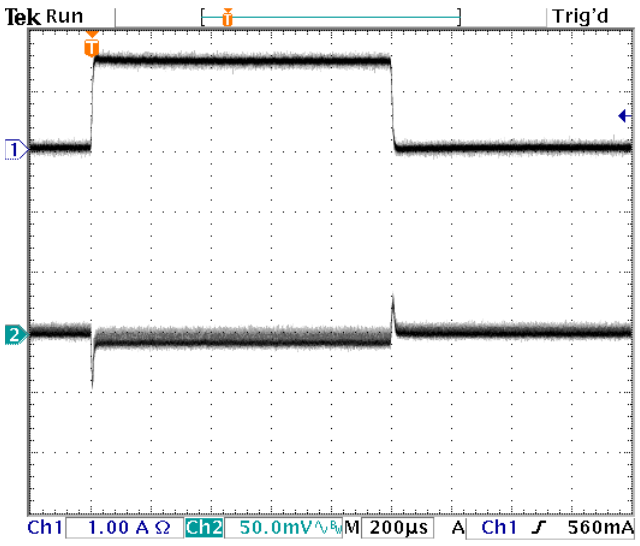


Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{LOAD} = 900mA

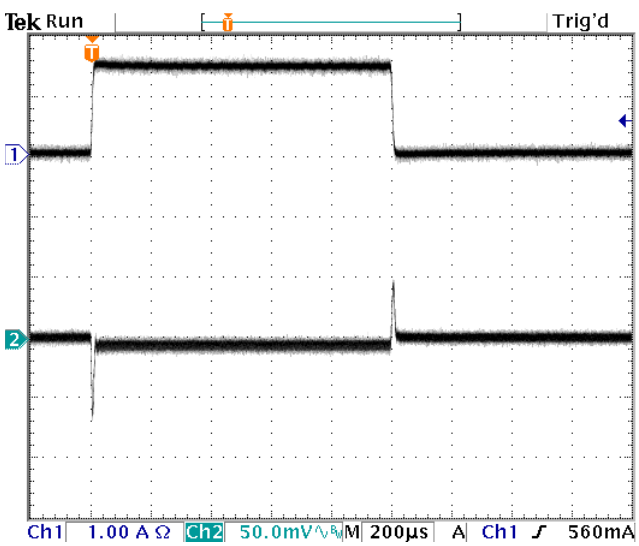


Output Ripple: V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{LOAD} = 900mA

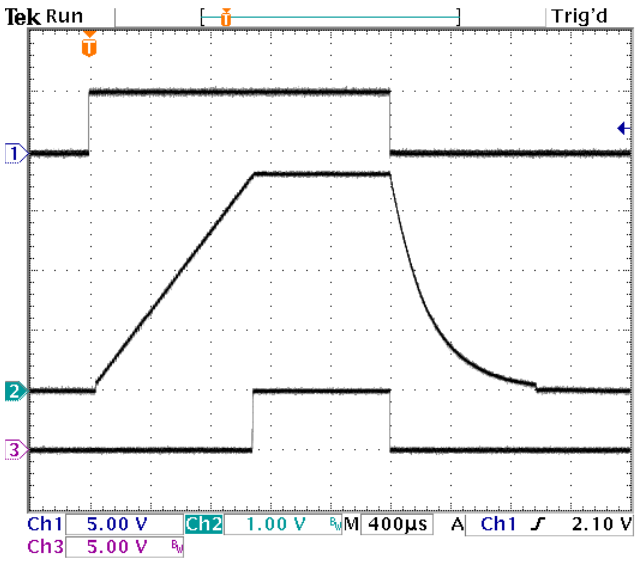
TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)



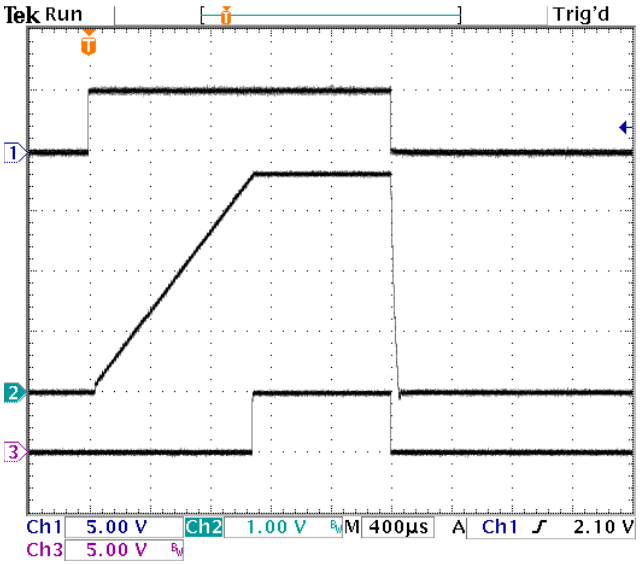
Transient Response: V_{IN} = 5.0V, V_{OUT} = 1.2V, Load Step 0 to 1.5A



Transient Response: V_{IN} = 3.3V, V_{OUT} = 1.8V, Load Step 0 to 1.5A



Startup and Shutdown Waveform V_{IN} = 5.0V, V_{OUT} = 3.7V, I_{LOAD} = 0mA



Startup and Shutdown Waveform V_{IN} = 5.0V, V_{OUT} = 3.7V, I_{LOAD} = 900mA

(4) Application Circuit in Figure 1 used for typical performance characteristics.

FUNCTIONAL BLOCK DIAGRAM

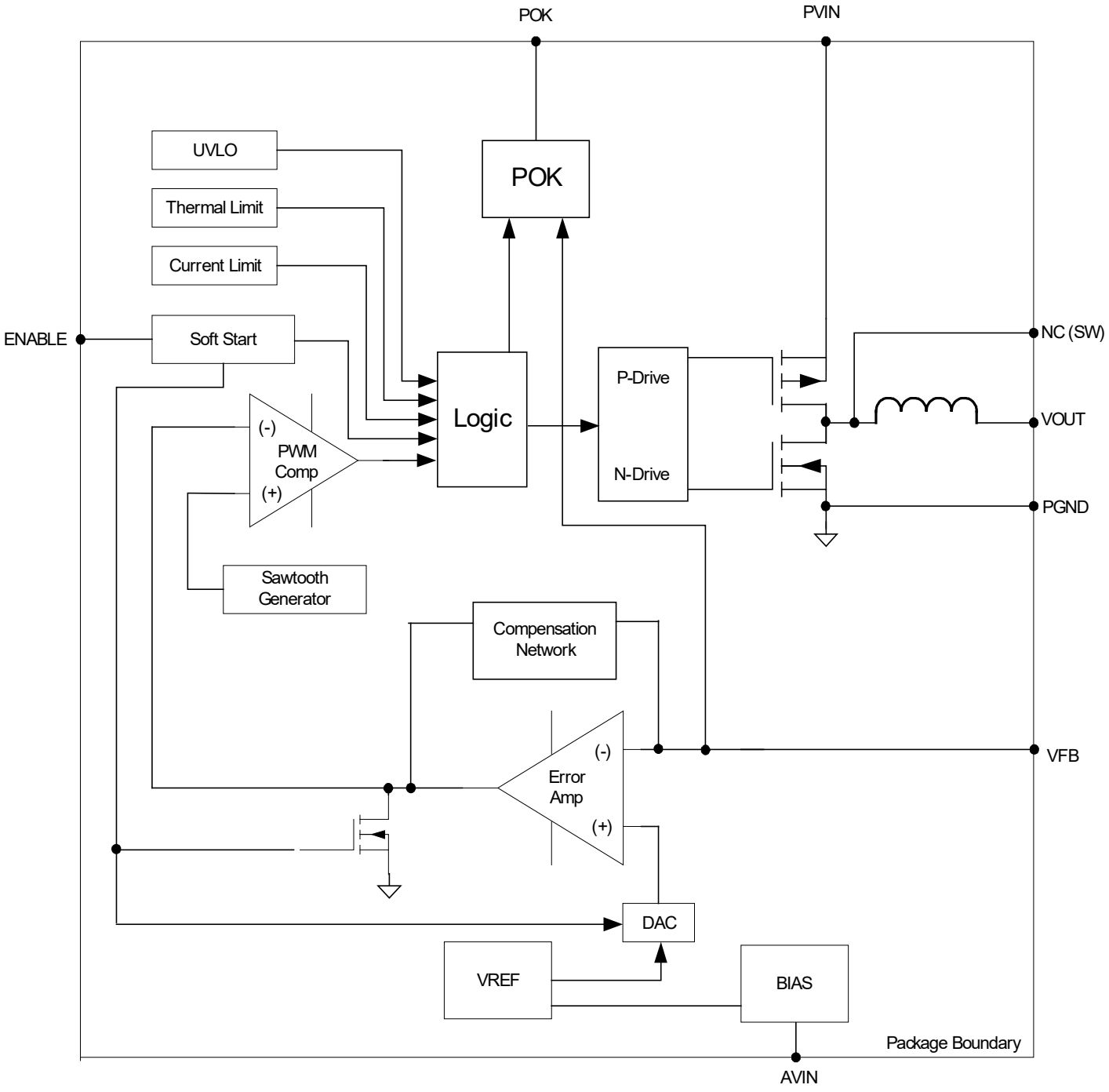


Figure 4. Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous DC-DC Step-Down PowerSoC

The EP53F8QI leverages advanced CMOS technology to provide high switching frequency, while also maintaining high efficiency.

Packaged in a 3 mm x 3 mm x 1.1 mm QFN, the EP53F8QI provides a high degree of flexibility in circuit design while maintaining a very small footprint. High switching frequency allows for the use of very small MLCC input and output filter capacitors.

The converter uses voltage mode control to provide high noise immunity, low output impedance and excellent load transient response. Most compensation components are integrated into the device, requiring only a single external compensation capacitor.

Output voltage is programmed via an external resistor divider. Output voltage can be programmed from 0.6V to V_{IN}-$V_{DROPOUT}$.

POK monitors the output voltage and signals if it is within ±10% of nominal. Protection features include under voltage lockout (UVLO), over current protection, short circuit protection, and thermal overload protection.

Stability over Wide Range of Operating Conditions

The EP53F8QI utilizes an internal compensation network and is designed to provide stable operation over a wide range of operating conditions. The high switching frequency allows for a wide control loop bandwidth. To improve transient performance or reduce output voltage ripple with dynamic loads you have the option to add supplementary capacitance to the output. Please refer to the section on soft start for limitations on output capacitance.

Soft Start

The EP53F8QI has an internal soft-start circuit that controls the ramp of the output voltage. The control circuitry limits the V_{OUT} ramp rate to levels that are safe for the Power MOSFETS and the integrated inductor.

The device has a constant VOUT ramp time. Therefore, the ramp rate will vary with the output voltage setting. Output voltage ramp time is given in the Electrical Characteristics Table.

Excess bulk capacitance on the output of the device can cause an over-current condition at startup. Maximum allowable output capacitance depends on the device's minimum current limit as indicated in the Electrical Characteristics Table, the output current at startup, the minimum soft-start time also in the Electrical Characteristics Table and the output voltage. The total maximum capacitance on the output rail is estimated by the equation below:

$C_{OUT\_MAX} = 0.7 * (I_{LIMIT} - I_{OUT}) * t_{SS} / V_{OUT}$

C_{OUT_MAX} = maximum allowable output capacitance

I_{LIMIT} = minimum current limit = 2.0A

I_{OUT} = output current at startup

t_{SS} = minimum soft-start time = 0.78ms

V_{OUT} = output voltage

NOTE: Device stability still needs to be verified in the application if extra bulk capacitors are added to the output rail.

Over Current/Short Circuit Protection

When an over current condition occurs, V_{OUT} is pulled low. This condition is maintained for a period of 1.2 ms and then a normal soft start cycle is initiated. If the over current condition still persists, this cycle will repeat.

Under Voltage Lockout

An under voltage lockout circuit will hold off switching during initial power up until the input voltage reaches sufficient level to ensure proper operation. If the voltage drops below the UVLO threshold the lockout circuitry will again disable switching. Hysteresis is included to prevent chattering between UVLO high and low states.

Enable

The ENABLE pin provides means to shut down the converter or initiate normal operation. A logic high will enable the converter to go through the soft start cycle and regulate the output voltage to the desired value. A logic low will allow the device to discharge the output and go into shutdown mode for minimal power consumption. When the output is discharged, an auxiliary NFET turns on and limits the discharge current to 300 mA or below. The ENABLE pin should not be left floating as it could be in an unknown and random state. It is recommended to enable the device after both PVIN and AVIN is in regulation. At extremely cold conditions below -30°C, the controller may not be properly powered if ENABLE is tied directly to AVIN during startup. It is recommended to use an external RC circuit to delay the ENABLE voltage rise so that the internal controller has time to startup into regulation (see circuit below). The RC circuit may be adjusted so that AVIN and PVIN are above UVLO before ENABLE is high. The startup time will be delayed by the extra time it takes for the capacitor voltage to reach the ENABLE threshold.

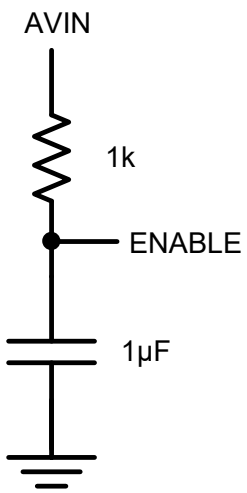


Figure 5. ENABLE Delay Circuit

Thermal Shutdown

When excessive power is dissipated in the device, its junction temperature rises. Once the junction temperature exceeds the thermal shutdown temperature, the thermal shutdown circuit turns off the converter, allowing the device to cool. When the junction temperature decreases to a safe operating level, the device will be re-enabled and go through a normal startup process. The specific thermal shutdown junction temperature and hysteresis can be found in the thermal characteristics table.

Power OK

The EP53F8QI provides an open drain output to indicate if the output voltage stays within 92% to 111% of the set value. Within this range, the POK output is allowed to be pulled high. Outside this range, POK remains low. However, during transitions such as power up, power down, and dynamic voltage scaling, the POK output will not change state until the transition is complete for enhanced noise immunity.

The POK has 5mA sink capability for events where it needs to feed a digital controller with standard CMOS inputs. When POK is pulled high, the pin leakage current is as low as 500 nA maximum over temperature. This allows a large pull up resistor such as 100 kΩ to be used for minimal current consumption in shutdown mode.

The POK output can also be conveniently used as an ENABLE input of the next stage for power sequencing of multiple converters.

APPLICATION INFORMATION

Output Voltage Programming

The EP53F8QI uses a simple resistor divider to program the output voltage.

Referring to Figure , use 237 kΩ, 1% or better for the upper resistor (Ra). The value of the bottom resistor (Rb) in kΩ is given as:

$$Rb = \frac{142.2}{V_{OUT} - 0.6} k\Omega$$

Where V_{OUT} is the output voltage. Rb should also be a 1% or better resistor.

A 5.0pF MLCC capacitor is required in parallel with Ra for compensation.

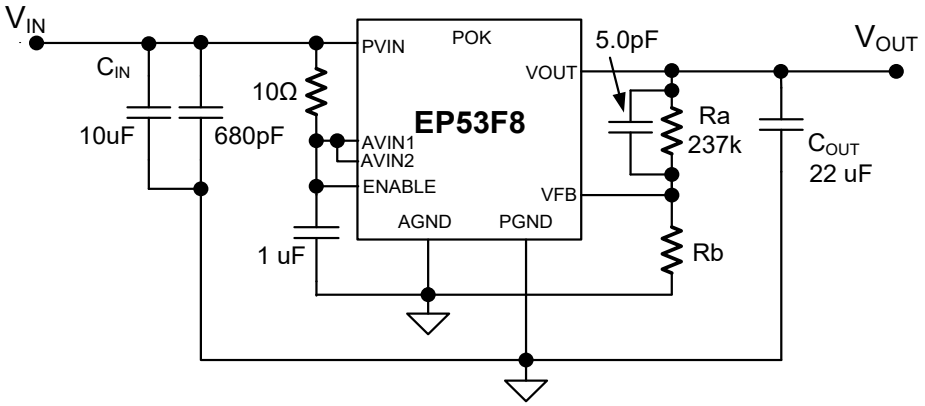


Figure 6. EP53A8HQI VID Application Circuit

Power-Up/Down

During power-up, ENABLE should not be asserted before PVIN, and PVIN should not be asserted before AVIN. The PVIN should never be powered when AVIN is off. During power down, the AVIN should not be powered down before the PVIN. Tying PVIN and AVIN or all three pins (AVIN, PVIN, ENABLE) together during power up or power down meets these requirements.

Startup into Pre-Bias

The EP53F8QI supports startup into a pre-biased output of up to 1.5V. The output of the EP53F8QI can be pre-biased with a voltage up to 1.5V when the EP53F8QI is first enabled.

Input and Output Capacitor Selection

Low ESR MLC capacitors with X5R or X7R or equivalent dielectric should be used for input and output capacitors. Y5V or equivalent dielectrics lose too much capacitance with frequency, DC bias, and temperature. Therefore, they are not suitable for switch-mode DC-DC converter filtering, and must be avoided.

The **input filter capacitor** requirement is a 10µF, 10V 0805 MLCC capacitor in parallel with a 680pF MLCC capacitor. The 680pF capacitor provides additional high frequency decoupling and is manditory. The 680pF capacitor must be placed closest to the EP53F8QI as shown in Figure 6.

The **output filter capacitor** requirement is a 22µF, 6.3V, 0805 MLCC for most applications. The output ripple can be reduced by using 2 x 22µF, 6.3V, 0805 MLC capacitors.

Additional bulk capacitance for decoupling and bypass can be placed at the load as long as there is sufficient separation between the V_{OUT} Sense point and the bulk capacitance.

Excess total capacitance on the output (Output Filter + Bulk) can cause an over-current condition at startup. Refer to the section on Soft-Start for the maximum total capacitance on the output.

AVIN Decoupling

AVIN should be connected to PVIN using a 10Ω resistor. An 0402 or smaller case size is recommended for this resistor. A 1µF, 10 V, 0402 MLC capacitor should be connected from AVIN to AGND to provide high frequency decoupling for the control circuitry supply for optimal performance.

POK Pull Up Resistor Selection

If the POK signal is required for the application. The POK pin must be pulled up through a resistor to any voltage source that can be as high as V_{IN}. The simplest way is to connect POK to the power input of the converter through a resistor. A 100 kΩ pull up resistor is recommended for most applications for minimal current drain from the voltage source and good noise immunity. POK can sink up to 5mA.

LAYOUT RECOMMENDATIONS

Figure 7 shows critical components and layer 1 traces of a recommended minimum footprint EP53F8QI layout with ENABLE tied to V_{IN}. Alternate ENABLE configurations, and other small signal pins need to be connected and routed according to specific customer application. Please see the Gerber files on the Intel website www.Intel.com/enpirion for exact dimensions and other layers. Please refer to Figure 7 while reading the layout recommendations in this section.

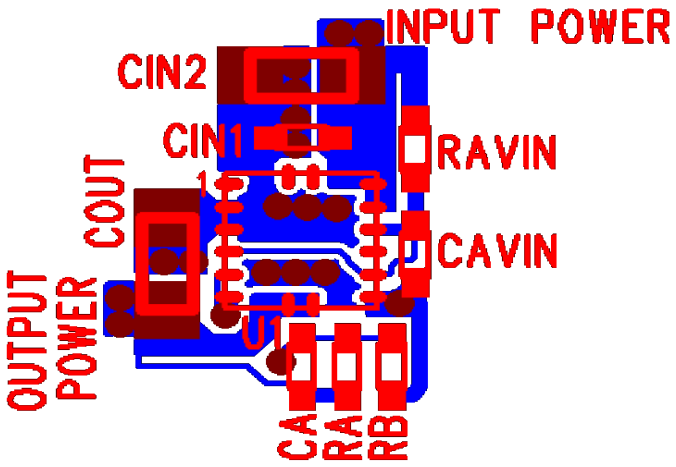


Figure 7. Top PCB Layer Critical Components and Copper for Minimum Footprint (Top View)

Recommendation 1: Input and output filter capacitors should be placed on the same side of the PCB, and as close to the EP53F8QI package as possible. They should be connected to the device with very short and wide traces. Do not use thermal reliefs or spokes when connecting the capacitor pads to the respective nodes. The +V and GND traces between the capacitors and the EP53F8QI should be as close to each other as possible so that the gap between the two nodes is minimized, even under the capacitors.

Recommendation 2: Input and output grounds are separated until they connect at the PGND pins. The separation shown on Figure 7 between the input and output GND circuits helps minimize noise coupling between the converter input and output switching loops.

Recommendation 3: The system ground plane should be the first layer immediately below the surface layer. This ground plane should be continuous and un-interrupted below the converter and the input/output capacitors. Please see the Gerber files on the Intel website www.Intel.com/enpirion.

Recommendation 4: Multiple small vias should be used to connect the ground traces under the device to the system ground plane on another layer for heat dissipation. The drill diameter of the vias should be 0.33mm, and the vias must have at least 1 oz. copper plating on the inside wall, making the finished hole size around 0.20-0.26mm. Do not use thermal reliefs or spokes to connect the vias to the ground plane. It is preferred to put these vias under the capacitors along the edge of the GND copper closest to the +V copper. Please see Figure 7. These vias connect the input/output filter capacitors to the GND plane and help reduce parasitic inductances in the input and output current loops. If the vias cannot be placed under C_{IN} and C_{OUT}, then put them just outside the capacitors along the GND. Do not use thermal reliefs or spokes to connect these vias to the ground plane.

Recommendation 5: AVIN is the power supply for the internal small-signal control circuits. It should be connected to the input voltage at a quiet point. In Figure 7 this connection is made with RAVIN at the input capacitor close to the V_{IN} connection.

RECOMMENDED PCB FOOTPRIN

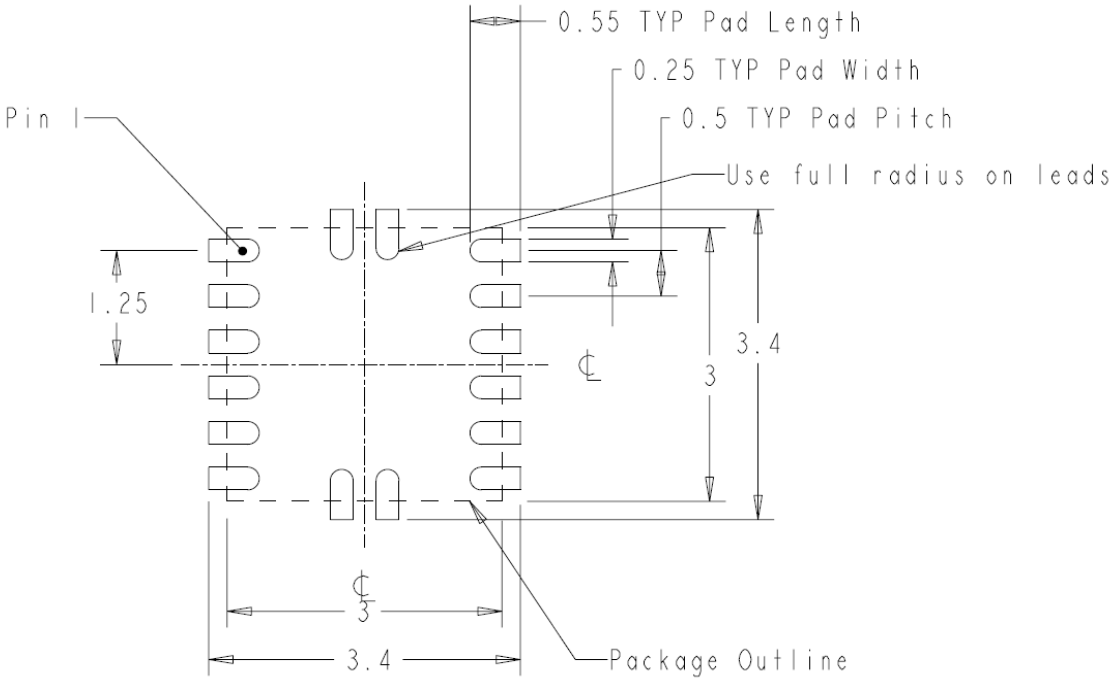


Figure 8. EP53F8QI PCB Footprint (Top View)

PACKAGE DIMENSIONS

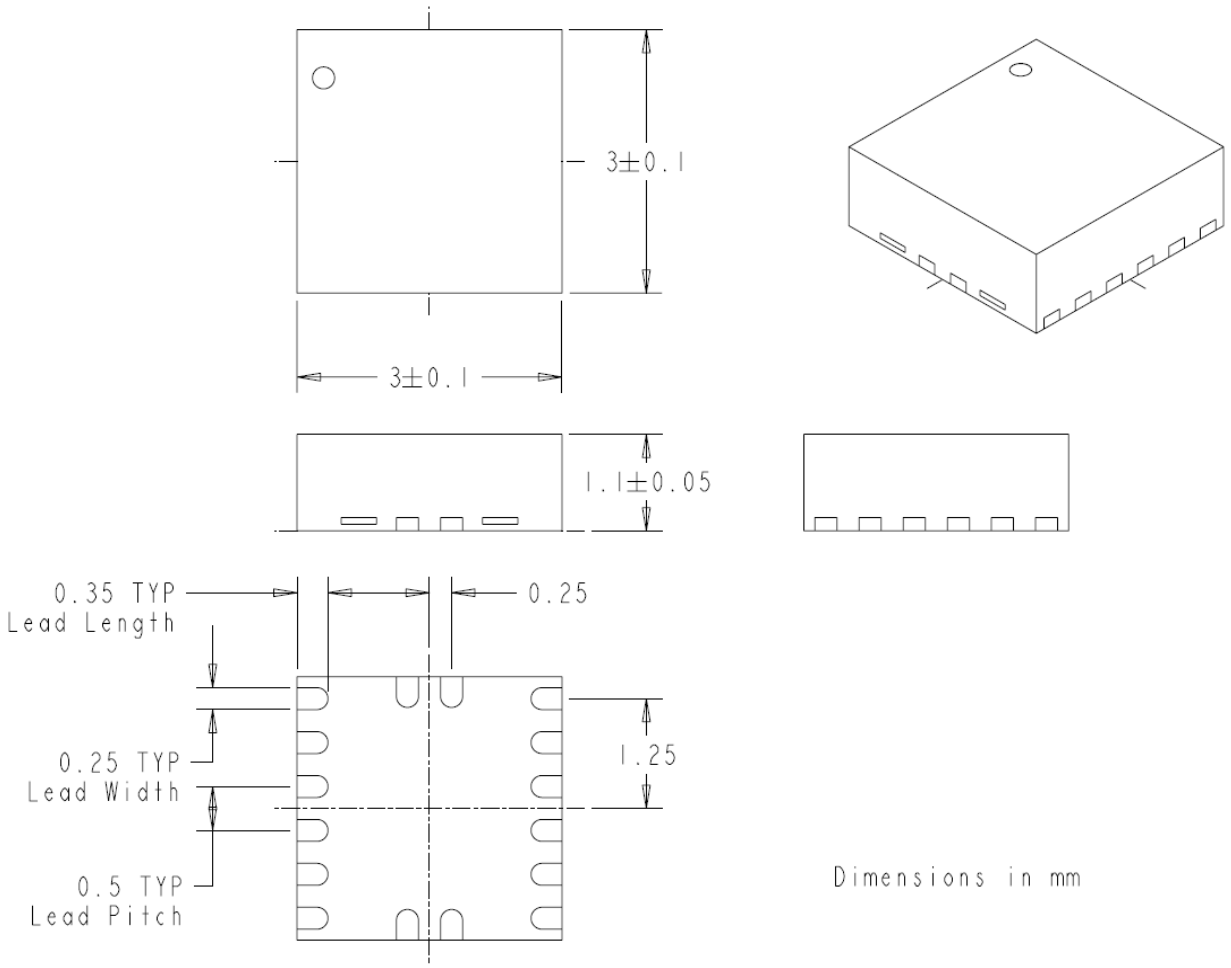


Figure 9. EP53F8QI Package Dimensions

Packing and Marking Information: https://www.intel.com/support/quality-and-reliability/packing.html

REVISION HISTORY

Rev	Date	Change(s)
J	Dec, 2018	• Changed datasheet into Intel format. • Updated COUT_Max equation.
K	April, 2019	• Formatting changes

WHERE TO GET MORE INFORMATION

For more information about Intel® and Enpirion® PowerSoCs, visit:

www.intel.com/enpirion