1 Characteristics

Figure 2. Device configuration

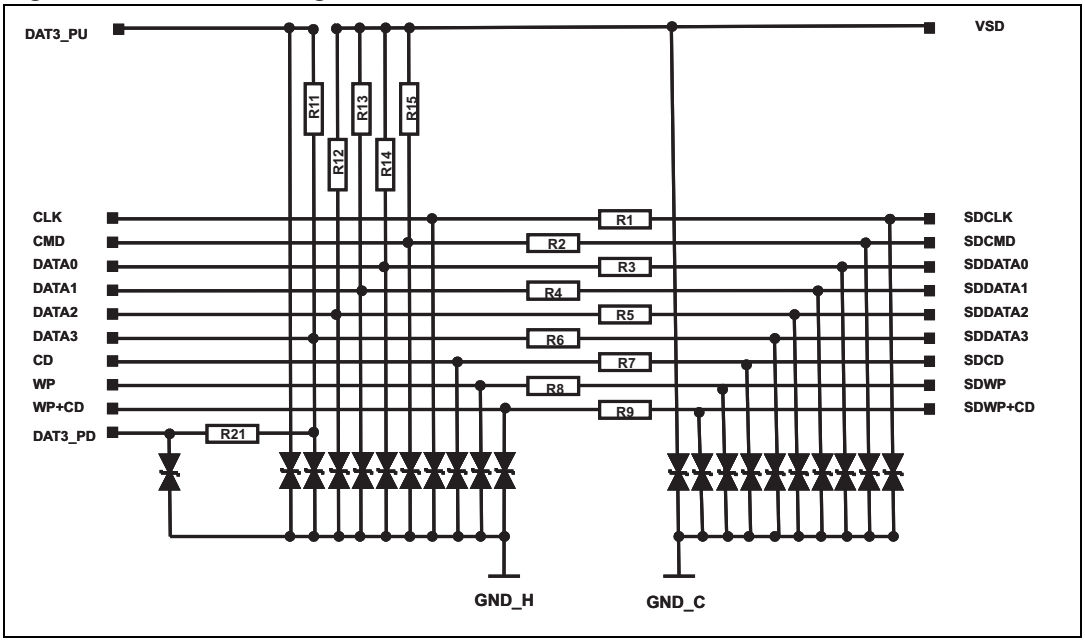


Table 1. Pin-signal attribution

Pin	Description	Pin	Description	Pin	Description	Pin	Description	Pin	Description
A1	DATA2	B1	CD	C1	DAT3_PD	D1	WP+CD	E1	DATA1
A2	DATA3	B2	CMD	C2	WP	D2	CLK	E2	DATA0
A3	GND_H	B3		C3	DAT3_PU	D3	GND_C	E3	GND_C
A4	SDDATA2	B4	SDCD	C4	SDWP	D4	SDWP+CD	E4	SDDATA1
A5	SDDATA3	B5	SDCMD	C5	VSD	D5	SDCLK	E5	SDDATA0

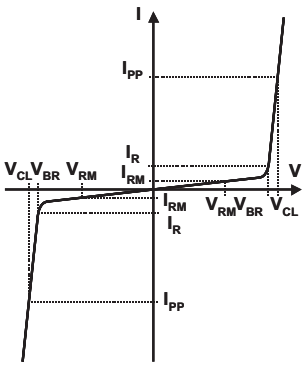
Table 2. Absolute ratings (limiting values)

Symbol	Parameter	Value	Unit
V_{PP}	**Internal pins (A1, B1, C1, D1, E1, A2, B2, C2, D2, E2, C3)** ESD discharge IEC 61000-4-2, air discharge ESD discharge IEC 61000-4-2, contact discharge **External pins (A4, B4, C4, D4, E4, A5, B5, C5, D5, E5)** ESD discharge IEC 61000-4-2, air discharge ESD discharge IEC 61000-4-2, contact discharge	 2 2 15 8	kV
T_j	Junction temperature	125	°C
T_{op}	Operating temperature range	-30 to + 85	°C
T_{stg}	Storage temperature range	-55 to 150	°C

GND bumps (GND_H and GND_C - A3, D3 and E3) must be connected to ground on the printed circuit board for ESD testing and RF measurements.

Table 3. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameters
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between input and output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min	Typ	Max	Unit
V_{BR}	I_R = 1 mA	6		20	V
I_{RM}	V_{RM} = 5 V per line		50	200	nA
R1, R2, R3, R4, R5, R6, R7, R8, R9	Tolerance ± 20%		40		Ω
R11, R12, R13, R14	Tolerance ± 30%		50		kΩ
R15	Tolerance ± 30%		15		kΩ
R21	Tolerance ± 30%		470		kΩ
C_{line}	V_{line} = 0 V, V_{OSC} = 30 mV, F = 1 MHz (under zero light conditions)			20	pF

Figure 3. S21(dB) all lines attenuation measurement

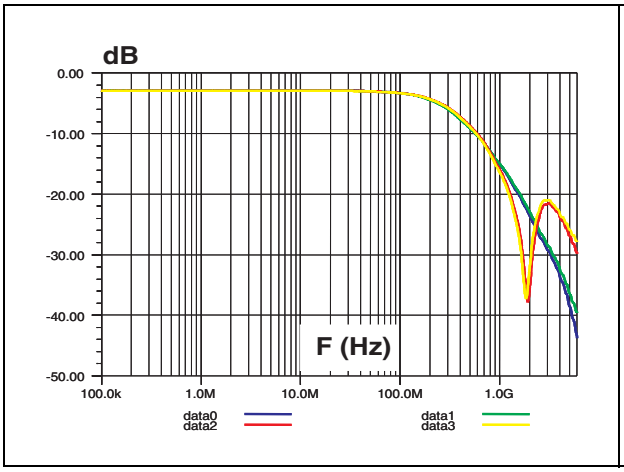


Figure 4. Analog cross talk measurement

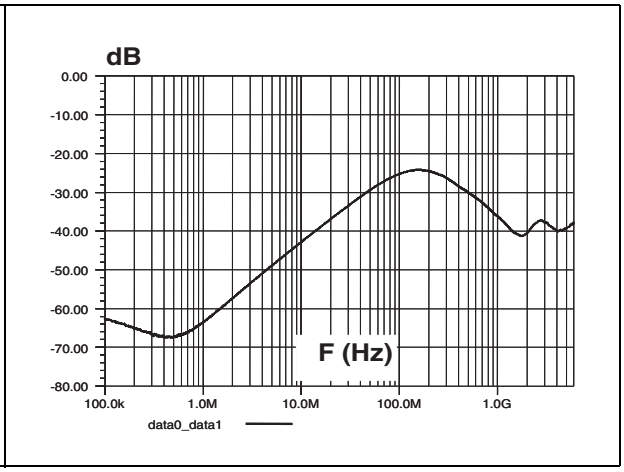


Figure 5. Digital crosstalk measurement

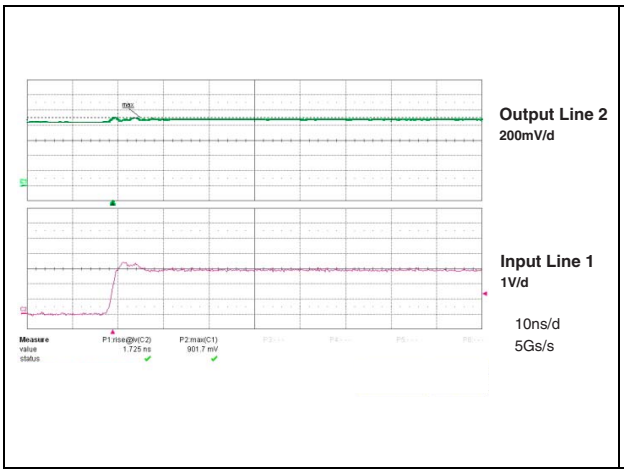


Figure 6. ESD response to IEC 61000-4-2 (+15 kV air discharge) on one input (V_{IN}) and on one output (V_{OUT})

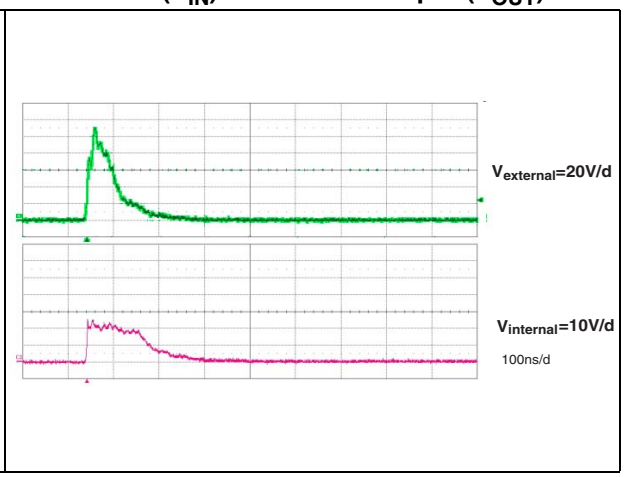


Figure 7. ESD response to IEC 61000-4-2 (-15 kV air discharge) on one input (V_{IN}) and on one output (V_{OUT})

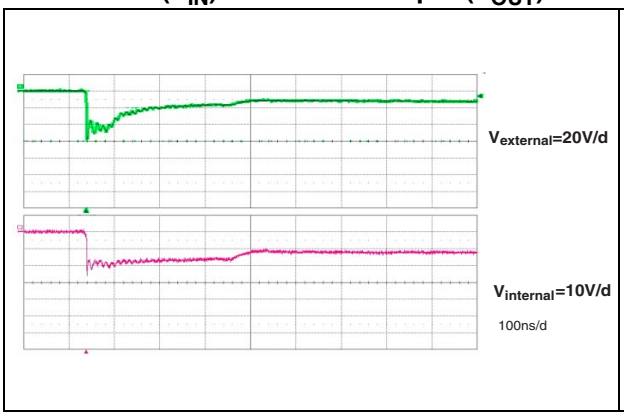
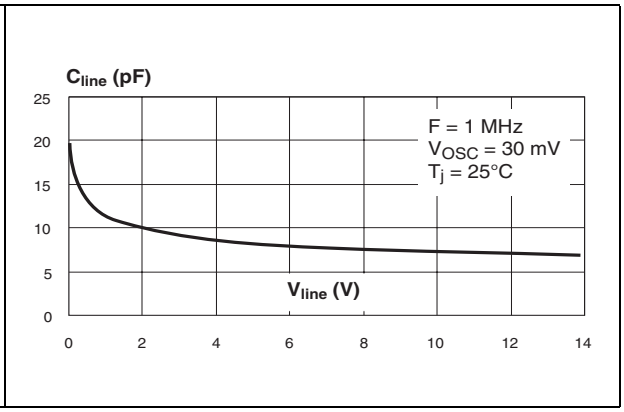


Figure 8. Line capacitance versus applied voltage



2 Application information

Figure 9. Aplac model

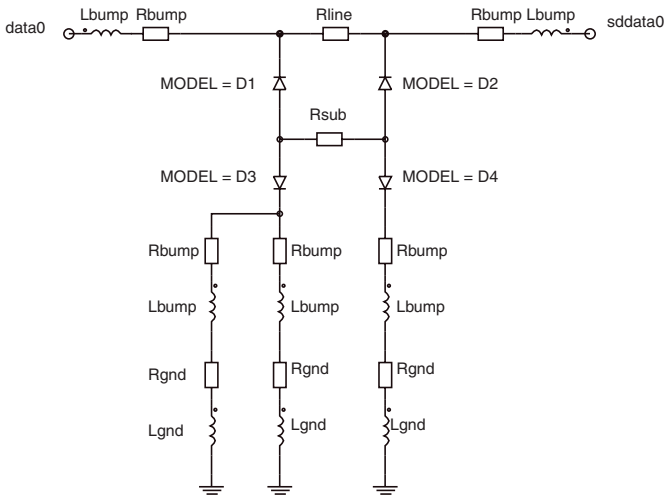
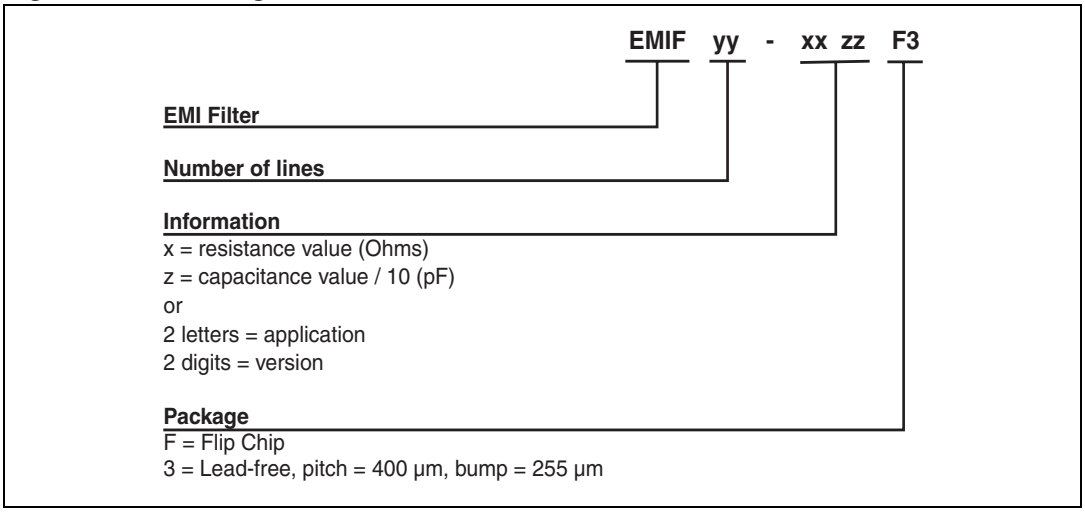


Figure 10. Aplac model variables

Variables	Diode D1	Diode D2	Diode D3	Diode D4
aplacvar Rline 40	BV=7	BV=7	BV=7	BV=7
aplacvar C_d1 14.5p	IBV=1m	IBV=1m	IBV=1m	IBV=1m
aplacvar C_d2 6.5p	CJO=C_d1	CJO=C_d2	CJO=C_d3	CJO=C_d4
aplacvar C_d3 303p	M=0.28	M=0.28	M=0.28	M=0.28
aplacvar C_d4 14.5p	RS=1.13	RS=0.8	RS=0.37	RS=1.13
aplacvar Lbump 43pH	VJ=0.6	VJ=0.6	VJ=0.6	VJ=0.6
aplacvar Rbump 17m	TT=100n	TT=100n	TT=100n	TT=100n
aplacvar Cbump 150f				
aplacvar Lgnd 150pH				
aplacvar Rgnd 10m				
aplacvar Rsub 5				

3 Ordering information scheme

Figure 11. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Figure 12. Package dimensions

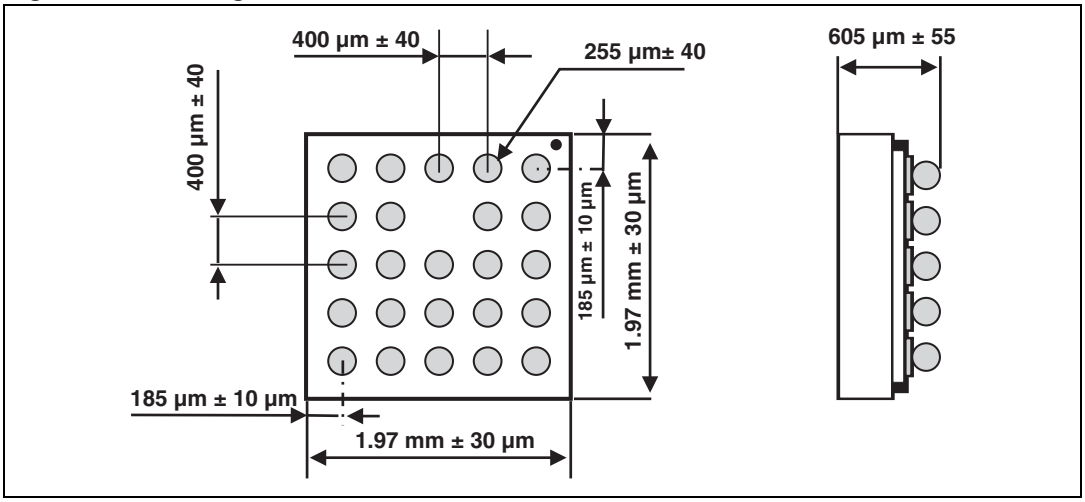


Figure 13. Footprint

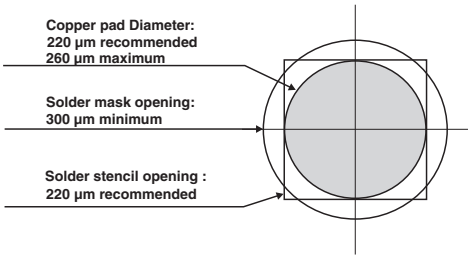


Figure 14. Marking

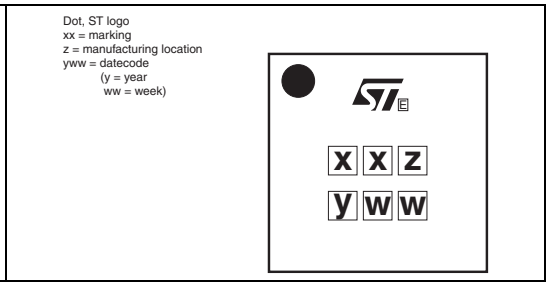
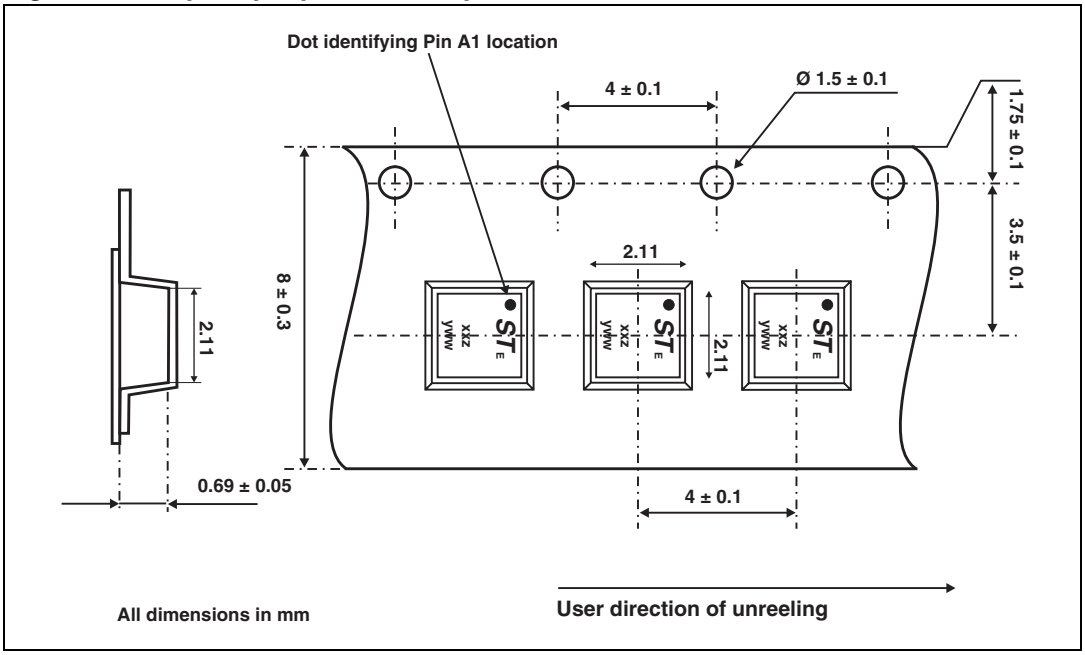


Figure 15. Flip Chip tape and reel specifications



Note: More information is available in the application note:

AN2348: "STMicroelectronics 400 micro-metre Flip Chip: Package description and recommendation for use"

AN1751: EMI Filters: Recommendations and measurements

5 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF09-SD01F3	GZ	Flip Chip	5.2 mg	5000	Tape and reel (7")

6 Revision history

Table 5. Document revision history

Date	Revision	Changes
19-Oct-2005	1	Initial release.
09-Feb-2006	2	Tape cavity dimensions added in Figure 13. Other graphics improved.
22-Mar-2006	3	Reformatted to current standard. Typical and maximum values updated for I_{RM} in Electrical characteristics, page 3.
28-Apr-2008	4	Updated ECOPACK statement. Updated *Figure 11*, *Figure 12* and *Figure 15.* Reformatted to current standards.

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