

1. Feature List

The EFM8BB1 highlighted features are listed below.

- Core:
 - Pipelined CIP-51 Core
 - Fully compatible with standard 8051 instruction set
 - 70% of instructions execute in 1-2 clock cycles
 - 25 MHz maximum operating frequency
- Memory:
 - Up to 8 kB flash memory, in-system re-programmable from firmware.
 - Up to 512 bytes RAM (including 256 bytes standard 8051 RAM and 256 bytes on-chip XRAM)
- Power:
 - Internal LDO regulator for CPU core voltage
 - Power-on reset circuit and brownout detectors
- I/O: Up to 18 total multifunction I/O pins:
 - All pins 5 V tolerant under bias
 - Flexible peripheral crossbar for peripheral routing
 - 5 mA source, 12.5 mA sink allows direct drive of LEDs
- Clock Sources:
 - Internal 24.5 MHz oscillator with $\pm 2\%$ accuracy
 - Internal 80 kHz low-frequency oscillator
 - External CMOS clock option
- Timers/Counters and PWM:
 - 3-channel programmable counter array (PCA) supporting PWM, capture/compare, and frequency output modes
 - 4 x 16-bit general-purpose timers
 - Independent watchdog timer, clocked from the low frequency oscillator
- Communications and Digital Peripherals:
 - UART
 - SPI™ Master / Slave
 - SMBus™/I2C™ Master / Slave
 - 16-bit CRC unit, supporting automatic CRC of flash at 256-byte boundaries
- Analog:
 - 12-Bit Analog-to-Digital Converter (ADC)
 - 2 x Low-current analog comparators with adjustable reference
- On-Chip, Non-Intrusive Debugging
 - Full memory and register inspection
 - Four hardware breakpoints, single-stepping
- Pre-loaded UART bootloader
- Temperature range -40 to 85 °C or -40 to 125 °C
- Single power supply 2.2 to 3.6 V
- QSOP24, SOIC16, and QFN20 packages

With on-chip power-on reset, voltage supply monitor, watchdog timer, and clock oscillator, the EFM8BB1 devices are truly standalone system-on-a-chip solutions. The flash memory is reprogrammable in-circuit, providing non-volatile data storage and allowing field upgrades of the firmware. The on-chip debugging interface (C2) allows non-intrusive (uses no on-chip resources), full speed, in-circuit debugging using the production MCU installed in the final application. This debug logic supports inspection and modification of memory and registers, setting breakpoints, single stepping, and run and halt commands. All analog and digital peripherals are fully functional while debugging. Each device is specified for 2.2 to 3.6 V operation and is AEC-Q100 qualified. Both the G-grade and I-grade devices are available in 20-pin QFN, 16-pin SOIC or 24-pin QSOP packages, and A-grade devices are available in the 20-pin QFN package. All package options are lead-free and RoHS compliant.

2. Ordering Information

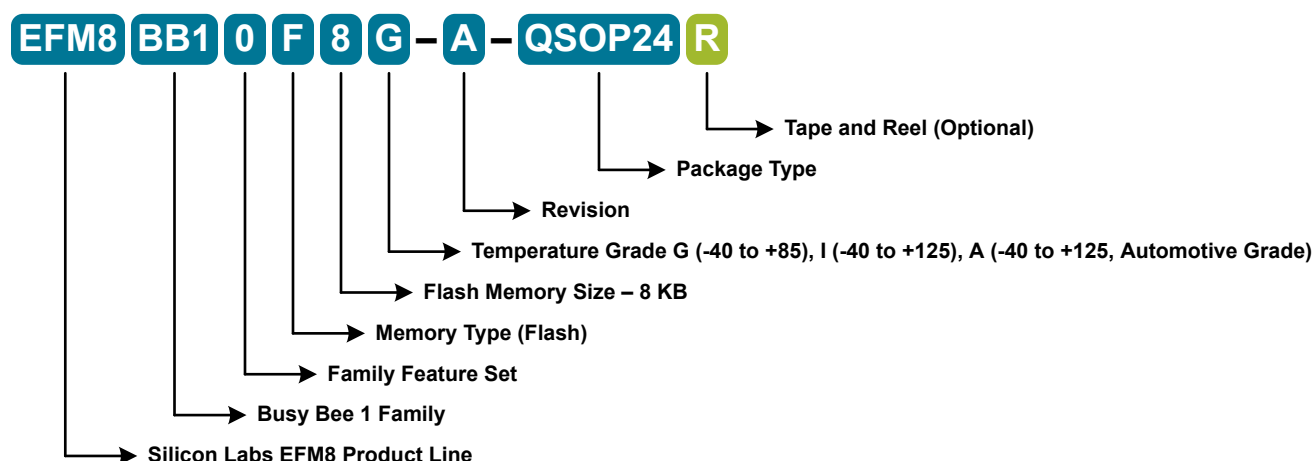


Figure 2.1. EFM8BB1 Part Numbering

All EFM8BB1 family members have the following features:

- CIP-51 Core running up to 25 MHz
- Two Internal Oscillators (24.5 MHz and 80 kHz)
- SMBus / I2C
- SPI
- UART
- 3-Channel Programmable Counter Array (PWM, Clock Generation, Capture/Compare)
- 4 16-bit Timers
- 2 Analog Comparators
- 12-bit Analog-to-Digital Converter with integrated multiplexer, voltage reference, and temperature sensor
- 16-bit CRC Unit
- AEC-Q100 qualified
- Pre-loaded UART bootloader

In addition to these features, each part number in the EFM8BB1 family has a set of features that vary across the product line. The product selection guide shows the features available on each family member.

Table 2.1. Product Selection Guide

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB10F8G-A-QSOP24	8	512	18	16	8	8	Yes	-40 to +85 C	QSOP24
EFM8BB10F8G-A-QFN20	8	512	16	15	8	7	Yes	-40 to +85 C	QFN20
EFM8BB10F8G-A-SOIC16	8	512	13	12	6	6	Yes	-40 to +85 C	SOIC16
EFM8BB10F4G-A-QFN20	4	512	16	15	8	7	Yes	-40 to +85 C	QFN20
EFM8BB10F2G-A-QFN20	2	256	16	15	8	7	Yes	-40 to +85 C	QFN20

Ordering Part Number	Flash Memory (kB)	RAM (Bytes)	Digital Port I/Os (Total)	ADC0 Channels	Comparator 0 Inputs	Comparator 1 Inputs	Pb-free (RoHS Compliant)	Temperature Range	Package
EFM8BB10F8I-A-QSOP24	8	512	18	16	8	8	Yes	-40 to +125 C	QSOP24
EFM8BB10F8I-A-QFN20	8	512	16	15	8	7	Yes	-40 to +125 C	QFN20
EFM8BB10F8I-A-SOIC16	8	512	13	12	6	6	Yes	-40 to +125 C	SOIC16
EFM8BB10F4I-A-QFN20	4	512	16	15	8	7	Yes	-40 to +125 C	QFN20
EFM8BB10F2I-A-QFN20	2	256	16	15	8	7	Yes	-40 to +125 C	QFN20
EFM8BB10F8A-A-QFN20	8	512	16	15	8	7	Yes	-40 to +125 C	QFN20
EFM8BB10F4A-A-QFN20	4	512	16	15	8	7	Yes	-40 to +125 C	QFN20
EFM8BB10F2A-A-QFN20	2	256	16	15	8	7	Yes	-40 to +125 C	QFN20

The A-grade (i.e. EFM8BB10F8A-A-QFN20) devices receive full automotive quality production status, including AEC-Q100 qualification, registration with International Material Data System (IMDS), and Part Production Approval Process (PPAP) documentation. PPAP documentation is available at www.silabs.com with a registered and NDA approved user account.

Table of Contents

1. Feature List	2
2. Ordering Information	3
3. System Overview	7
3.1 Introduction	7
3.2 Power	8
3.3 I/O	8
3.4 Clocking	8
3.5 Counters/Timers and PWM	9
3.6 Communications and Other Digital Peripherals	10
3.7 Analog	11
3.8 Reset Sources	12
3.9 Debugging	12
3.10 Bootloader	13
4. Electrical Specifications	15
4.1 Electrical Characteristics	15
4.1.1 Recommended Operating Conditions	15
4.1.2 Power Consumption	16
4.1.3 Reset and Supply Monitor	18
4.1.4 Flash Memory	19
4.1.5 Internal Oscillators	19
4.1.6 External Clock Input	20
4.1.7 ADC	21
4.1.8 Voltage Reference	22
4.1.9 Temperature Sensor	23
4.1.10 1.8 V Internal LDO Voltage Regulator	23
4.1.11 Comparators	24
4.1.12 Port I/O	26
4.1.13 SMBus	27
4.2 Thermal Conditions	29
4.3 Absolute Maximum Ratings	29
4.4 Typical Performance Curves	30
5. Typical Connection Diagrams	34
5.1 Power	34
5.2 Debug	34
5.3 Other Connections	35
6. Pin Definitions	36
6.1 EFM8BB1x-QSOP24 Pin Definitions	36
6.2 EFM8BB1x-QFN20 Pin Definitions	39

6.3 EFM8BB1x-SOIC16 Pin Definitions	.42
7. QSOP24 Package Specifications	44
7.1 QSOP24 Package Dimensions	.44
7.2 QSOP24 PCB Land Pattern	.46
7.3 QSOP24 Package Marking	.47
8. QFN20 Package Specifications.	48
8.1 QFN20 Package Dimensions	.48
8.2 QFN20 PCB Land Pattern	.50
8.3 QFN20 Package Marking	.51
9. SOIC16 Package Specifications	52
9.1 SOIC16 Package Dimensions	.52
9.2 SOIC16 PCB Land Pattern	.54
9.3 SOIC16 Package Marking	.55
10. Revision History.	56
10.1 Revision 1.6	.56
10.2 Revision 1.5	.56
10.3 Revision 1.4	.56
10.4 Revision 1.3	.56
10.5 Revision 1.2	.56
10.6 Revision 1.1	.56

3. System Overview

3.1 Introduction

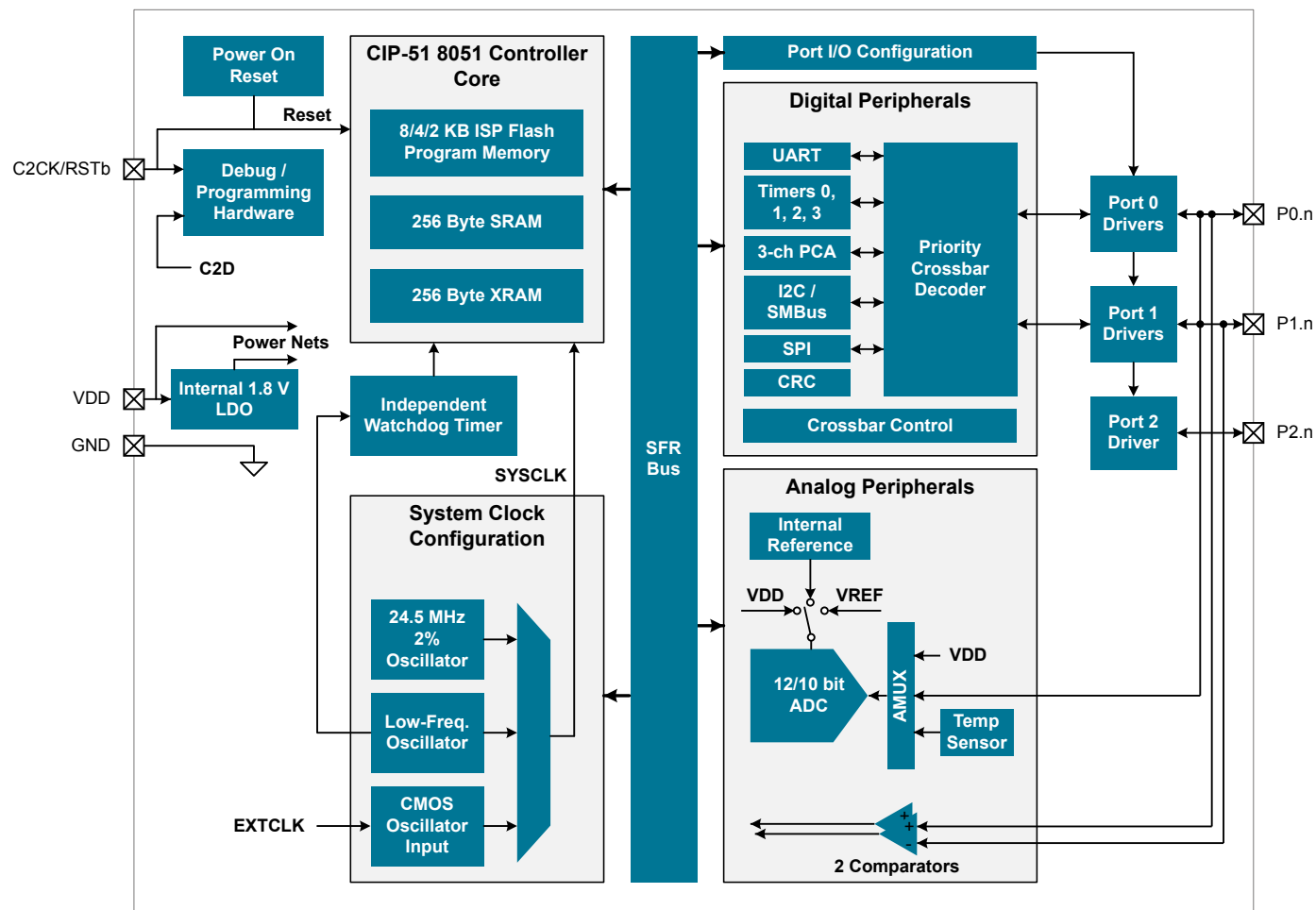


Figure 3.1. Detailed EFM8BB1 Block Diagram

This section describes the EFM8BB1 family at a high level. For more information on each module including register definitions, see the EFM8BB1 Reference Manual.

3.2 Power

All internal circuitry draws power from the VDD supply pin. External I/O pins are powered from the VIO supply voltage (or VDD on devices without a separate VIO connection), while most of the internal circuitry is supplied by an on-chip LDO regulator. Control over the device power can be achieved by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and placed in low power mode. Digital peripherals, such as timers and serial buses, have their clocks gated off and draw little power when they are not in use.

Table 3.1. Power Modes

Power Mode	Details	Mode Entry	Wake-Up Sources
Normal	Core and all peripherals clocked and fully operational	—	—
Idle	- Core halted - All peripherals clocked and fully operational - Code resumes execution on wake event	Set IDLE bit in PCON0	Any interrupt
Stop	- All internal power nets shut down - Pins retain state - Exit on any reset source	1. Clear STOPCF bit in REG0CN 2. Set STOP bit in PCON0	Any reset source
Shutdown	- All internal power nets shut down - Pins retain state - Exit on pin or power-on reset	1. Set STOPCF bit in REG0CN 2. Set STOP bit in PCON0	- RSTb pin reset - Power-on reset

3.3 I/O

Digital and analog resources are externally available on the device's multi-purpose I/O pins. Port pins P0.0-P1.7 can be defined as general-purpose I/O (GPIO), assigned to one of the internal digital resources through the crossbar or dedicated channels, or assigned to an analog function. Port pins P2.0 and P2.1 can be used as GPIO. Additionally, the C2 Interface Data signal (C2D) is shared with P2.0.

- Up to 18 multi-functions I/O pins, supporting digital and analog functions.
- Flexible priority crossbar decoder for digital peripheral assignment.
- Two drive strength settings for each port.
- Two direct-pin interrupt sources with dedicated interrupt vectors (INT0 and INT1).
- Up to 16 direct-pin interrupt sources with shared interrupt vector (Port Match).

3.4 Clocking

The CPU core and peripheral subsystem may be clocked by both internal and external oscillator resources. By default, the system clock comes up running from the 24.5 MHz oscillator divided by 8.

- Provides clock to core and peripherals.
- 24.5 MHz internal oscillator (HFOSC0), accurate to $\pm 2\%$ over supply and temperature corners.
- 80 kHz low-frequency oscillator (LFOSC0).
- External CMOS clock input (EXTCLK).
- Clock divider with eight settings for flexible clock scaling: Divide the selected clock source by 1, 2, 4, 8, 16, 32, 64, or 128.

3.5 Counters/Timers and PWM

Programmable Counter Array (PCA0)

The programmable counter array (PCA) provides multiple channels of enhanced timer and PWM functionality while requiring less CPU intervention than standard counter/timers. The PCA consists of a dedicated 16-bit counter/timer and one 16-bit capture/compare module for each channel. The counter/timer is driven by a programmable timebase that has flexible external and internal clocking options. Each capture/compare module may be configured to operate independently in one of five modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, or Pulse-Width Modulated (PWM) Output. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the crossbar to port I/O when enabled.

- 16-bit time base
- Programmable clock divisor and clock source selection
- Up to three independently-configurable channels
- 8, 9, 10, 11 and 16-bit PWM modes (center or edge-aligned operation)
- Output polarity control
- Frequency output mode
- Capture on rising, falling or any edge
- Compare function for arbitrary waveform generation
- Software timer (internal compare) mode
- Can accept hardware “kill” signal from comparator 0

Timers (Timer 0, Timer 1, Timer 2, and Timer 3)

Several counter/timers are included in the device: two are 16-bit counter/timers compatible with those found in the standard 8051, and the rest are 16-bit auto-reload timers for timing peripherals or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. The other timers offer both 16-bit and split 8-bit timer functionality with auto-reload and capture capabilities.

Timer 0 and Timer 1 include the following features:

- Standard 8051 timers, supporting backwards-compatibility with firmware and hardware.
- Clock sources include SYSCLK, SYSCLK divided by 12, 4, or 48, the External Clock divided by 8, or an external pin.
- 8-bit auto-reload counter/timer mode
- 13-bit counter/timer mode
- 16-bit counter/timer mode
- Dual 8-bit counter/timer mode (Timer 0)

Timer 2 and Timer 3 are 16-bit timers including the following features:

- Clock sources include SYSCLK, SYSCLK divided by 12, or the External Clock divided by 8.
- 16-bit auto-reload timer mode
- Dual 8-bit auto-reload timer mode
- External pin capture (Timer 2)
- LFOSC0 capture (Timer 3)

Watchdog Timer (WDT0)

The device includes a programmable watchdog timer (WDT) running off the low-frequency oscillator. A WDT overflow forces the MCU into the reset state. To prevent the reset, the WDT must be restarted by application software before overflow. If the system experiences a software or hardware malfunction preventing the software from restarting the WDT, the WDT overflows and causes a reset. Following a reset, the WDT is automatically enabled and running with the default maximum time interval. If needed, the WDT can be disabled by system software or locked on to prevent accidental disabling. Once locked, the WDT cannot be disabled until the next system reset. The state of the RST pin is unaffected by this reset.

The Watchdog Timer has the following features:

- Programmable timeout interval
- Runs from the low-frequency oscillator
- Lock-out feature to prevent any modification until a system reset

3.6 Communications and Other Digital Peripherals

Universal Asynchronous Receiver/Transmitter (UART0)

UART0 is an asynchronous, full duplex serial port offering modes 1 and 3 of the standard 8051 UART. Enhanced baud rate support allows a wide range of clock sources to generate standard baud rates. Received data buffering allows UART0 to start reception of a second incoming data byte before software has finished reading the previous data byte.

The UART module provides the following features:

- Asynchronous transmissions and receptions.
- Baud rates up to $\text{SYSCLK}/2$ (transmit) or $\text{SYSCLK}/8$ (receive).
- 8- or 9-bit data.
- Automatic start and stop generation.
- Single-byte FIFO on transmit and receive.

Serial Peripheral Interface (SPI0)

The serial peripheral interface (SPI) module provides access to a flexible, full-duplex synchronous serial bus. The SPI can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select the SPI in slave mode, or to disable master mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a firmware-controlled chip-select output in master mode, or disabled to reduce the number of pins required. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

The SPI module includes the following features:

- Supports 3- or 4-wire operation in master or slave modes.
- Supports external clock frequencies up to $\text{SYSCLK} / 2$ in master mode and $\text{SYSCLK} / 10$ in slave mode.
- Support for four clock phase and polarity options.
- 8-bit dedicated clock rate generator.
- Support for multiple masters on the same data lines.

System Management Bus / I2C (SMB0)

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I²C serial bus.

The SMBus module includes the following features:

- Standard (up to 100 kbps) and Fast (400 kbps) transfer speeds.
- Support for master, slave, and multi-master modes.
- Hardware synchronization and arbitration for multi-master mode.
- Clock low extending (clock stretching) to interface with faster masters.
- Hardware support for 7-bit slave and general call address recognition.
- Firmware support for 10-bit slave address decoding.
- Ability to inhibit all slave states.
- Programmable data setup/hold times.

16-bit CRC (CRC0)

The cyclic redundancy check (CRC) module performs a CRC using a 16-bit polynomial. CRC0 accepts a stream of 8-bit data and posts the 16-bit result to an internal register. In addition to using the CRC block for data manipulation, hardware can automatically CRC the flash contents of the device.

The CRC module is designed to provide hardware calculations for flash memory verification and communications protocols. The CRC module supports the standard CCITT-16 16-bit polynomial (0x1021), and includes the following features:

- Support for CCITT-16 polynomial
- Byte-level bit reversal
- Automatic CRC of flash contents on one or more 256-byte blocks
- Initial seed selection of 0x0000 or 0xFFFF

3.7 Analog

12-Bit Analog-to-Digital Converter (ADC0)

The ADC is a successive-approximation-register (SAR) ADC with 12-, 10-, and 8-bit modes, integrated track-and hold and a programmable window detector. The ADC is fully configurable under software control via several registers. The ADC may be configured to measure different signals using the analog multiplexer. The voltage reference for the ADC is selectable between internal and external reference sources.

- Up to 16 external inputs.
- Single-ended 12-bit and 10-bit modes.
- Supports an output update rate of 200 ksps samples per second in 12-bit mode or 800 ksps samples per second in 10-bit mode.
- Operation in low power modes at lower conversion speeds.
- Asynchronous hardware conversion trigger, selectable between software, external I/O and internal timer sources.
- Output data window comparator allows automatic range checking.
- Support for burst mode, which produces one set of accumulated data per conversion-start trigger with programmable power-on settling and tracking time.
- Conversion complete and window compare interrupts supported.
- Flexible output data formatting.
- Includes an internal fast-settling reference with two levels (1.65 V and 2.4 V) and support for external reference and signal ground.
- Integrated temperature sensor.

Low Current Comparators (CMP0, CMP1)

Analog comparators are used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. External input connections to device I/O pins and internal connections are available through separate multiplexers on the positive and negative inputs. Hysteresis, response time, and current consumption may be programmed to suit the specific needs of the application.

The comparator module includes the following features:

- Up to 8 external positive inputs.
- Up to 8 external negative inputs.
- Additional input options:
 - Internal connection to LDO output.
 - Direct connection to GND.
- Synchronous and asynchronous outputs can be routed to pins via crossbar.
- Programmable hysteresis between 0 and ± 20 mV
- Programmable response time.
- Interrupts generated on rising, falling, or both edges.

3.8 Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- The core halts program execution.
- Module registers are initialized to their defined reset values unless the bits reset only with a power-on reset.
- External port pins are forced to a known state.
- Interrupts and timers are disabled.

All registers are reset to the predefined values noted in the register descriptions unless the bits only reset with a power-on reset. The contents of RAM are unaffected during a reset; any previously stored data is preserved as long as power is not lost. The Port I/O latches are reset to 1 in open-drain mode. Weak pullups are enabled during and after the reset. For Supply Monitor and power-on resets, the RSTb pin is driven low until the device exits the reset state. On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to an internal oscillator. The Watchdog Timer is enabled, and program execution begins at location 0x0000.

Reset sources on the device include the following:

- Power-on reset
- External reset pin
- Comparator reset
- Software-triggered reset
- Supply monitor reset (monitors VDD supply)
- Watchdog timer reset
- Missing clock detector reset
- Flash error reset

3.9 Debugging

The EFM8BB1 devices include an on-chip Silicon Labs 2-Wire (C2) debug interface to allow flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

3.10 Bootloader

All devices come pre-programmed with a UART bootloader. This bootloader resides in the code security page, which is the last last page of code flash; it can be erased if it is not needed.

The byte before the Lock Byte is the Bootloader Signature Byte. Setting this byte to a value of 0xA5 indicates the presence of the bootloader in the system. Any other value in this location indicates that the bootloader is not present in flash.

When a bootloader is present, the device will jump to the bootloader vector after any reset, allowing the bootloader to run. The bootloader then determines if the device should stay in bootload mode or jump to the reset vector located at 0x0000. When the bootloader is not present, the device will jump to the reset vector of 0x0000 after any reset.

More information about the bootloader protocol and usage can be found in *AN945: EFM8 Factory Bootloader User Guide*. Application notes can be found on the Silicon Labs website (www.silabs.com/8bit-appnotes) or within Simplicity Studio by using the [Application Notes] tile.

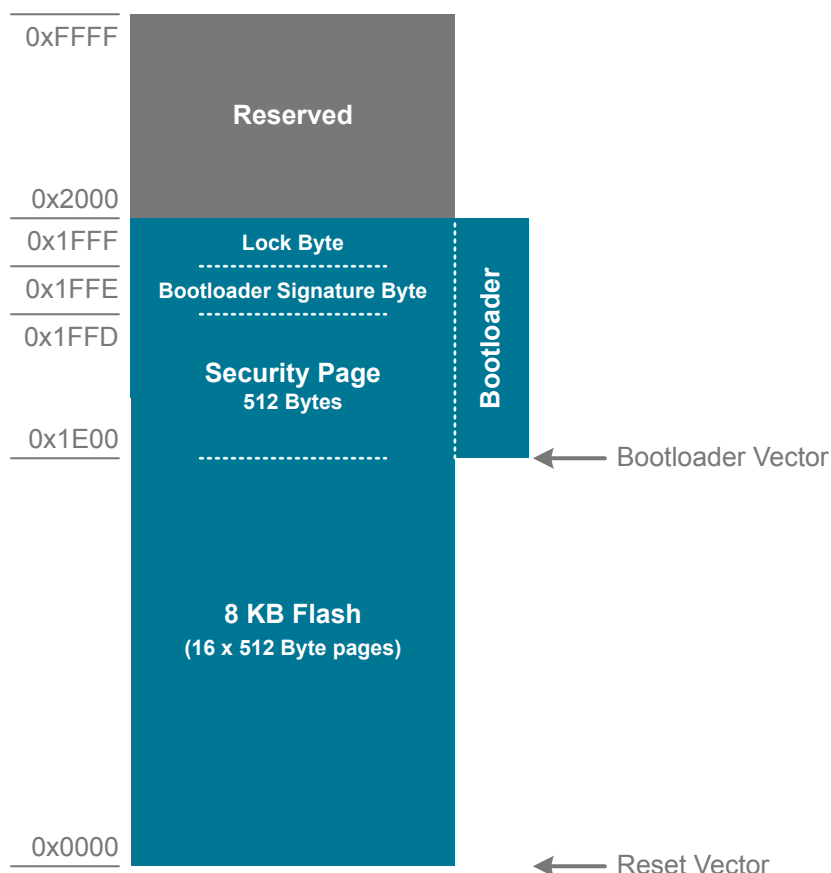


Figure 3.2. Flash Memory Map with Bootloader—8 KB Devices

Table 3.2. Summary of Pins for Bootloader Communication

Bootloader	Pins for Bootload Communication
UART	TX – P0.4
	RX – P0.5

Table 3.3. Summary of Pins for Bootload Mode Entry

Device Package	Pin for Bootload Mode Entry
QSOP24	P2.0 / C2D
QFN20	P2.0 / C2D
SOIC16	P2.0 / C2D

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the conditions listed in [Table 4.1 Recommended Operating Conditions on page 15](#), unless stated otherwise.

4.1.1 Recommended Operating Conditions

Table 4.1. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating Supply Voltage on VDD	V _{DD}		2.2	—	3.6	V
System Clock Frequency	f _{SYSCLK}		0	—	25	MHz
Operating Ambient Temperature	T _A	G-grade devices	−40	—	85	°C
		I-grade or A-grade devices	−40	—	125	°C

Note:

1. All voltages with respect to GND
2. GPIO levels are undefined whenever VDD is less than 1 V.

4.1.2 Power Consumption

Table 4.2. Power Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Core Supply Current (G-grade devices, -40 °C to +85 °C)						
Normal Mode—Full speed with code executing from flash	I_{DD}	$F_{SYSCLK} = 24.5 \text{ MHz}^2$	—	4.45	4.85	mA
		$F_{SYSCLK} = 1.53 \text{ MHz}^2$	—	915	1150	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$, $T_A = 25 \text{ °C}$	—	250	290	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$	—	250	380	μA
Idle Mode—Core halted with peripherals running	I_{DD}	$F_{SYSCLK} = 24.5 \text{ MHz}^2$	—	2.05	2.3	mA
		$F_{SYSCLK} = 1.53 \text{ MHz}^2$	—	550	700	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$, $T_A = 25 \text{ °C}$	—	125	130	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$	—	125	200	μA
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I_{DD}	$T_A = 25 \text{ °C}$	—	105	120	μA
		$T_A = -40 \text{ to } +85 \text{ °C}$	—	105	170	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I_{DD}		—	0.2	—	μA
Digital Core Supply Current (I-grade or A-grade devices, -40 °C to +125 °C)						
Normal Mode—Full speed with code executing from flash	I_{DD}	$F_{SYSCLK} = 24.5 \text{ MHz}^2$	—	4.45	5.25	mA
		$F_{SYSCLK} = 1.53 \text{ MHz}^2$	—	915	1600	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$, $T_A = 25 \text{ °C}$	—	250	290	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$	—	250	725	μA
Idle Mode—Core halted with peripherals running	I_{DD}	$F_{SYSCLK} = 24.5 \text{ MHz}^2$	—	2.05	2.6	mA
		$F_{SYSCLK} = 1.53 \text{ MHz}^2$	—	550	1000	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$, $T_A = 25 \text{ °C}$	—	125	130	μA
		$F_{SYSCLK} = 80 \text{ kHz}^3$	—	125	550	μA
Stop Mode—Core halted and all clocks stopped, Internal LDO On, Supply monitor off.	I_{DD}	$T_A = 25 \text{ °C}$	—	105	120	μA
		$T_A = -40 \text{ to } +125 \text{ °C}$	—	105	270	μA
Shutdown Mode—Core halted and all clocks stopped, Internal LDO Off, Supply monitor off.	I_{DD}		—	0.2	—	μA
Analog Peripheral Supply Currents (-40 °C to +125 °C)						
High-Frequency Oscillator	I_{HFOSC}	Operating at 24.5 MHz, $T_A = 25 \text{ °C}$	—	155	—	μA
Low-Frequency Oscillator	I_{LFOSC}	Operating at 80 kHz, $T_A = 25 \text{ °C}$	—	3.5	—	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
ADC0 Always-on ⁴	I_{ADC}	800 ksps, 10-bit conversions or 200 ksps, 12-bit conversions Normal bias settings $V_{DD} = 3.0\text{ V}$	—	845	1200	μA
		250 ksps, 10-bit conversions or 62.5 ksps 12-bit conversions Low power bias settings $V_{DD} = 3.0\text{ V}$	—	425	580	μA
ADC0 Burst Mode, 10-bit single conversions, external reference	I_{ADC}	200 ksps, $V_{DD} = 3.0\text{ V}$	—	370	—	μA
		100 ksps, $V_{DD} = 3.0\text{ V}$	—	185	—	μA
		10 ksps, $V_{DD} = 3.0\text{ V}$	—	19	—	μA
ADC0 Burst Mode, 10-bit single conversions, internal reference, Low power bias settings	I_{ADC}	200 ksps, $V_{DD} = 3.0\text{ V}$	—	490	—	μA
		100 ksps, $V_{DD} = 3.0\text{ V}$	—	245	—	μA
		10 ksps, $V_{DD} = 3.0\text{ V}$	—	23	—	μA
ADC0 Burst Mode, 12-bit single conversions, external reference	I_{ADC}	100 ksps, $V_{DD} = 3.0\text{ V}$	—	530	—	μA
		50 ksps, $V_{DD} = 3.0\text{ V}$	—	265	—	μA
		10 ksps, $V_{DD} = 3.0\text{ V}$	—	53	—	μA
ADC0 Burst Mode, 12-bit single conversions, internal reference	I_{ADC}	100 ksps, $V_{DD} = 3.0\text{ V}$, Normal bias	—	950	—	μA
		50 ksps, $V_{DD} = 3.0\text{ V}$, Low power bias	—	420	—	μA
		10 ksps, $V_{DD} = 3.0\text{ V}$, Low power bias	—	85	—	μA
Internal ADC0 Reference, Always-on ⁵	I_{VREFFS}	Normal Power Mode	—	680	790	μA
		Low Power Mode	—	160	210	μA
Temperature Sensor	I_{TSENSE}		—	75	120	μA
Comparator 0 (CMP0), Comparator 1 (CMP1)	I_{CMP}	CPMD = 11	—	0.5	—	μA
		CPMD = 10	—	3	—	μA
		CPMD = 01	—	10	—	μA
		CPMD = 00	—	25	—	μA
Voltage Supply Monitor (VMON0)	I_{VMON}		—	15	20	μA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. Currents are additive. For example, where I_{DD} is specified and the mode is not mutually exclusive, enabling the functions increases supply current by the specified amount. 2. Includes supply current from internal regulator, supply monitor, and High Frequency Oscillator. 3. Includes supply current from internal regulator, supply monitor, and Low Frequency Oscillator. 4. ADC0 always-on power excludes internal reference supply current. 5. The internal reference is enabled as-needed when operating the ADC in burst mode to save power.						

4.1.3 Reset and Supply Monitor

Table 4.3. Reset and Supply Monitor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
V _{DD} Supply Monitor Threshold	V _{VDDM}		1.85 ¹	1.95	2.1	V
Power-On Reset (POR) Threshold	V _{POR}	Rising Voltage on V _{DD}	—	1.4	—	V
		Falling Voltage on V _{DD}	0.75	—	1.36	V
V _{DD} Ramp Time	t _{RMP}	Time to V _{DD} ≥ 2.2 V	10	—	—	μs
Reset Delay from POR	t _{POR}	Relative to V _{DD} ≥ V _{POR}	3	10	31	ms
Reset Delay from non-POR source	t _{RST}	Time between release of reset source and code execution	—	39	—	μs
RST Low Time to Generate Reset	t _{RSTL}		15	—	—	μs
Missing Clock Detector Response Time (final rising edge to reset)	t _{MCD}	F _{SYSCLK} > 1 MHz	—	0.625	1.2	ms
Missing Clock Detector Trigger Frequency	F _{MCD}		—	7.5	13.5	kHz
V _{DD} Supply Monitor Turn-On Time	t _{MON}		—	2	—	μs
Note: 1. MCU core, digital logic, flash memory, and RAM operation is guaranteed down to the minimum V_{DD} Supply Monitor Threshold.						

4.1.4 Flash Memory

Table 4.4. Flash Memory

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Write Time ^{1,2}	t_{WRITE}	One Byte, $F_{\text{SYSCLK}} = 24.5 \text{ MHz}$	19	20	21	μs
Erase Time ^{1,2}	t_{ERASE}	One Page, $F_{\text{SYSCLK}} = 24.5 \text{ MHz}$	5.2	5.35	5.5	ms
V_{DD} Voltage During Programming ³	V_{PROG}		2.2	—	3.6	V
Endurance (Write/Erase Cycles)	N_{WE}		20k	100k	—	Cycles
CRC Calculation Time	t_{CRC}	One 256-Byte Block $\text{SYSCLK} = 24.5 \text{ MHz}$	—	11	—	μs

Note:

1. Does not include sequencing time before and after the write/erase operation, which may be multiple SYSCLK cycles.
2. The internal High-Frequency Oscillator has a programmable output frequency using the HFO0CAL register, which is factory programmed to 24.5 MHz. If user firmware adjusts the oscillator speed, it must be between 22 and 25 MHz during any flash write or erase operation. It is recommended to write the HFO0CAL register back to its reset value when writing or erasing flash.
3. Flash can be safely programmed at any voltage above the supply monitor threshold (V_{VDDM}).
4. Data Retention Information is published in the Quarterly Quality and Reliability Report.

4.1.5 Internal Oscillators

Table 4.5. Internal Oscillators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Frequency Oscillator 0 (24.5 MHz)						
Oscillator Frequency	f_{HFOSC0}	Full Temperature and Supply Range	24	24.5	25	MHz
Power Supply Sensitivity	$\text{PSS}_{\text{HFOSC0}}$	$T_A = 25^\circ\text{C}$	—	0.5	—	%/V
Temperature Sensitivity	$\text{TS}_{\text{HFOSC0}}$	$V_{\text{DD}} = 3.0 \text{ V}$	—	40	—	ppm/ $^\circ\text{C}$
Low Frequency Oscillator (80 kHz)						
Oscillator Frequency	f_{LFOSC}	Full Temperature and Supply Range	75	80	85	kHz
Power Supply Sensitivity	$\text{PSS}_{\text{LFOSC}}$	$T_A = 25^\circ\text{C}$	—	0.05	—	%/V
Temperature Sensitivity	TS_{LFOSC}	$V_{\text{DD}} = 3.0 \text{ V}$	—	65	—	ppm/ $^\circ\text{C}$

4.1.6 External Clock Input

Table 4.6. External Clock Input

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
External Input CMOS Clock Frequency (at EXTCLK pin)	f_{CMOS}		0	—	25	MHz
External Input CMOS Clock High Time	t_{CMOSH}		18	—	—	ns
External Input CMOS Clock Low Time	t_{CMOSL}		18	—	—	ns

4.1.7 ADC

Table 4.7. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Resolution	N _{bits}	12 Bit Mode	12			Bits
		10 Bit Mode	10			Bits
Throughput Rate (High Speed Mode)	f _S	12 Bit Mode	—	—	200	ksps
		10 Bit Mode	—	—	800	ksps
Throughput Rate (Low Power Mode)	f _S	12 Bit Mode	—	—	62.5	ksps
		10 Bit Mode	—	—	250	ksps
Tracking Time	t _{TRK}	High Speed Mode	230	—	—	ns
		Low Power Mode	450	—	—	ns
Power-On Time	t _{PWR}		1.2	—	—	μs
SAR Clock Frequency	f _{SAR}	High Speed Mode, Reference is 2.4 V internal	—	—	6.25	MHz
		High Speed Mode, Reference is not 2.4 V internal	—	—	12.5	MHz
		Low Power Mode	—	—	4	MHz
Conversion Time	t _{CNV}	10-Bit Conversion, SAR Clock = 12.25 MHz, System Clock = 24.5 MHz.	1.1			μs
Sample/Hold Capacitor	C _{SAR}	Gain = 1	—	5	—	pF
		Gain = 0.5	—	2.5	—	pF
Input Pin Capacitance	C _{IN}		—	20	—	pF
Input Mux Impedance	R _{MUX}		—	550	—	Ω
Voltage Reference Range	V _{REF}		1	—	V _{DD}	V
Input Voltage Range*	V _{IN}	Gain = 1	0	—	V _{REF}	V
		Gain = 0.5	0	—	2xV _{REF}	V
Power Supply Rejection Ratio	PSRR _{ADC}		—	70	—	dB
DC Performance						
Integral Nonlinearity	INL	12 Bit Mode	—	±1	±2.3	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Differential Nonlinearity (Guaranteed Monotonic)	DNL	12 Bit Mode	–1	±0.7	1.9	LSB
		10 Bit Mode	—	±0.2	±0.6	LSB
Offset Error	E _{OFF}	12 Bit Mode, V _{REF} = 1.65 V	–3	0	3	LSB
		10 Bit Mode, V _{REF} = 1.65 V	–2	0	2	LSB
Offset Temperature Coefficient	TC _{OFF}		—	0.004	—	LSB/°C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Slope Error	E _M	12 Bit Mode	—	±0.02	±0.1	%
		10 Bit Mode	—	±0.06	±0.24	%
Dynamic Performance 10 kHz Sine Wave Input 1dB below full scale, Max throughput, using AGND pin						
Signal-to-Noise	SNR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Signal-to-Noise Plus Distortion	SNDR	12 Bit Mode	61	66	—	dB
		10 Bit Mode	53	60	—	dB
Total Harmonic Distortion (Up to 5th Harmonic)	THD	12 Bit Mode	—	71	—	dB
		10 Bit Mode	—	70	—	dB
Spurious-Free Dynamic Range	SFDR	12 Bit Mode	—	−79	—	dB
		10 Bit Mode	—	−74	—	dB
Note: 1. Absolute input pin voltage is limited by the V _{DD} supply.						

4.1.8 Voltage Reference

Table 4.8. Voltage Reference

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Internal Fast Settling Reference						
Output Voltage (Full Temperature and Supply Range)	V_{REFFS}	1.65 V Setting	1.62	1.65	1.68	V
		2.4 V Setting, $V_{DD} \geq 2.6$ V	2.35	2.4	2.45	V
Temperature Coefficient	TC_{REFFS}		—	50	—	ppm/°C
Turn-on Time	t_{REFFS}		—	—	1.5	μs
Power Supply Rejection	$PSRR_{REFFS}$		—	400	—	ppm/V
External Reference						
Input Current	I_{EXTREF}	Sample Rate = 800 ksps; $V_{REF} = 3.0$ V	—	5	—	μA

4.1.9 Temperature Sensor

Table 4.9. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Offset	V_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	757	—	mV
Offset Error ¹	E_{OFF}	$T_A = 0\text{ }^{\circ}\text{C}$	—	17	—	mV
Slope	M		—	2.85	—	mV/ $^{\circ}\text{C}$
Slope Error ¹	E_M		—	70	—	$\mu\text{V}/^{\circ}\text{C}$
Linearity			—	0.5	—	$^{\circ}\text{C}$
Turn-on Time			—	1.8	—	μs

Note:

1. Represents one standard deviation from the mean.

4.1.10 1.8 V Internal LDO Voltage Regulator

Table 4.10. 1.8V Internal LDO Voltage Regulator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage	$V_{OUT_1.8V}$		1.74	1.8	1.85	V

4.1.11 Comparators

Table 4.11. Comparators

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Response Time, CPMD = 00 (Highest Speed)	t_{RESP0}	+100 mV Differential	—	100	—	ns
		–100 mV Differential	—	150	—	ns
Response Time, CPMD = 11 (Low- est Power)	t_{RESP3}	+100 mV Differential	—	1.5	—	μs
		–100 mV Differential	—	3.5	—	μs
Positive Hysteresis Mode 0 (CPMD = 00)	HYS_{CP+}	CPHYP = 00	—	0.4	—	mV
		CPHYP = 01	—	8	—	mV
		CPHYP = 10	—	16	—	mV
		CPHYP = 11	—	32	—	mV
Negative Hysteresis Mode 0 (CPMD = 00)	HYS_{CP-}	CPHYN = 00	—	–0.4	—	mV
		CPHYN = 01	—	–8	—	mV
		CPHYN = 10	—	–16	—	mV
		CPHYN = 11	—	–32	—	mV
Positive Hysteresis Mode 1 (CPMD = 01)	HYS_{CP+}	CPHYP = 00	—	0.5	—	mV
		CPHYP = 01	—	6	—	mV
		CPHYP = 10	—	12	—	mV
		CPHYP = 11	—	24	—	mV
Negative Hysteresis Mode 1 (CPMD = 01)	HYS_{CP-}	CPHYN = 00	—	–0.5	—	mV
		CPHYN = 01	—	–6	—	mV
		CPHYN = 10	—	–12	—	mV
		CPHYN = 11	—	–24	—	mV
Positive Hysteresis Mode 2 (CPMD = 10)	HYS_{CP+}	CPHYP = 00	—	0.7	—	mV
		CPHYP = 01	—	4.5	—	mV
		CPHYP = 10	—	9	—	mV
		CPHYP = 11	—	18	—	mV
Negative Hysteresis Mode 2 (CPMD = 10)	HYS_{CP-}	CPHYN = 00	—	–0.6	—	mV
		CPHYN = 01	—	–4.5	—	mV
		CPHYN = 10	—	–9	—	mV
		CPHYN = 11	—	–18	—	mV
Positive Hysteresis Mode 3 (CPMD = 11)	HYS_{CP+}	CPHYP = 00	—	1.5	—	mV
		CPHYP = 01	—	4	—	mV
		CPHYP = 10	—	8	—	mV
		CPHYP = 11	—	16	—	mV

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative Hysteresis Mode 3 (CPMD = 11)	HYS _{CP-}	CPHYN = 00	—	-1.5	—	mV
		CPHYN = 01	—	-4	—	mV
		CPHYN = 10	—	-8	—	mV
		CPHYN = 11	—	-16	—	mV
Input Range (CP+ or CP-)	V _{IN}		-0.25	—	V _{DD} +0.25	V
Input Pin Capacitance	C _{CP}		—	7.5	—	pF
Common-Mode Rejection Ratio	CMRR _{CP}		—	70	—	dB
Power Supply Rejection Ratio	PSRR _{CP}		—	72	—	dB
Input Offset Voltage	V _{OFF}	T _A = 25 °C	-10	0	10	mV
Input Offset Tempco	TC _{OFF}		—	3.5	—	μV/°C

4.1.12 Port I/O

Table 4.12. Port I/O

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output High Voltage (Low Drive) ¹	V _{OH}	I _{OH} = -1 mA	V _{DD} - 0.7	—	—	V
Output High Voltage (High Drive) ¹	V _{OH}	I _{OH} = -3 mA	V _{DD} - 0.7	—	—	V
Output Low Voltage (Low Drive) ¹	V _{OL}	I _{OL} = 1.4 mA	—	—	0.6	V
Output Low Voltage (High Drive) ¹	V _{OL}	I _{OL} = 8.5 mA	—	—	0.6	V
Output Low Voltage (High Drive) ¹	V _{OL}	I _{OL} = 10 mA -10 °C ≤ T _A ≤ 60 °C V _{DD} = 3.0 V Guaranteed by characterization	—	0.25	0.33	V
Output Low Voltage (High Drive) ¹	V _{OL}	I _{OL} = 10 mA -10 °C ≤ T _A ≤ 60 °C V _{DD} = 3.6 V Guaranteed by characterization	—	0.23	0.31	V
Input High Voltage	V _{IH}		V _{DD} - 0.6	—	—	V
Input Low Voltage	V _{IL}		—	—	0.6	V
Pin Capacitance	C _{IO}		—	7	—	pF
Weak Pull-Up Current (V _{IN} = 0 V)	I _{PU}	V _{DD} = 3.6	-30	-20	-10	μA
Input Leakage (Pullups off or Analog)	I _{LK}	GND < V _{IN} < V _{DD}	-1.1	—	1.1	μA
Input Leakage Current with V _{IN} above V _{DD}	I _{LK}	V _{DD} < V _{IN} < V _{DD} +2.0 V	0	5	150	μA
Note: 1. See Figure 4.6 Typical V_{OH} Curves on page 33 and Figure 4.7 Typical V_{OL} Curves on page 33 for more information.						

4.1.13 SMBus

Table 4.13. SMBus Peripheral Timing Performance (Master Mode)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Standard Mode (100 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	70 ²	kHz
SMBus Operating Frequency	f_{SMB}		40 ¹	—	70 ²	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		9.4	—	—	μ s
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		4.7	—	—	μ s
Repeated START Condition Setup Time	$t_{SU:STA}$		9.4	—	—	μ s
STOP Condition Setup Time	$t_{SU:STO}$		9.4	—	—	μ s
Data Hold Time	$t_{HD:DAT}$		489 ³	—	—	ns
Data Setup Time	$t_{SU:DAT}$		448 ³	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		4.7	—	—	μ s
Clock High Period	t_{HIGH}		9.4	—	50 ⁴	μ s
Fast Mode (400 kHz Class)						
I2C Operating Frequency	f_{I2C}		0	—	255 ²	kHz
SMBus Operating Frequency	f_{SMB}		40 ¹	—	255 ²	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		2.6	—	—	μ s
Hold Time After (Repeated) START Condition	$t_{HD:STA}$		1.3	—	—	μ s
Repeated START Condition Setup Time	$t_{SU:STA}$		2.6	—	—	μ s
STOP Condition Setup Time	$t_{SU:STO}$		2.6	—	—	μ s
Data Hold Time	$t_{HD:DAT}$		489 ³	—	—	ns
Data Setup Time	$t_{SU:DAT}$		448 ³	—	—	ns
Detect Clock Low Timeout	$t_{TIMEOUT}$		25	—	—	ms
Clock Low Period	t_{LOW}		1.3	—	—	μ s
Clock High Period	t_{HIGH}		2.6	—	50 ⁴	μ s

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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Note:

1. The minimum SMBus frequency is limited by the maximum Clock High Period requirement of the SMBus specification.
2. The maximum I2C and SMBus frequencies are limited by the minimum Clock Low Period requirements of their respective specifications. The maximum frequency cannot be achieved with all combinations of oscillators and dividers available, but the effective frequency must not exceed 256 kHz.
3. Data setup and hold timing at 25 MHz or lower with EXTHOLD set to 1.
4. SMBus has a maximum requirement of 50 μ s for Clock High Period. Operating frequencies lower than 40 kHz will be longer than 50 μ s. I2C can support periods longer than 50 μ s.

Table 4.14. SMBus Peripheral Timing Formulas (Master Mode)

Parameter	Symbol	Clocks
SMBus Operating Frequency	f_{SMB}	$f_{CSO} / 3$
Bus Free Time Between STOP and START Conditions	t_{BUF}	$2 / f_{CSO}$
Hold Time After (Repeated) START Condition	$t_{HD:STA}$	$1 / f_{CSO}$
Repeated START Condition Setup Time	$t_{SU:STA}$	$2 / f_{CSO}$
STOP Condition Setup Time	$t_{SU:STO}$	$2 / f_{CSO}$
Clock Low Period	t_{LOW}	$1 / f_{CSO}$
Clock High Period	t_{HIGH}	$2 / f_{CSO}$

Note:

1. f_{CSO} is the SMBus peripheral clock source overflow frequency.

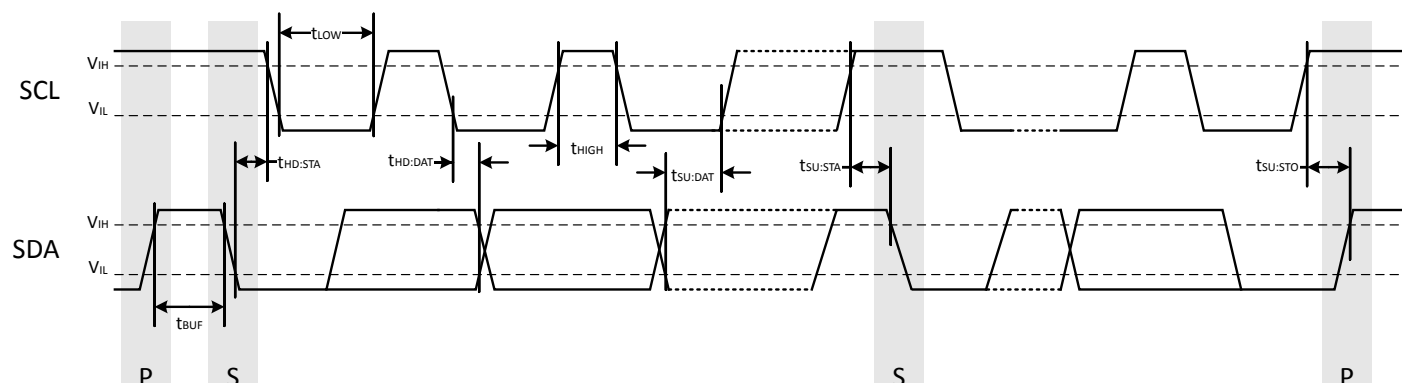


Figure 4.1. SMBus Peripheral Timing Diagram (Master Mode)

4.2 Thermal Conditions

Table 4.15. Thermal Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance (Junction to Ambient)	θ_{JA}	SOIC-16 Packages	—	70	—	°C/W
		QFN-20 Packages	—	60	—	°C/W
		QSOP-24 Packages	—	65	—	°C/W
Thermal Resistance (Junction to Case)	θ_{JC}	QFN-20 Packages	—	28.86	—	°C/W

Note:

1. Thermal resistance assumes a multi-layer PCB with any exposed pad soldered to a PCB pad.

4.3 Absolute Maximum Ratings

Stresses above those listed in [Table 4.16 Absolute Maximum Ratings on page 29](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. For more information on the available quality and reliability data, see the Quality and Reliability Monitor Report at <http://www.silabs.com/support/quality/pages/default.aspx>.

Table 4.16. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Max	Unit
Ambient Temperature Under Bias	T_{BIAS}		−55	125	°C
Storage Temperature	T_{STG}		−65	150	°C
Voltage on VDD	V_{DD}		GND−0.3	4.2	V
Voltage on I/O pins or RST	V_{IN}	$V_{DD} \geq 3.3\text{ V}$	GND−0.3	5.8	V
		$V < 3.3\text{ V}$	GND−0.3	$V_{DD}+2.5$	V
Total Current Sunk into Supply Pin	I_{VDD}		—	200	mA DD
Total Current Sourced out of Ground Pin	I_{GND}		200	—	mA
Current Sourced or Sunk by Any I/O Pin or RSTb	I_{IO}		−100	100	mA
Operating Junction Temperature	T_J	$T_A = -40\text{ °C to }85\text{ °C}$	−40	105	°C
		$T_A = -40\text{ °C to }125\text{ °C}$ (I-grade or A-grade parts only)	−40	130	°C

Exposure to maximum rating conditions for extended periods may affect device reliability.

4.4 Typical Performance Curves

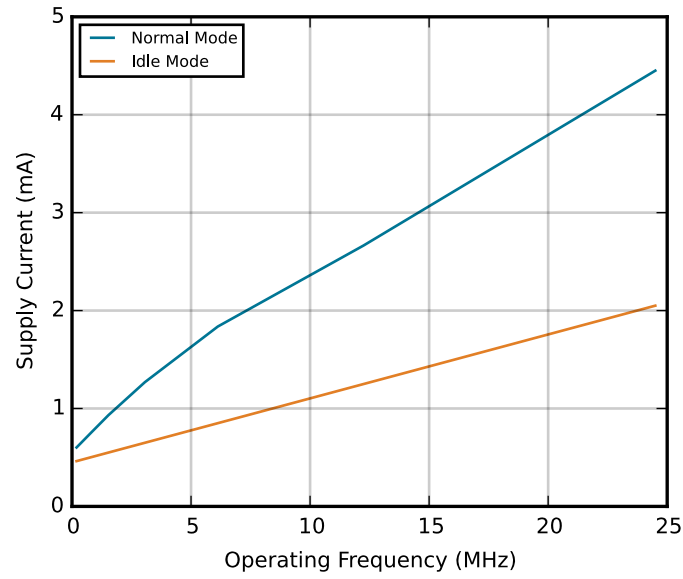


Figure 4.2. Typical Operating Supply Current using HFOSC0

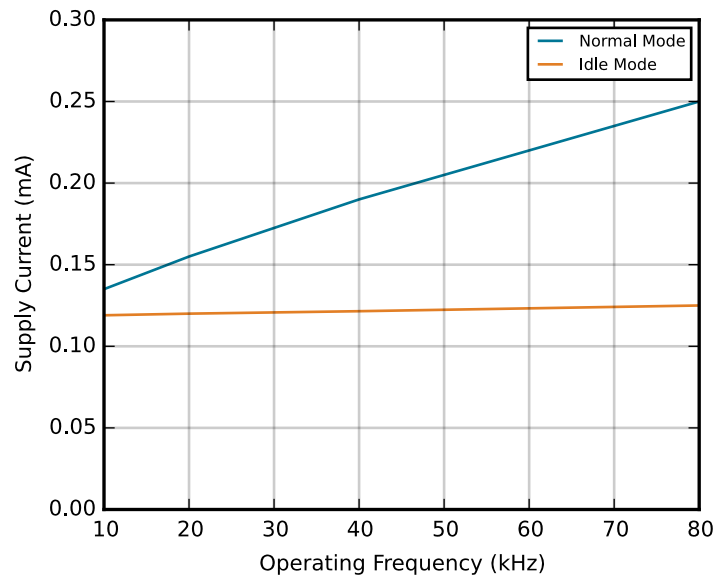


Figure 4.3. Typical Operating Supply Current using LFOSC

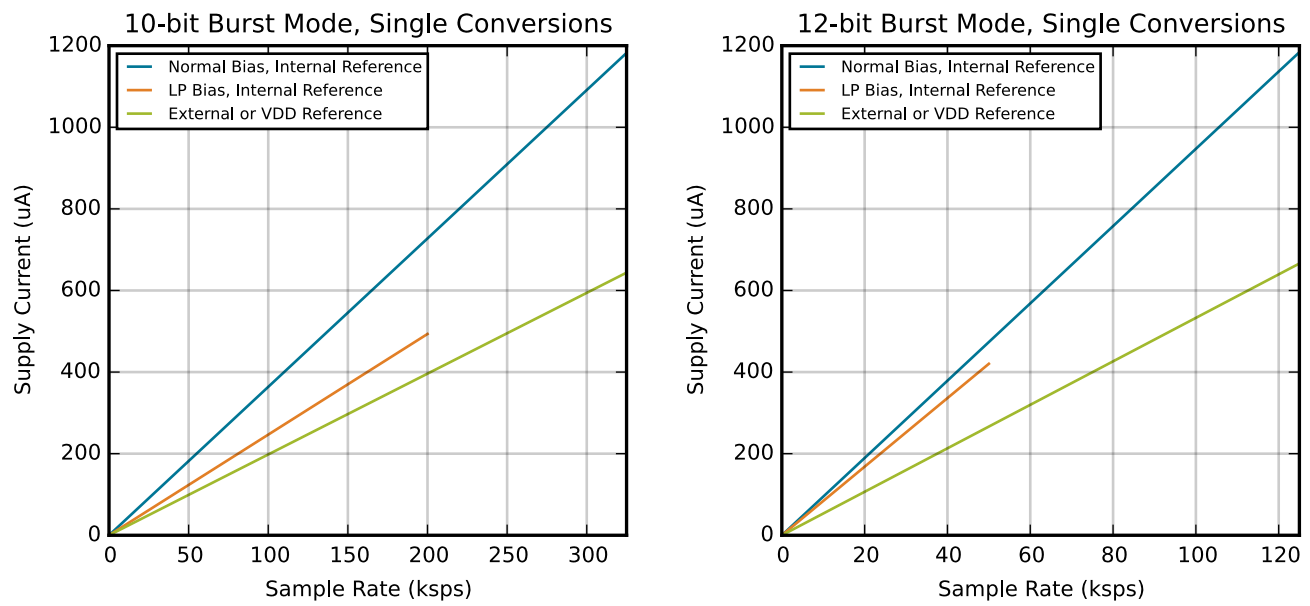


Figure 4.4. Typical ADC0 and Internal Reference Supply Current in Burst Mode

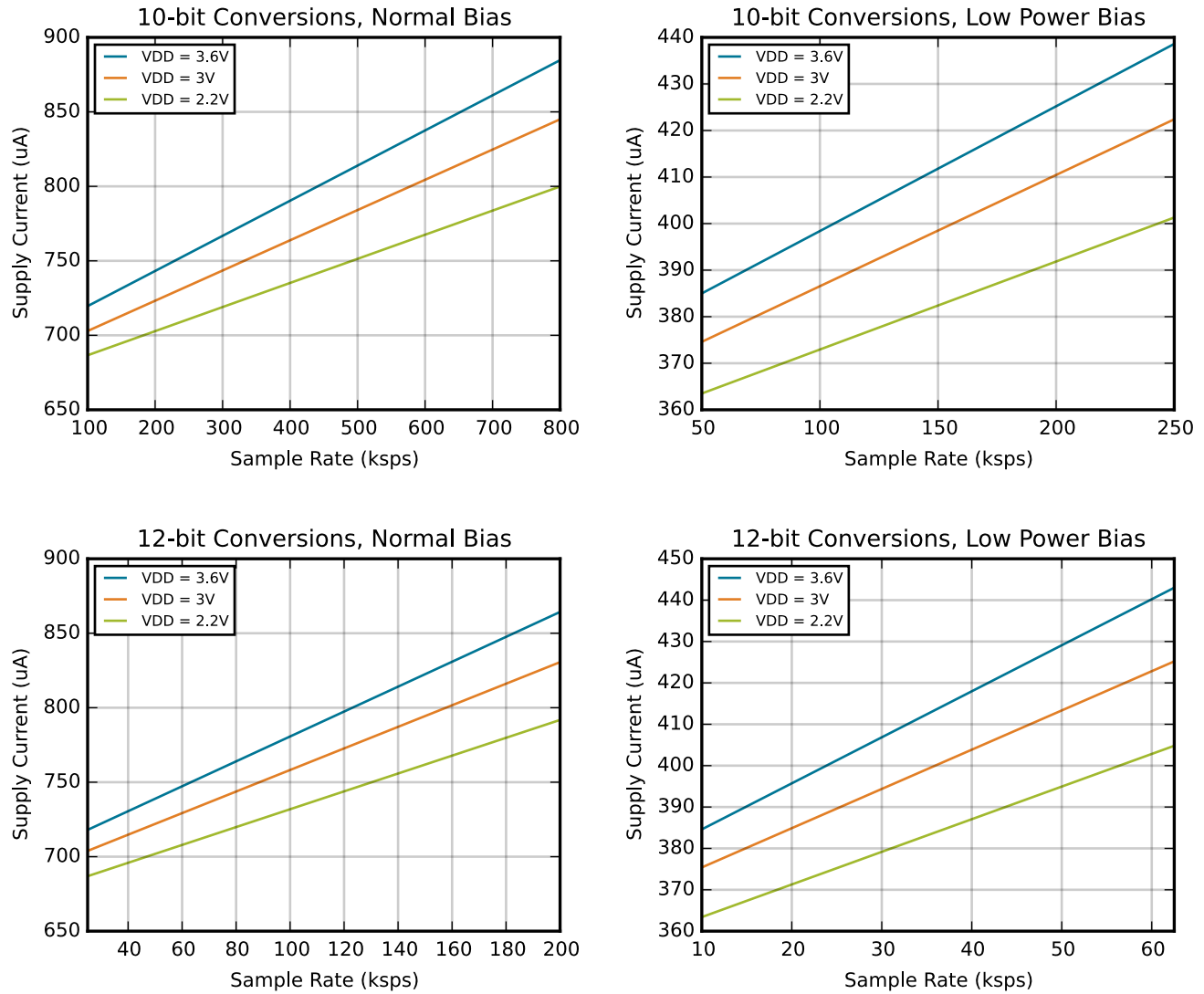


Figure 4.5. Typical ADC0 Supply Current in Normal (always-on) Mode

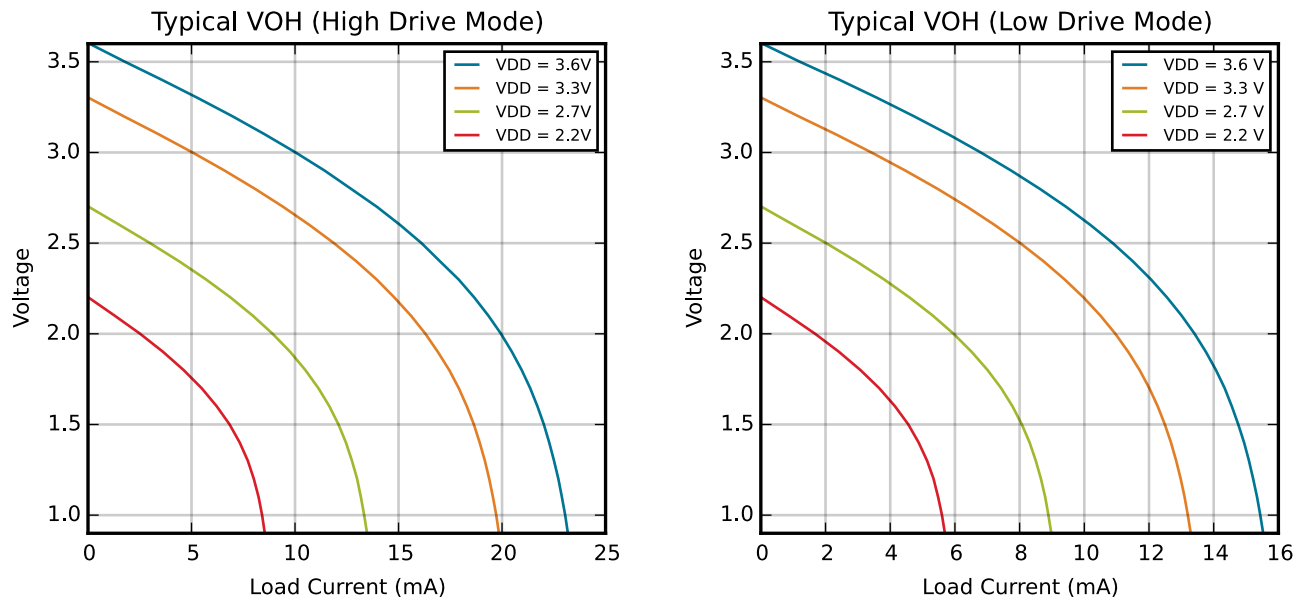


Figure 4.6. Typical V_{OH} Curves

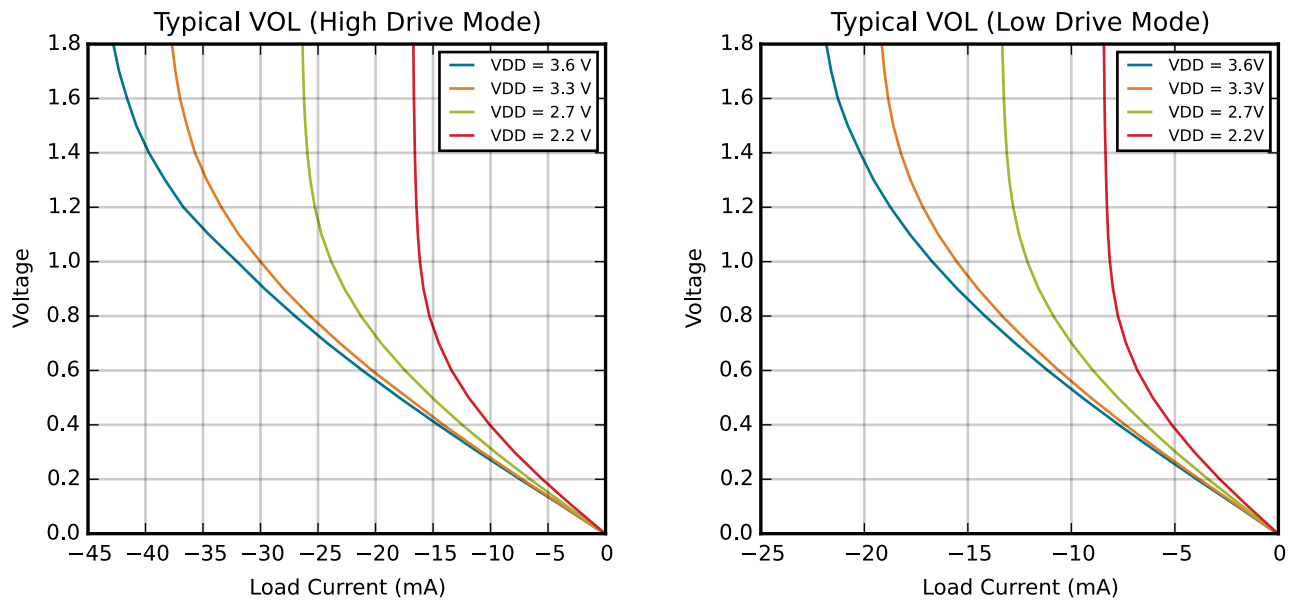


Figure 4.7. Typical V_{OL} Curves

5. Typical Connection Diagrams

5.1 Power

Figure 5.1 Power Connection Diagram on page 34 shows a typical connection diagram for the power pins of the EFM8BB1 devices.

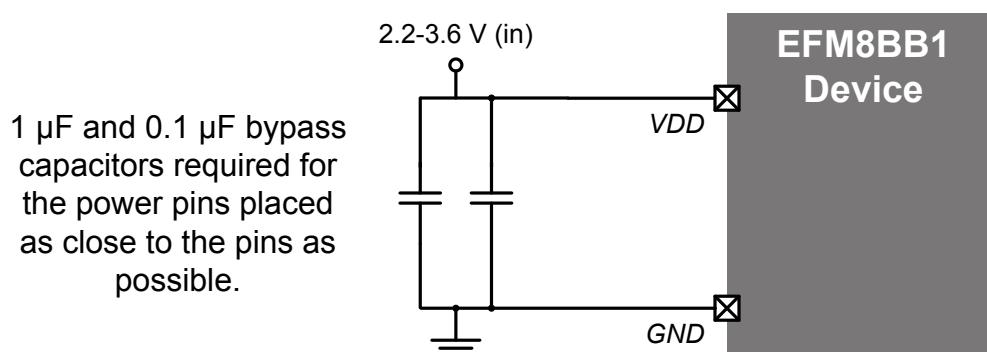


Figure 5.1. Power Connection Diagram

5.2 Debug

The diagram below shows a typical connection diagram for the debug connections pins. The pin sharing resistors are only required if the functionality on the C2D (a GPIO pin) and the C2CK (RSTb) is routed to external circuitry. For example, if the RSTb pin is connected to an external switch with debouncing filter or if the GPIO sharing with the C2D pin is connected to an external circuit, the pin sharing resistors and connections to the debug adapter must be placed on the hardware. Otherwise, these components and connections can be omitted.

For more information on debug connections, see the example schematics and information available in application note, *AN124: Pin Sharing Techniques for the C2 Interface*. Application notes can be found on the Silicon Labs website (<http://www.silabs.com/8bit-app-notes>) or in Simplicity Studio.

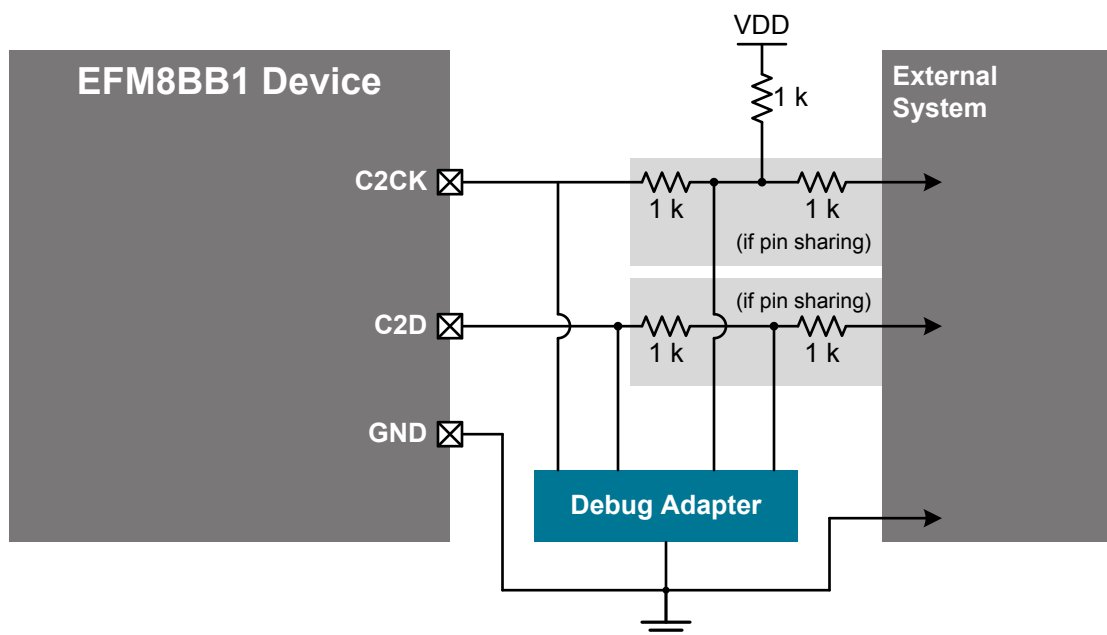


Figure 5.2. Debug Connection Diagram

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application note, "AN203: 8-bit MCU Printed Circuit Board Design Notes", contains detailed information on these connections. Application Notes can be accessed on the Silicon Labs website (www.silabs.com/8bit-appnotes).

6. Pin Definitions

6.1 EFM8BB1x-QSOP24 Pin Definitions

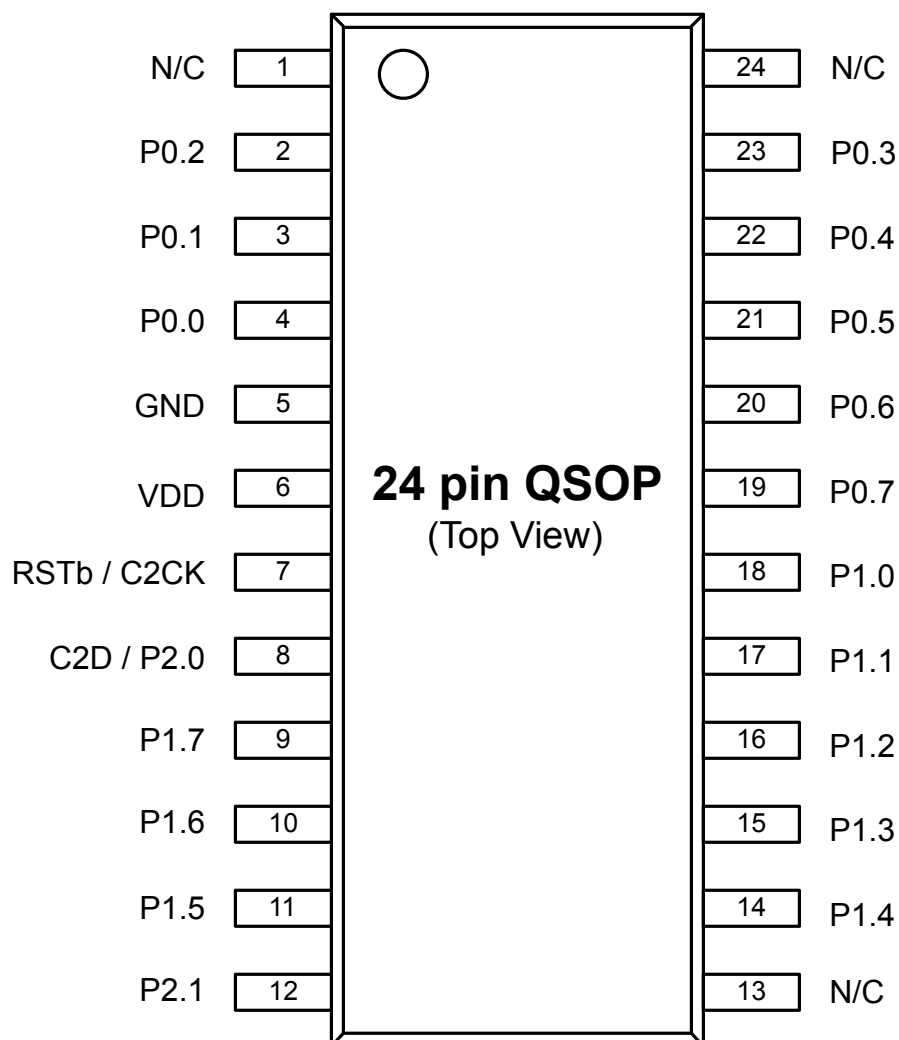


Figure 6.1. EFM8BB1x-QSOP24 Pinout

Table 6.1. Pin Definitions for EFM8BB1x-QSOP24

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	N/C	No Connection			
2	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND
4	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF
5	GND	Ground			
6	VDD	Supply Power Input			
7	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
8	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
9	P1.7	Multifunction I/O	Yes	P1MAT.7	ADC0.15 CMP1P.7 CMP1N.7
10	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.14 CMP1P.6 CMP1N.6
11	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP1P.5 CMP1N.5
12	P2.1	Multifunction I/O			
13	N/C	No Connection			
14	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
15	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
16	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
17	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1
18	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.0 CMP1N.0
19	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP0P.7 CMP0N.7
20	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.6 CMP0N.6
21	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0P.5 CMP0N.5
22	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.4 CMP0N.4
23	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3
24	N/C	No Connection			

6.2 EFM8BB1x-QFN20 Pin Definitions

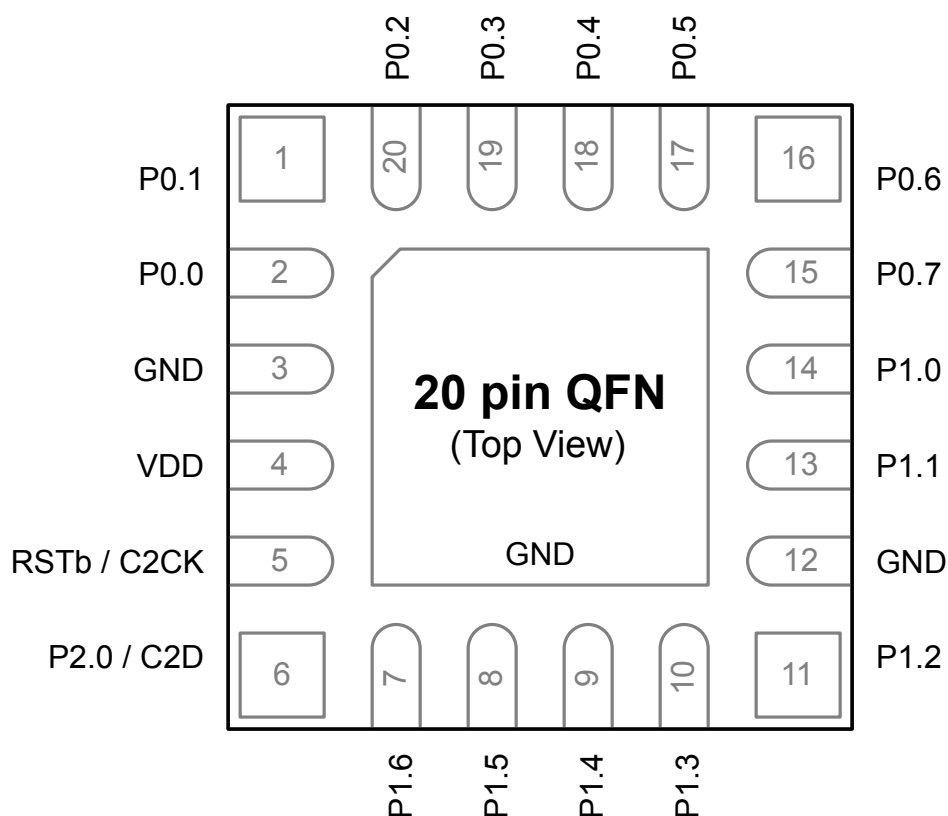


Figure 6.2. EFM8BB1x-QFN20 Pinout

Table 6.2. Pin Definitions for EFM8BB1x-QFN20

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1 AGND
2	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0 VREF

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
3	GND	Ground			
4	VDD	Supply Power Input			
5	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
6	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
7	P1.6	Multifunction I/O	Yes	P1MAT.6	ADC0.14 CMP1P.6 CMP1N.6
8	P1.5	Multifunction I/O	Yes	P1MAT.5	ADC0.13 CMP1P.5 CMP1N.5
9	P1.4	Multifunction I/O	Yes	P1MAT.4	ADC0.12 CMP1P.4 CMP1N.4
10	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.3 CMP1N.3
11	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.2 CMP1N.2
12	GND	Ground			
13	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.1 CMP1N.1
14	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.0 CMP1N.0
15	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP0P.7 CMP0N.7
16	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP0P.6 CMP0N.6

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
17	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0P.5 CMP0N.5
18	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.4 CMP0N.4
19	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3
20	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2
Center	GND	Ground			

6.3 EFM8BB1x-SOIC16 Pin Definitions

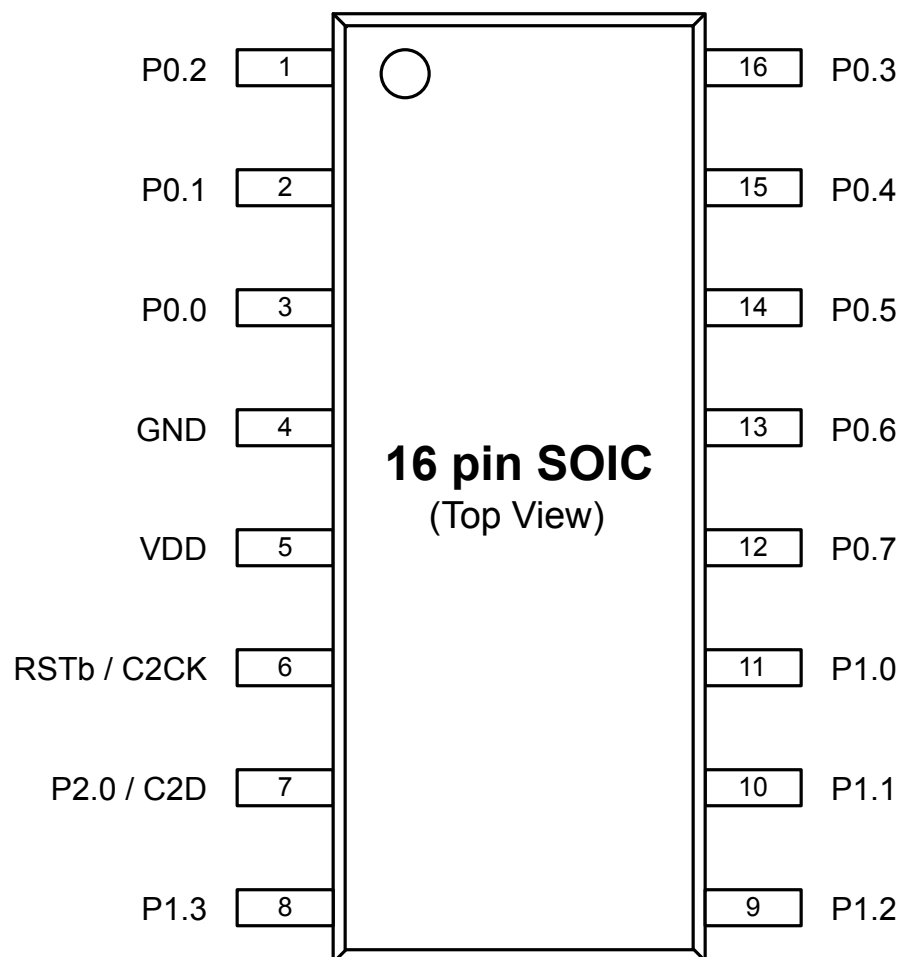


Figure 6.3. EFM8BB1x-SOIC16 Pinout

Table 6.3. Pin Definitions for EFM8BB1x-SOIC16

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
1	P0.2	Multifunction I/O	Yes	P0MAT.2 INT0.2 INT1.2	ADC0.2 CMP0P.2 CMP0N.2
2	P0.1	Multifunction I/O	Yes	P0MAT.1 INT0.1 INT1.1	ADC0.1 CMP0P.1 CMP0N.1
3	P0.0	Multifunction I/O	Yes	P0MAT.0 INT0.0 INT1.0	ADC0.0 CMP0P.0 CMP0N.0

Pin Number	Pin Name	Description	Crossbar Capability	Additional Digital Functions	Analog Functions
4	GND	Ground			
5	VDD	Supply Power Input			
6	RSTb / C2CK	Active-low Reset / C2 Debug Clock			
7	P2.0 / C2D	Multifunction I/O / C2 Debug Data			
8	P1.3	Multifunction I/O	Yes	P1MAT.3	ADC0.11 CMP1P.5 CMP1N.5
9	P1.2	Multifunction I/O	Yes	P1MAT.2	ADC0.10 CMP1P.4 CMP1N.4
10	P1.1	Multifunction I/O	Yes	P1MAT.1	ADC0.9 CMP1P.3 CMP1N.3
11	P1.0	Multifunction I/O	Yes	P1MAT.0	ADC0.8 CMP1P.2 CMP1N.2
12	P0.7	Multifunction I/O	Yes	P0MAT.7 INT0.7 INT1.7	ADC0.7 CMP1P.1 CMP1N.1
13	P0.6	Multifunction I/O	Yes	P0MAT.6 CNVSTR INT0.6 INT1.6	ADC0.6 CMP1P.0 CMP1N.0
14	P0.5	Multifunction I/O	Yes	P0MAT.5 INT0.5 INT1.5	ADC0.5 CMP0P.5 CMP0N.5
15	P0.4	Multifunction I/O	Yes	P0MAT.4 INT0.4 INT1.4	ADC0.4 CMP0P.4 CMP0N.4
16	P0.3	Multifunction I/O	Yes	P0MAT.3 EXTCLK INT0.3 INT1.3	ADC0.3 CMP0P.3 CMP0N.3

7. QSOP24 Package Specifications

7.1 QSOP24 Package Dimensions

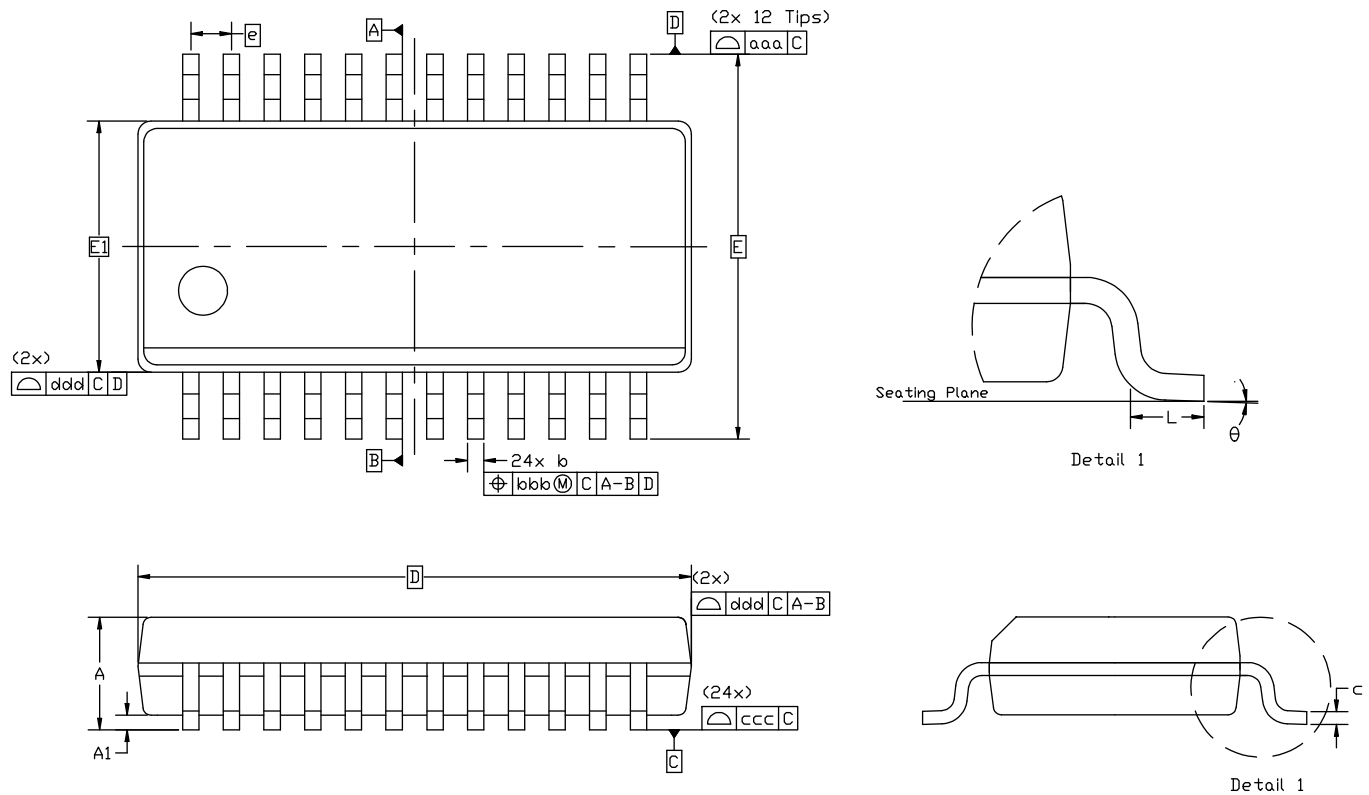


Figure 7.1. QSOP24 Package Drawing

Table 7.1. QSOP24 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
b	0.20	—	0.30
c	0.10	—	0.25
D	8.65 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	0.635 BSC		
L	0.40	—	1.27

Dimension	Min	Typ	Max
theta	0°	—	8°
aaa	0.20		
bbb	0.18		
ccc	0.10		
ddd	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-137, variation AE.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 QSOP24 PCB Land Pattern

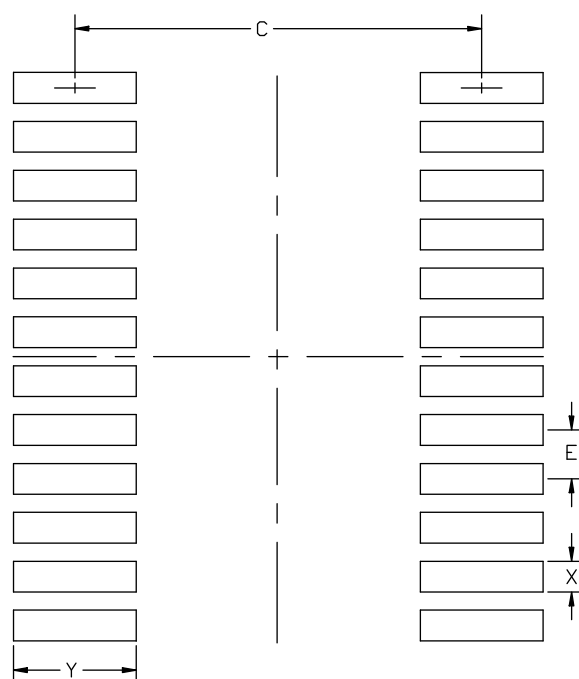


Figure 7.2. QSOP24 PCB Land Pattern Drawing

Table 7.2. QSOP24 PCB Land Pattern Dimensions

Dimension	Min	Max
C	5.20	5.30
E	0.635 BSC	
X	0.30	0.40
Y	1.50	1.60

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This land pattern design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
7. A No-Clean, Type-3 solder paste is recommended.
8. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 QSOP24 Package Marking



Figure 7.3. QSOP24 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

8. QFN20 Package Specifications

8.1 QFN20 Package Dimensions

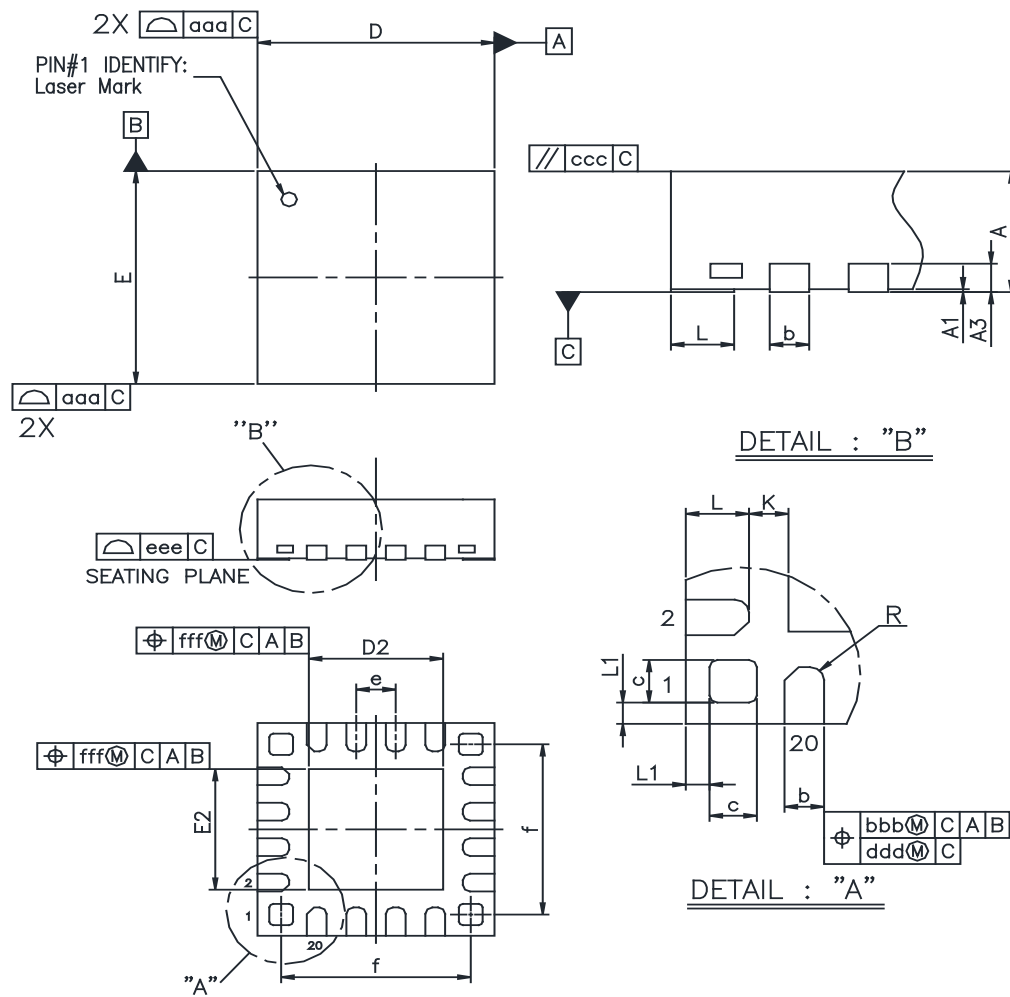


Figure 8.1. QFN20 Package Drawing

Table 8.1. QFN20 Package Dimensions

Dimension	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
c	0.25	0.30	0.35
D	3.00 BSC		
D2	1.6	1.70	1.80
e	0.50 BSC		
E	3.00 BSC		

Dimension	Min	Typ	Max
E2	1.60	1.70	1.80
f	2.50 BSC		
L	0.30	0.40	0.50
K	0.25 REF		
R	0.09	0.125	0.15
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. The drawing complies with JEDEC MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8.2 QFN20 PCB Land Pattern

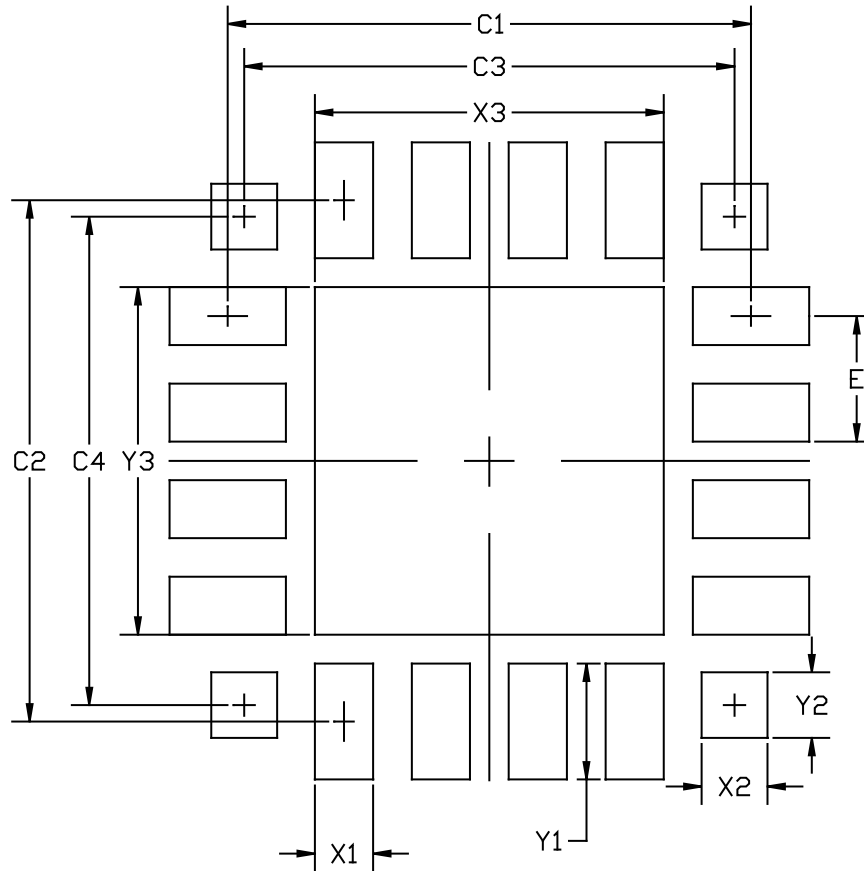


Figure 8.2. QFN20 PCB Land Pattern Drawing

Table 8.2. QFN20 PCB Land Pattern Dimensions

Dimension	Min	Max
C1		3.10
C2		3.10
C3		2.50
C4		2.50
E		0.50
X1		0.30
X2	0.25	0.35
X3		1.80
Y1		0.90
Y2	0.25	0.35
Y3		1.80

Dimension	Min	Max
Note: 1. All dimensions shown are in millimeters (mm) unless otherwise noted. 2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification. 3. This Land Pattern Design is based on the IPC-7351 guidelines. 4. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad. 5. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release. 6. The stencil thickness should be 0.125 mm (5 mils). 7. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads. 8. A 2 x 2 array of 0.75 mm openings on a 0.95 mm pitch should be used for the center pad to assure proper paste volume. 9. A No-Clean, Type-3 solder paste is recommended. 10. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.		

8.3 QFN20 Package Marking

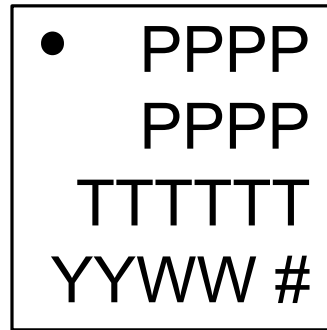


Figure 8.3. QFN20 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

9. SOIC16 Package Specifications

9.1 SOIC16 Package Dimensions

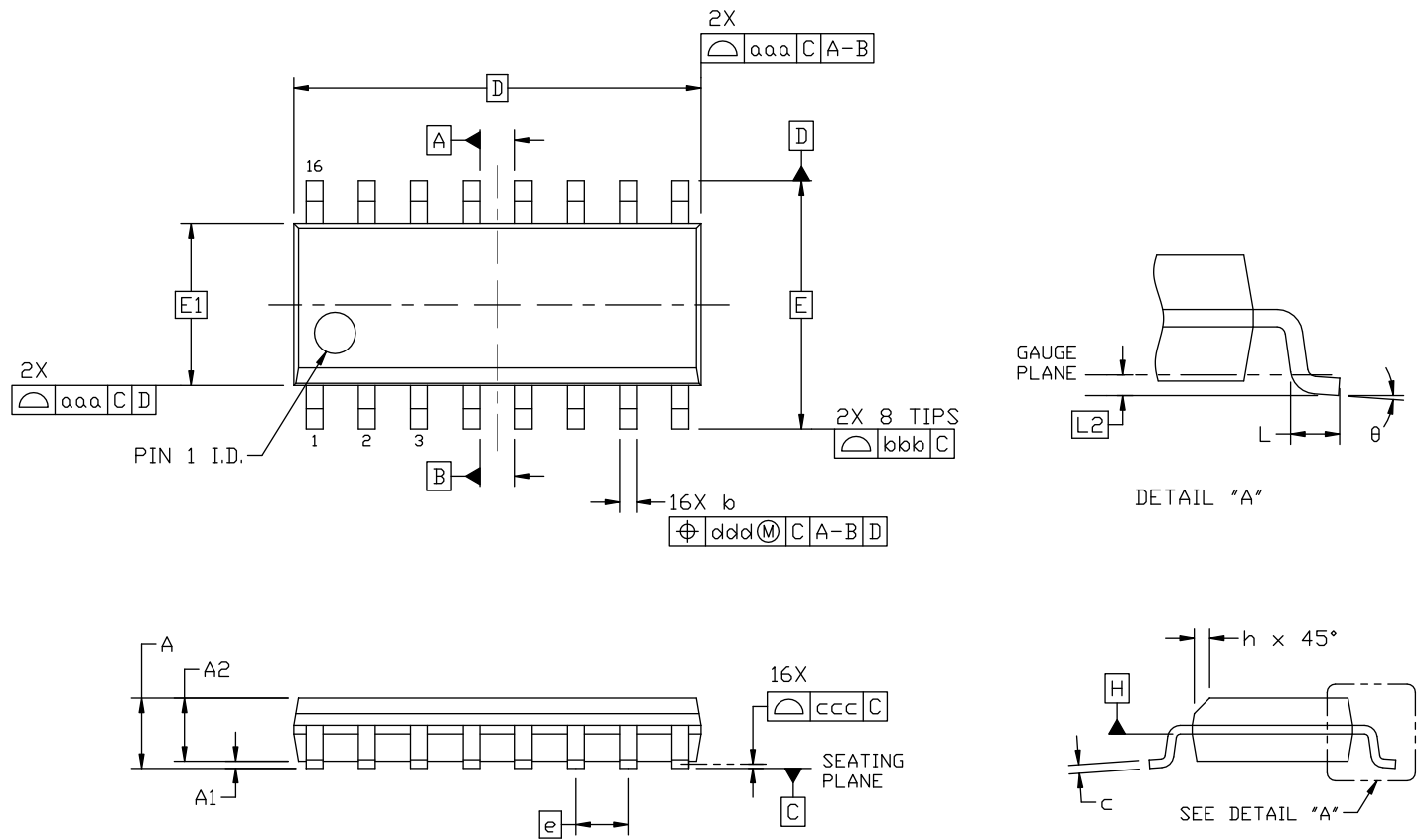


Figure 9.1. SOIC16 Package Drawing

Table 9.1. SOIC16 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.75
A1	0.10	—	0.25
A2	1.25	—	—
b	0.31	—	0.51
c	0.17	—	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
L	0.40	—	1.27

Dimension	Min	Typ	Max
L2	0.25 BSC		
h	0.25	—	0.50
θ	0°	—	8°
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9.2 SOIC16 PCB Land Pattern

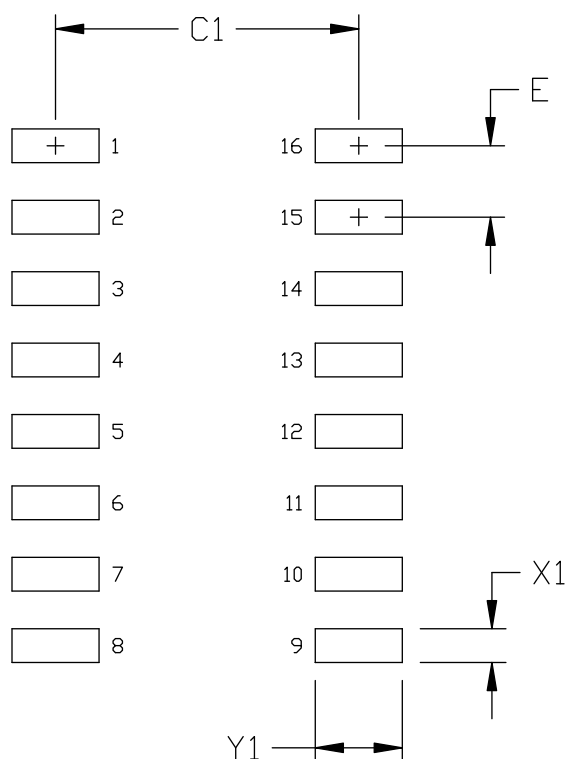


Figure 9.2. SOIC16 PCB Land Pattern Drawing

Table 9.2. SOIC16 PCB Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	5.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.55

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on IPC-7351 pattern SOIC127P600X165-16N for Density Level B (Median Land Protrusion).
3. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

9.3 SOIC16 Package Marking



Figure 9.3. SOIC16 Package Marking

The package marking consists of:

- P P P P P P P P – The part number designation.
- T T T T T T – A trace or manufacturing code.
- Y Y – The last 2 digits of the assembly year.
- W W – The 2-digit workweek when the device was assembled.
- # – The device revision (A, B, etc.).

10. Revision History

10.1 Revision 1.6

March 13th, 2017

Updated the language in [1. Feature List](#) to clarify the package offerings for each of the different temperature grades.

Corrected the application note number for *AN124: Pin Sharing Techniques for the C2 Interface* in [5.2 Debug](#).

10.2 Revision 1.5

October 7th, 2016

Added A-grade parts.

Added specifications for [4.1.13 SMBus](#).

Added bootloader pinout information to [3.10 Bootloader](#).

Added CRC Calculation Time to [4.1.4 Flash Memory](#).

Added Thermal Resistance (Junction to Case) for QFN20 packages to [4.2 Thermal Conditions](#).

Added a note linking to the Typical VOH and VOL Performance graphs in [4.1.12 Port I/O](#).

Added [4.1.10 1.8 V Internal LDO Voltage Regulator](#).

Added a note to [3.1 Introduction](#) referencing the Reference Manual.

10.3 Revision 1.4

April 22nd, 2016

Added a reference to *AN945: EFM8 Factory Bootloader User Guide* in [3.10 Bootloader](#).

Added I-grade devices.

Added a note that all GPIO values are undefined when VDD is below 1 V to [4.1.1 Recommended Operating Conditions](#).

Adjusted the Total Current Sunk into Supply Pin and Total Current Sourced out of Ground Pin specifications in [4.3 Absolute Maximum Ratings](#).

10.4 Revision 1.3

January 7th, 2016

Added [5.2 Debug](#).

Updated [3.10 Bootloader](#) to include information about the bootloader implementation.

10.5 Revision 1.2

Updated Port I/O specifications in [4.1.12 Port I/O](#) to include new V_{OL} specifications.

Added a note to [Table 4.3 Reset and Supply Monitor on page 18](#) regarding guaranteed operation.

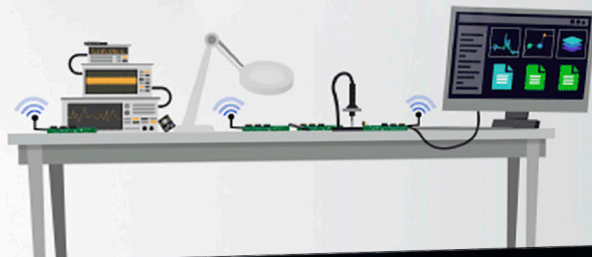
Updated package diagram and landing diagram specifications for the QFN20 package.

10.6 Revision 1.1

Initial release.

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