

Absolute Maximum Rating

Rating	Symbol	Value	Units
Steady-State Power	P _{ss}	100	mW
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V _{ESD}	>16 >10	kV
Operating Temperature	T _J	-55 to +125	°C
Storage Temperature	T _{STG}	-55 to +150	°C

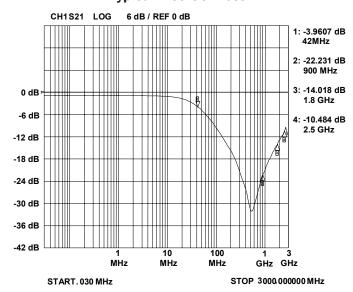
Electrical Characteristics (T=25°C)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
TVS Reverse Stand-Off Voltage	$V_{_{\mathrm{RWM}}}$				5	V
TVS Reverse Breakdown Voltage	$V_{_{BR}}$	I _t = 1mA	6			V
TVS Reverse Leakage Current	I _R	V _{RWM} = 5V, T=25°C			5	μΑ
Series Resistance	R	Each Line	8.5	10	11.5	Ohms
Total Capacitance	Стот	Any I/O to Ground $V_R = 0V$, $f = 1MHz$			160	pF

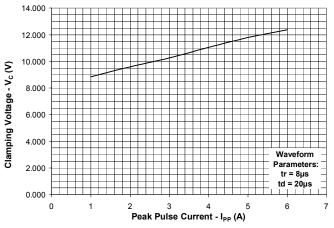


Typical Characteristics

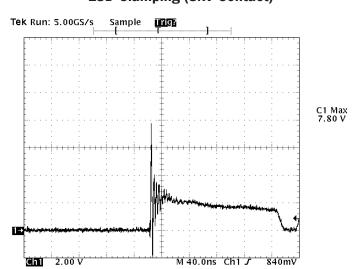
Typical Insertion loss



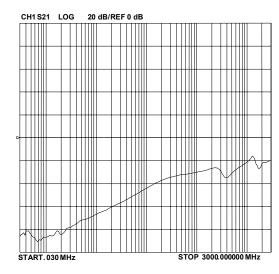
Clamping Voltage vs. Peak Pulse Current



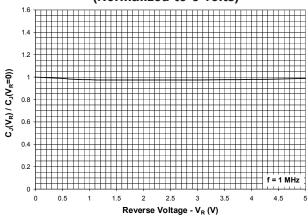
ESD Clamping (8kV Contact)



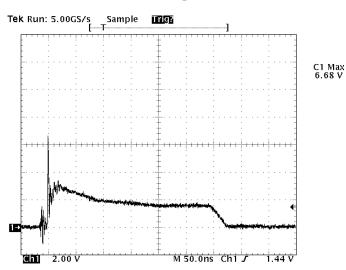
Analog Crosstalk



Capacitance vs. Reverse Voltage (Normalized to 0 volts)



ESD Clamping (15kV Air)





Applications Information

Device Connection Options

The EClamp1002A provides EMI filtering and ESD protection in a small SC-89 package for speaker port applications. The equivalent circuit diagram is shown below. The layout of the device is designed such that the data lines can be routed through the device. The first line pair enters at pins 1 and exits at pins 6. The second line pair enters at pins 3 and exits at pins 4. The device is symmetrical so the above connections may be reversed. Layout examples are shown to the right.

Circuit Board Layout Recommendations for Suppression of ESD.

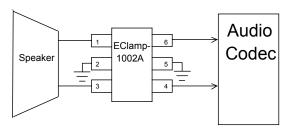
Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

- Place the TVS near the input terminals or connectors to restrict transient coupling.
- Minimize the path length between the TVS and the protected line.
- Minimize all conductive loops including power and ground loops.
- The ESD transient return path to ground should be kept as short as possible.
- Never run critical signals near board edges.
- Use ground planes whenever possible.

Matte Tin Lead Finish

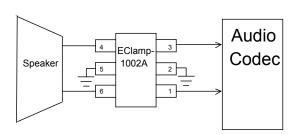
Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

Layout Examples



Option 1

Pin	Identification		
1	Line 1 In (From Speaker)		
6	Line 1 Out (To Audio Circuit)		
3	Line 2 In (From Speaker)		
4	Line 2 Out (To Audio Circuit)		
2, 5	Ground		

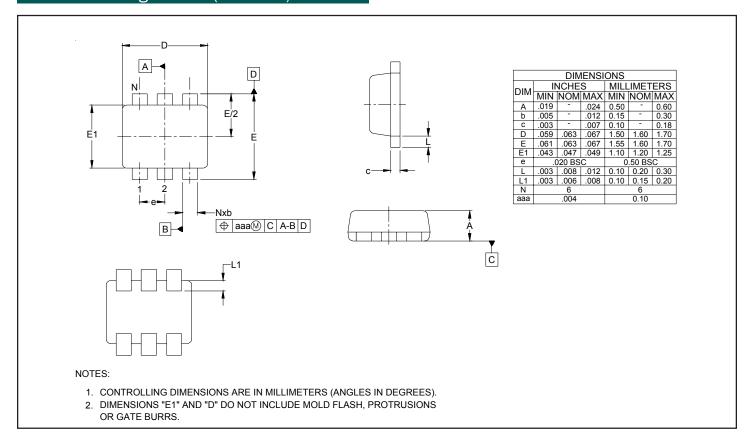


Option 2

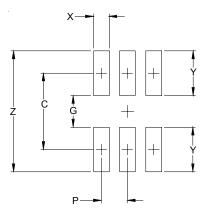
Pin	Identification		
6	Line 1 In (From Speaker)		
1	Line 1 Out (To Audio Circuit)		
4	Line 2 In (From Speaker)		
3	3 Line 2 Out (To Audio Circuit)		
2, 5	Ground		



Outline Drawing- SC-89 (SOT-666)



Land Pattern- SC-89 (SOT-666)



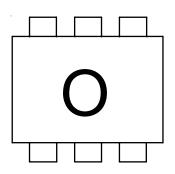
	DIMENSIONS			
DIM INCHES		MILLIMETERS		
С	(.057)	(1.45)		
Р	.020	0.50		
G	.024	0.60		
Х	.012	0.30		
Υ	.033	0.85		
7	090	2 30		

NOTES:

 THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET



Marking Code



Ordering Information

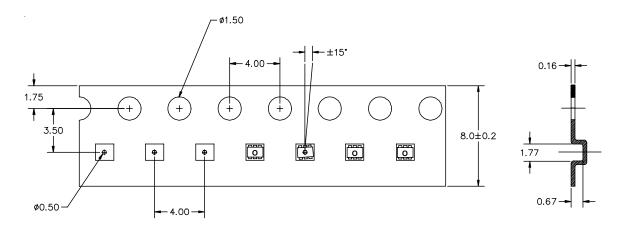
Part Number	Lead	Device	Qty per	Reel
	Finish	Marking	Reel	Size
EClamp1002A.TCT	Pb Free	0	3,000	7 Inch

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Note:

(1) Device is symmetrical so there is no pin 1 identifier.

Tape and Reel Specification



- 2 DIMENSIONS ARE IN MILLIMETERS.
- SAME AS 3M US046041.

Tape Specification and Device Orientation

Contact Information

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