

Symbol	Test Conditions	Characteristic Values		
		(T _J = 25°C unless otherwise specified)		
		min.	typ.	max.
R_G			0.3	Ω
C_{iss}			5100	pF
C_{oss}	V _{GS} = 0 V, V _{DS} = 0.8 V _{DSS(max)} , f = 1 MHz		300	pF
C_{rss}			92	pF
C_{stray}	Back Metal to any Pin		46	pF
T_{d(on)}			5	ns
T_{on}	V _{GS} = 15 V, V _{DS} = 0.8 V _{DSS} I _D = 0.5 I _{DM}		5	ns
T_{d(off)}	R _G = 0.2 Ω (External)		5	ns
T_{off}			8	ns
Q_{g(on)}			155	nC
Q_{gs}	V _{GS} = 10 V, V _{DS} = 0.5 V _{DSS} I _D = 0.5 I _{D25}		35	nC
Q_{gd}			87	nC

Source-Drain Diode		Characteristic Values		
		(T _J = 25°C unless otherwise specified)		
Symbol	Test Conditions	min.		max.
I_S	V _{GS} = 0 V			44 A
I_{SM}	Repetitive; pulse width limited by T _{JM}			288 A
V_{SD}	I _F = I _S , V _{GS} = 0 V, Pulse test, t ≤ 300 μs, duty cycle ≤ 2%			1.5 V
T_{rr}			200	ns
Q_{RM}	I _F = I _S , -di/dt = 100A/μs, V _R = 100V		0.6	μC
I_{RM}			14	A

CAUTION: Operation at or above the Maximum Ratings values may impact device reliability or cause permanent damage to the device.

Information in this document is believed to be accurate and reliable. IXYSRF reserves the right to make changes to information published in this document at any time and without notice.

For detailed device mounting and installation instructions, see the “*Device Installation & Mounting Instructions*” technical note on the IXYSRF web site at;

http://www.ixysrf.com/pdf/switch_mode/appnotes/7de_series_mosfet_installation_instructions.pdf

IXYS RF reserves the right to change limits, test conditions and dimensions.

IXYS RF MOSFETS are covered by one or more of the following U.S. patents:

4,835,592	4,860,072	4,881,106	4,891,686	4,931,844	5,017,508
5,034,796	5,049,961	5,063,307	5,187,117	5,237,481	5,486,715
5,381,025	5,640,045				

Fig. 1

Typical Transfer Characteristics
 $V_{DS} = 50V$, $PW = 15\mu s$

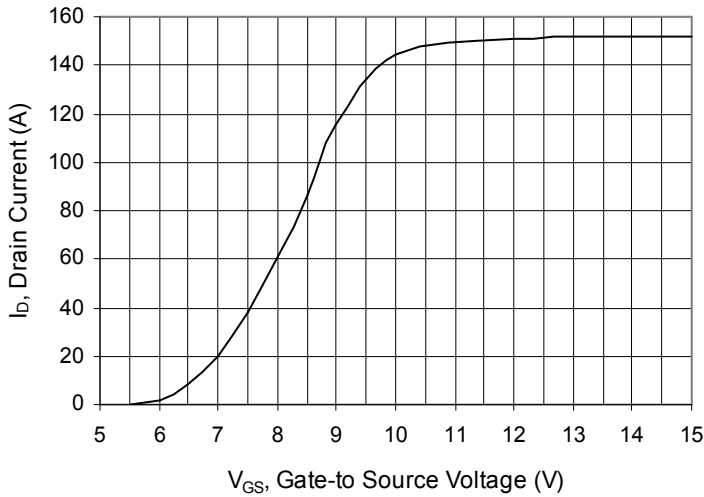


Fig. 2

Typical Output Characteristics

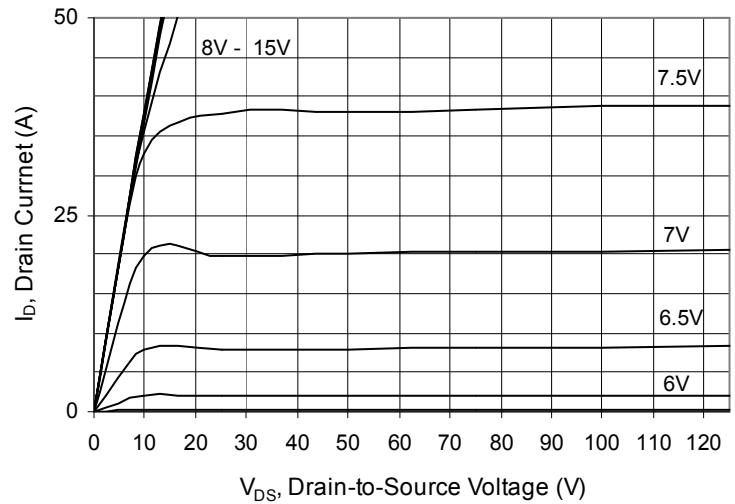


Fig. 3

Gate Charge vs. Gate-to-Source Voltage
 $V_{DS} = 250V$, $I_D = 22A$

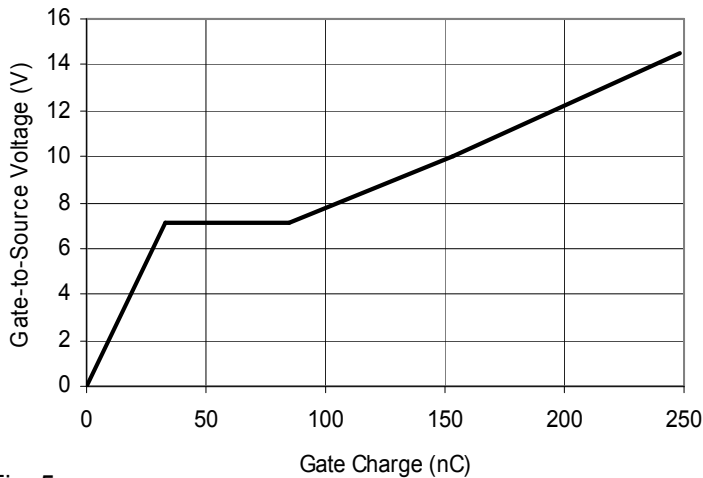


Fig. 4

Extended Typical Output Characteristics

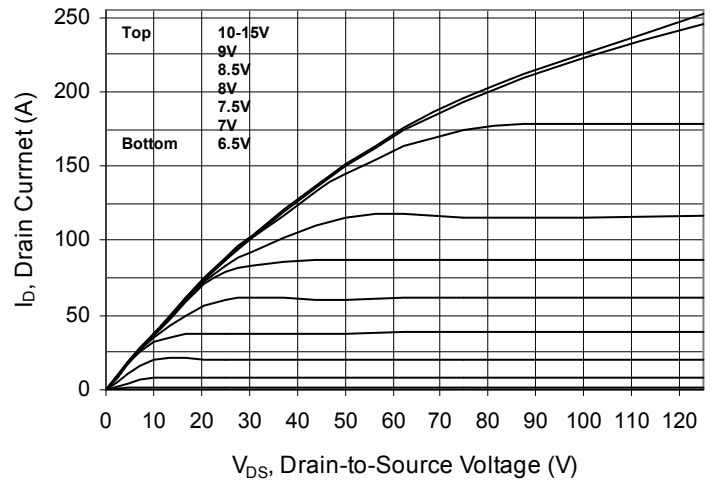
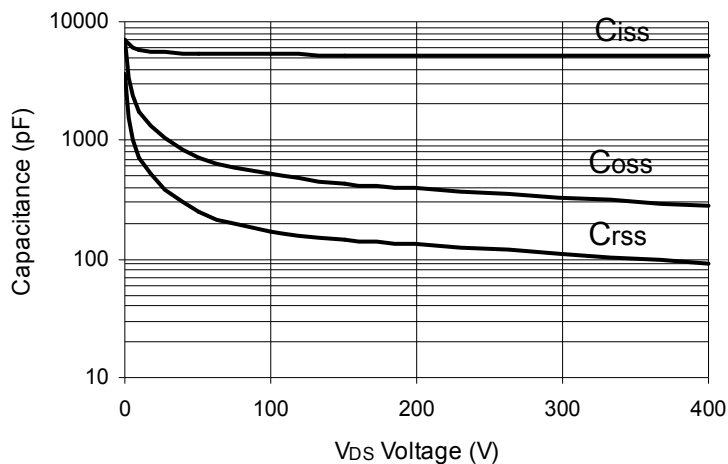


Fig. 5

V_{DS} vs. Capacitance



Technical drawing of a mechanical part, showing top and side views with dimensions in inches and millimeters.

Top View Dimensions:

- Overall width: 1.600 [40.64]
- Overall height: 0.830 [21.08]
- Left side features:
 - Source: 0.306 [7.77]
 - Gate: 0.070 [1.78]
 - Source: 0.162 [4.11]
- Right side features:
 - Source: 0.050 [1.27]
 - Drain: 0.346 [8.79]
 - Source: 0.770 [19.56]
- Internal features:
 - Top center: 0.915 [23.24]
 - Bottom center: 0.050 [1.27]

Side View Dimensions:

- Overall height: 0.125 [3.18]
- Overall width: 0.006 [0.15]
- Overall depth: 0.049 [1.24]

501N44A DE-SERIES SPICE Model (Preliminary)

The DE-SERIES SPICE Model is illustrated in Figure 7. The model is an expansion of the SPICE level 3 MOSFET model. It includes the stray inductive terms L_G , L_S and L_D . R_d is the $R_{DS(ON)}$ of the device, R_{ds} is the resistive leakage term. The output capacitance, C_{OSS} , and reverse transfer capacitance, C_{RSS} are modeled with reversed biased diodes. This provides a varactor type response necessary for a high power device model. The turn on delay and the turn off delay are adjusted via R_{on} and R_{off} .

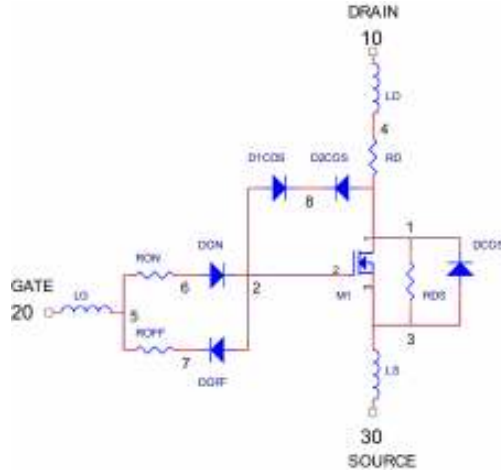


Figure 7 DE-SERIES SPICE Model

This SPICE model may be downloaded as a text file from the IXYSRF web site at

http://www.ixysrf.com/products/switch_mode.html

<http://www.ixysrf.com/spice/de475-501n44a.html>

Net List:

.SUBCKT 501N44A 10 20 30

* TERMINALS: D G S

* 500 Volt 44 Amp 0.13 ohm N-Channel Power MOSFET

* REV.A 01-09-02

M1 1 2 3 3 DMOS L=1U W=1U

RON 5 6 0.3

DON 6 2 D1

ROF 5 7 .1

DOF 2 7 D1

D1CRS 2 8 D2

D2CRS 1 8 D2

CGS 2 3 5.2N

RD 4 1 0.13

DCOS 3 1 D3

RDS 1 3 5.0MEG

LS 3 30 .5N

LD 10 4 1N

LG 20 5 1N

.MODEL DMOS NMOS (LEVEL=3 VTO=3.0 KP=3.8)

.MODEL D1 D (IS=.5F CJO=1P BV=100 M=.5 VJ=.6 TT=1N)

.MODEL D2 D (IS=.5F CJO=400P BV=500 M=.4 VJ=.6 TT=400N RS=10M)

.MODEL D3 D (IS=.5F CJO=900P BV=500 M=.3 VJ=.4 TT=400N RS=10M)

.ENDS

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