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## Selection Guide

Description		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Automotive-A	100	95	–	mA
	Automotive-E	–	–	95	mA
Maximum CMOS Standby Current	Automotive-A	10	10	–	mA
	Automotive-E	–	–	15	mA

## Pin Configuration

Figure 1. 36-pin SOJ pinout (Top View)

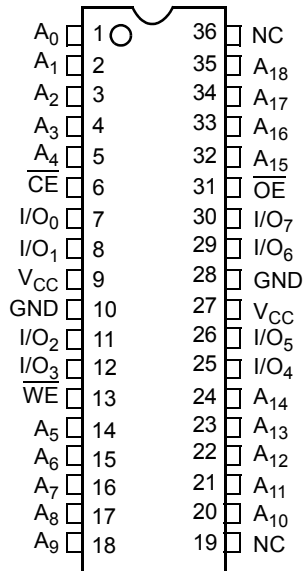
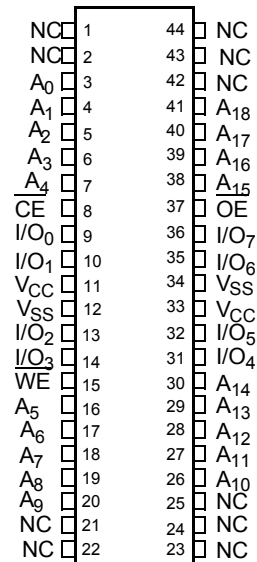


Figure 2. 44-pin TSOP II pinout (Top View)



## Pin Definitions

Pin Name	36-pin SOJ Pin Number	44-pin TSOP II Pin Number	I/O Type	Description
A <sub>0</sub> –A <sub>18</sub>	1–5, 14–18, 20–24, 32–35	3–7, 16–20, 26–30, 38–41	Input	<b>Address inputs used to select one of the address locations.</b>
I/O <sub>0</sub> –I/O <sub>7</sub>	7, 8, 11, 12, 25, 26, 29, 30	9, 10, 13, 14, 31, 32, 35, 36	Input/Output	<b>Bidirectional data I/O lines.</b> Used as input or output lines depending on operation.
NC <sup>[1]</sup>	19, 36	1, 2, 21, 22, 23, 24, 25, 42, 43, 44	No Connect	<b>No connects.</b> This pin is not connected to the die.
$\overline{\text{WE}}$	13	15	Input/Control	<b>Write Enable input, active LOW.</b> When selected LOW, a WRITE is conducted.
$\overline{\text{CE}}$	6	8	Input/Control	<b>Chip Enable input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{OE}}$	31	37	Input/Control	<b>Output Enable, active LOW.</b> Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-state, and act as input data pins.
V <sub>SS</sub> , GND	10, 28	12, 34	Ground	<b>Ground for the device.</b> Should be connected to ground of the system.
V <sub>CC</sub>	9, 27	11, 33	Power Supply	<b>Power supply inputs to the device.</b>

### Note

1. NC pins are not connected on the die.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65 °C to +150 °C

Ambient Temperature with  
Power Applied ..... -55 °C to +125 °C

Supply Voltage on  
 $V_{CC}$  to Relative GND <sup>[2]</sup> ..... -0.5 V to +4.6 VDC

Voltage Applied to Outputs  
in High Z State <sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Input Voltage <sup>[2]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into Outputs (LOW) ..... 20 mA

Static discharge voltage  
(MIL-STD-883, Method 3015) ..... > 2001 V

Latch up current ..... > 200 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$
Automotive-A	-40 °C to +85 °C	3.3 V ± 0.3 V
Automotive-E	-40 °C to +125 °C	

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10		-12		-15		Unit
				Min	Max	Min	Max	Min	Max	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min; I <sub>OH</sub> = −4.0 mA		2.4	–	2.4	–	2.4	–	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min; I <sub>OL</sub> = 8.0 mA		–	0.4	–	0.4	–	0.4	V
V <sub>IH</sub>	Input HIGH Voltage			2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	2.0	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[2]</sup>			−0.3	0.8	−0.3	0.8	−0.3	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	Auto-A	−1	+1	−1	+1	–	–	μA
			Auto-E	–	–	–	–	−20	+20	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>	Auto-A	–	100	–	95	–	–	mA
			Auto-E	–	–	–	–	–	95	
I <sub>SB1</sub>	Automatic CE Power Down Current – TTL Inputs	Max. V <sub>CC</sub> , $\overline{CE} \geq V_{IH}$ ; V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>	Auto-A	–	40	–	40	–	–	mA
			Auto-E	–	–	–	–	–	45	mA
I <sub>SB2</sub>	Automatic CE Power Down Current – CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> − 0.3 V, V <sub>IN</sub> ≥ V <sub>CC</sub> − 0.3 V, or V <sub>IN</sub> ≤ 0.3 V, f = 0	Auto-A	–	10	–	10	–	–	mA
			Auto-E	–	–	–	–	–	15	mA

### Note

2.  $V_{IL(\text{min})} = -2.0 \text{ V}$  and  $V_{IH(\text{max})} = V_{CC} + 0.5 \text{ V}$  for pulse durations of less than 20 ns.

## Capacitance

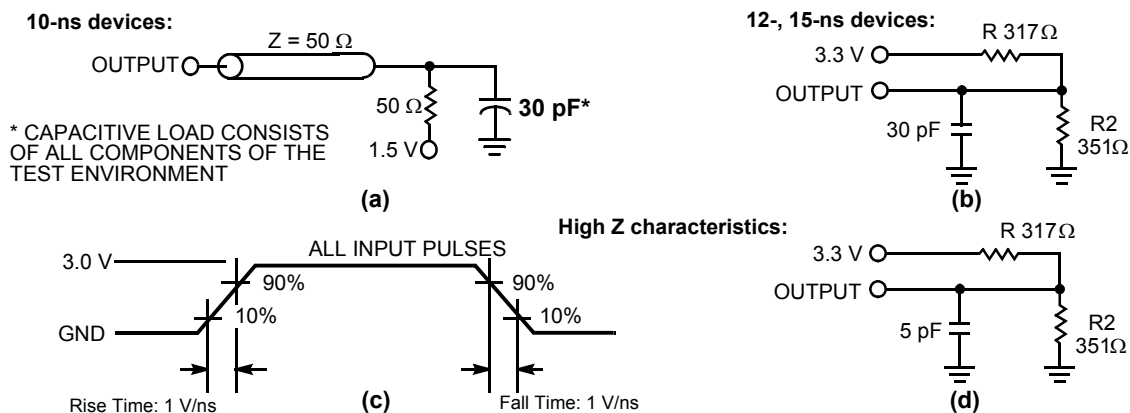
Parameter <sup>[3]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$	8	pF
$C_{OUT}$	Output capacitance		8	pF

## Thermal Resistance

Parameter <sup>[3]</sup>	Description	Test Conditions	36-pin SOJ	44-pin TSOP II	Unit
$\Theta_{JA}$	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	46.51	41.66	$^\circ\text{C/W}$
$\Theta_{JC}$	Thermal resistance (junction to case)		18.8	10.56	$^\circ\text{C/W}$

## AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms <sup>[4]</sup>



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) for 10 ns parts are tested using the load conditions shown in Figure 3 (a). All other speeds are tested using the Thevenin load shown in Figure 3 (b). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (d).

## AC Switching Characteristics

Over the Operating Range

Parameter <sup>[5]</sup>	Description	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t <sub>power</sub> <sup>[6]</sup>	V <sub>CC</sub> (typical) to the first access	100	–	100	–	100	–	μs
t <sub>RC</sub>	Read Cycle Time	10	–	12	–	15	–	ns
t <sub>AA</sub>	Address to Data Valid	–	10	–	12	–	15	ns
t <sub>OHA</sub>	Data Hold from Address Change	3	–	3	–	–	3	ns
t <sub>ACE</sub>	$\overline{\text{CE}}$ LOW to Data Valid	–	10	–	12	–	15	ns
t <sub>DOE</sub>	$\overline{\text{OE}}$ LOW to Data Valid	–	5	–	6	–	7	ns
t <sub>LZOE</sub>	$\overline{\text{OE}}$ LOW to Low Z <sup>[7]</sup>	0	–	0	–	0	–	ns
t <sub>HZOE</sub>	$\overline{\text{OE}}$ HIGH to High Z <sup>[7, 8]</sup>	–	5	–	6	–	7	ns
t <sub>LZCE</sub>	$\overline{\text{CE}}$ LOW to Low Z <sup>[7]</sup>	3	–	3	–	3	–	ns
t <sub>HZCE</sub>	$\overline{\text{CE}}$ HIGH to High Z <sup>[7, 8]</sup>	–	5	–	6	–	7	ns
t <sub>PU</sub>	$\overline{\text{CE}}$ LOW to Power Up	0	–	0	–	0	–	ns
t <sub>PD</sub>	$\overline{\text{CE}}$ HIGH to Power Down	–	10	–	12	–	15	ns
Write Cycle <sup>[9, 10]</sup>								
t <sub>WC</sub>	Write Cycle Time	10	–	12	–	15	–	ns
t <sub>SCE</sub>	$\overline{\text{CE}}$ LOW to Write End	7	–	8	–	10	–	ns
t <sub>AW</sub>	Address Setup to Write End	7	–	8	–	10	–	ns
t <sub>HA</sub>	Address Hold from Write End	0	–	0	–	0	–	ns
t <sub>SA</sub>	Address Setup to Write Start	0	–	0	–	0	–	ns
t <sub>PWE</sub>	$\overline{\text{WE}}$ Pulse Width	7	–	8	–	10	–	ns
t <sub>SD</sub>	Data Setup to Write End	5	–	6	–	7	–	ns
t <sub>HD</sub>	Data Hold from Write End	0	–	0	–	0	–	ns
t <sub>LZWE</sub>	$\overline{\text{WE}}$ HIGH to Low Z <sup>[7]</sup>	3	–	3	–	3	–	ns
t <sub>HZWE</sub>	$\overline{\text{WE}}$ LOW to High Z <sup>[7, 8]</sup>	–	5	–	6	–	7	ns

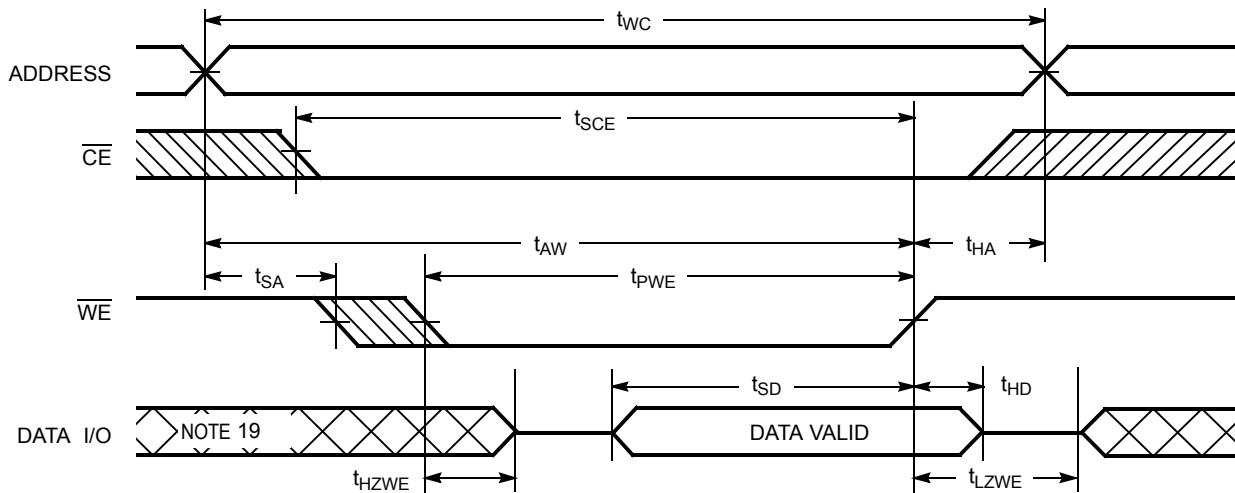
### Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
- $t_{\text{POWER}}$  gives the minimum amount of time that the power supply should be at stable, typical  $V_{\text{CC}}$  values until the first memory access can be performed.
- At any temperature and voltage condition,  $t_{\text{HZCE}}$  is less than  $t_{\text{LZCE}}$ ,  $t_{\text{HZOE}}$  is less than  $t_{\text{LZOE}}$ , and  $t_{\text{HZWE}}$  is less than  $t_{\text{LZWE}}$  for any device.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ , and  $t_{\text{HZWE}}$  are specified with a load capacitance of 5 pF as in part (d) of Figure 3 on page 5. Transition is measured  $\pm 500$  mV from steady-state voltage.
- The internal Write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}$  and  $\overline{\text{WE}}$  must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the Write.
- The minimum Write cycle time for Write Cycle No. 2 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{\text{HZWE}}$  and  $t_{\text{SD}}$ .



**Switching Waveforms** (continued)

**Figure 7. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW) [17, 18]**



**Notes**

17. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  HIGH, the output remains in high impedance state.
18. The minimum Write cycle time for Write Cycle No. 2 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
19. During this period, the I/Os are in output state. Do not apply input signals.

**Truth Table**

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> –I/O <sub>7</sub>	Mode	Power
H	X	X	High Z	Power Down	Standby (I <sub>SB</sub> )
L	L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	X	L	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )



## Ordering Information

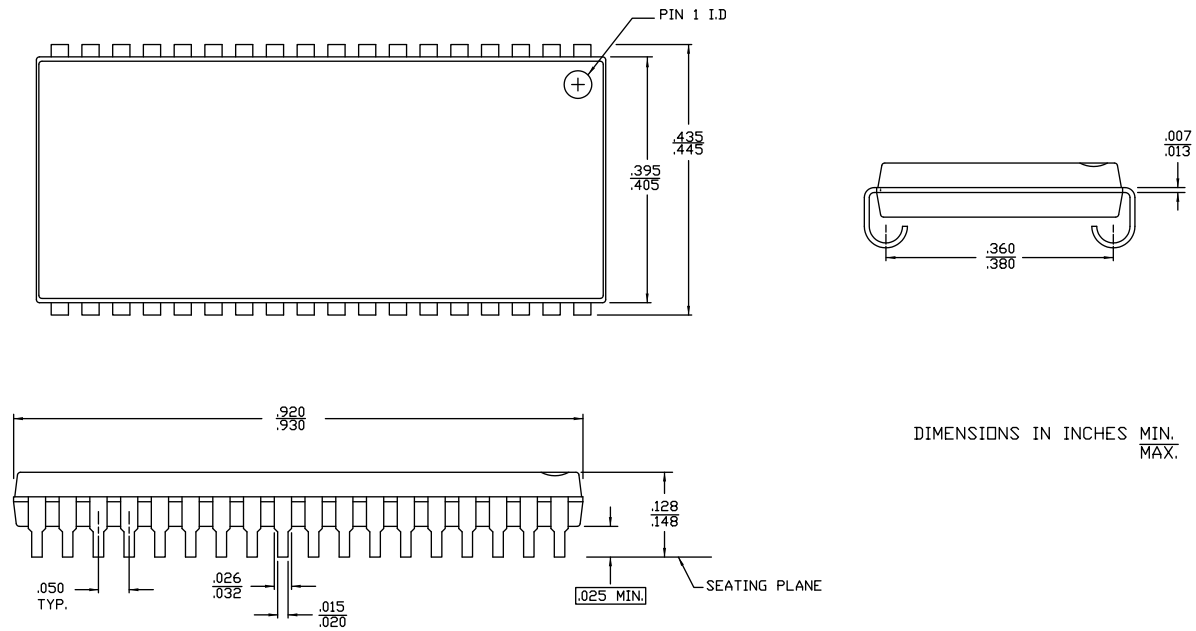
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1049CV33-10VXA	51-85090	36-pin (400-Mil) Molded SOJ (Pb-free)	Automotive-A
12	CY7C1049CV33-12ZSXA	51-85087	44-pin TSOP II (Pb-free)	Automotive-A
15	CY7C1049CV33-15VXE	51-85090	36-pin (400-Mil) Molded SOJ (Pb-free)	Automotive-E
	CY7C1049CV33-15ZSXE	51-85087	44-pin TSOP II (Pb-free)	Automotive-E

## Ordering Code Definitions

CY	7	C	1	04	9	C	V33	-	XX	XX	X	X	
													Temperature Range: X = A or E A = Automotive-A or E = Automotive-E
													X = Pb-free; X Absent = Leaded
													Package Type: XX = V or ZS V = 36-pin (400-Mil) Molded SOJ ZS = 44-pin TSOP II
													Speed Grade: XX = 10 ns or 12 ns or 15 ns
													V33 = 3.0 V to 3.6 V
													Process Technology: C = 150 nm
													Data width: 9 = × 8-bits
													Density: 04 = 4-Mbit density
													Family Code: 1 = Fast Asynchronous SRAM
													Technology Code: C = CMOS
													Marketing Code: 7 = SRAM
													Company ID: CY = Cypress

## Package Diagrams

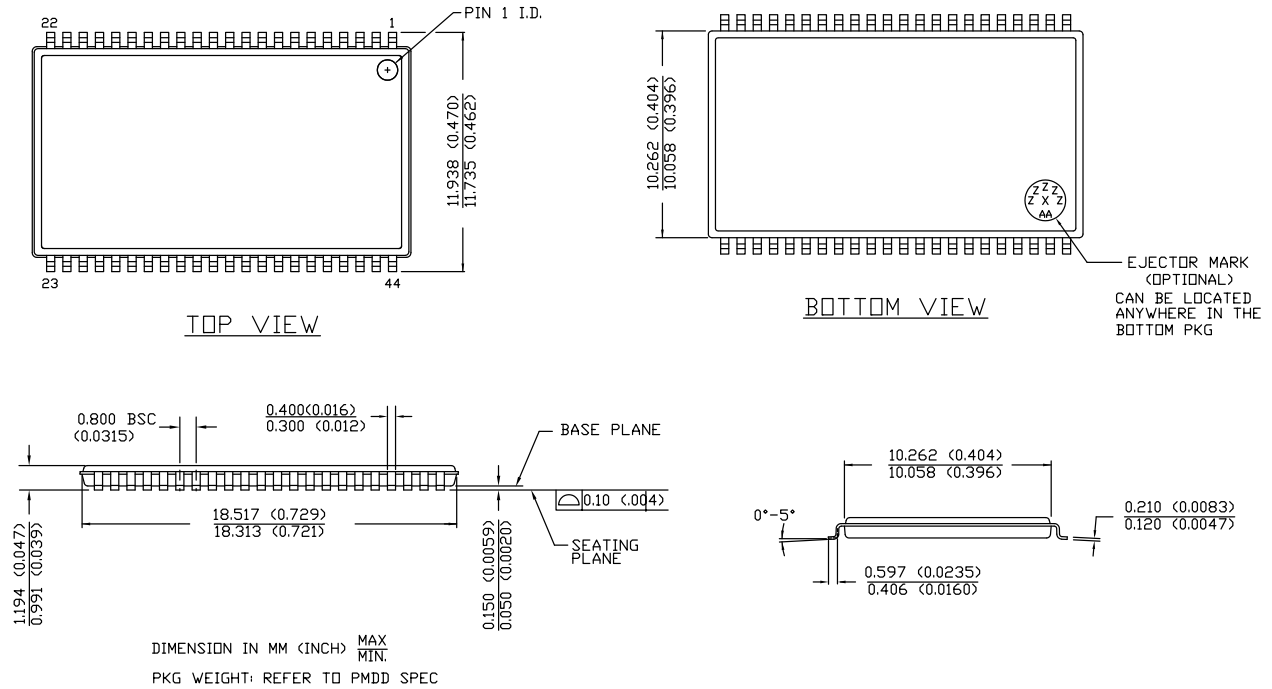
**Figure 8. 36-pin SOJ V36.4 (Molded) Package Outline, 51-85090**



51-85090 \*F

## Package Diagrams (continued)

Figure 9. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 \*E

## Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C1049CV33 Automotive, 4-Mbit (512 K × 8) Static RAM Document Number: 001-67511				
Rev.	ECN	Orig. of Change	Submission Date	Description of Change
**	3186792	PRAS	03/03/2011	Separation of the automotive data sheet from CY7C1049CV33 spec no. 38-05006 Rev. *J. Further rev of 38-05006 would include only industrial / commercial parts.
*A	3265070	PRAS	05/24/2011	Updated <a href="#">Functional Description</a> (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines."). Updated in new template.
*B	3546915	NILE	03/09/2012	Updated <a href="#">Pin Definitions</a> (Updated description of $\overline{WE}$ and $\overline{OE}$ pins). Updated <a href="#">Package Diagrams</a> .
*C	4311615	NILE / VINI	03/21/2014	Updated <a href="#">Maximum Ratings</a> : Added "Static discharge voltage" and "Latch up current" details.  Updated <a href="#">AC Switching Characteristics</a> : Updated Note 10.  Updated <a href="#">Switching Waveforms</a> : Added Note 18 and referred the same note in <a href="#">Figure 7</a> .  Updated <a href="#">Package Diagrams</a> : spec 51-85087 – Changed revision from *D to *E.  Updated in new template.  Completing Sunset Review.

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