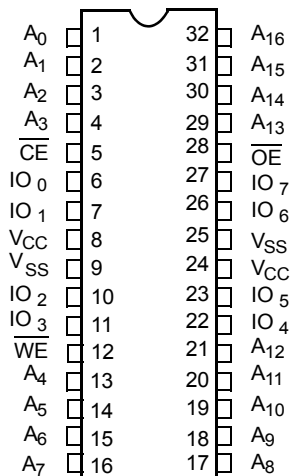


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Pin Configuration

Figure 1. 32-pin SOJ / TSOP II pinout (Top View)



Selection Guide

Description	-10 (Industrial)	Unit
Maximum Access Time	10	ns
Maximum Operating Current	80	mA
Maximum Standby Current	3	mA

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature -65 °C to +150 °C

Ambient Temperature with
Power Applied -55 °C to +125 °C

Supply Voltage on
 V_{CC} to Relative GND ^[2] -0.5 V to +6.0 V

DC Voltage Applied to Outputs
in High Z State ^[2] -0.5 V to $V_{CC} + 0.5$ V

DC Input Voltage ^[2] -0.5 V to $V_{CC} + 0.5$ V

Current into Outputs (LOW) 20 mA

Static Discharge Voltage
(per MIL-STD-883, Method 3015) > 2001 V

Latch-up Current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	-40 °C to +85 °C	5 V ± 0.5 V	10 ns

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-10 (Industrial)		Unit
				Min	Max	
V _{OH}	Output HIGH Voltage	I _{OH} = −4.0 mA		2.4	–	V
		I _{OH} = −0.1 mA		–	3.4 ^[3]	
V _{OL}	Output LOW Voltage	I _{OL} = 8.0 mA		–	0.4	V
V _{IH}	Input HIGH Voltage			2.2	V _{CC} + 0.5	V
V _{IL}	Input LOW Voltage ^[2]			−0.5	0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}		−1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled		−1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max, I _{OUT} = 0 mA, f = f _{max} = 1/t _{RC}	100 MHz	–	80	mA
			83 MHz	–	72	mA
			66 MHz	–	58	mA
			40 MHz	–	37	mA
I _{SB1}	Automatic CE Power-Down Current – TTL Inputs	Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{max}		–	10	mA
I _{SB2}	Automatic CE Power-Down Current – CMOS Inputs	Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3$ V, V _{IN} ≥ V _{CC} − 0.3 V, or V _{IN} ≤ 0.3 V, f = 0		–	3	mA

Note

2. V_{IL} (min) = -2.0 V and V_{IH} (max) = $V_{CC} + 1$ V for pulse durations of less than 5 ns.

3. Please note that the maximum V_{OH} limit does not exceed minimum CMOS V_{IH} of 3.5V. If you are interfacing this SRAM with 5 V legacy processors that require a minimum V_{IH} of 3.5 V, please refer to Application Note [AN6081](#) for technical details and options you may consider.

Capacitance

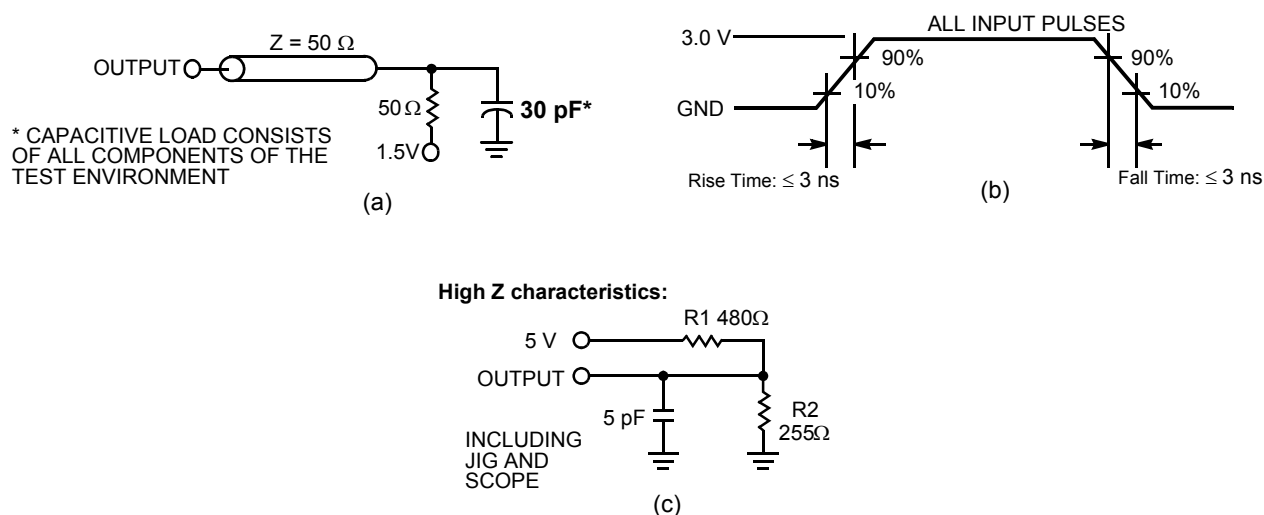
Parameter ^[4]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0 V	6	pF
C _{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter ^[4]	Description	Test Conditions	400-Mil Wide SOJ	TSOP II	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	56.29	62.22	°C/W
Θ _{JC}	Thermal resistance (junction to case)		38.14	21.43	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[5]



Notes

- Tested initially and after any design or process changes that may affect these parameters.
- AC characteristics (except High Z) are tested using the load conditions shown in Figure 2 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 2 (c).

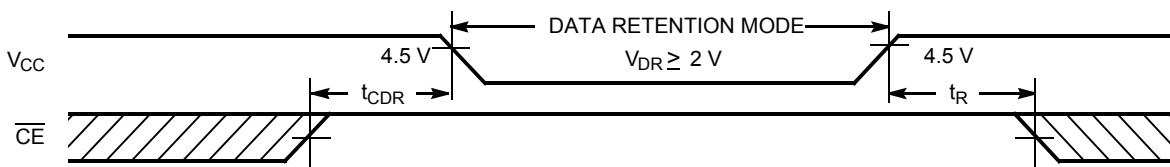
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0	–	V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0\text{ V}$, $\overline{CE} \geq V_{CC} - 0.3\text{ V}$, $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	3	mA
$t_{CDR}^{[6]}$	Chip Deselect to Data Retention Time		0	–	ns
$t_R^{[7]}$	Operation Recovery Time		t_{RC}	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

6. Tested initially and after any design or process changes that may affect these parameters.
7. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ $\geq 50\text{ }\mu\text{s}$ or stable at $V_{CC(min)}$ $\geq 50\text{ }\mu\text{s}$.

Switching Characteristics

Over the Operating Range

Parameter ^[8]	Description	-10 (Industrial)		Unit
		Min	Max	
Read Cycle				
t _{power} ^[9]	V _{CC} (typical) to the first access	100	–	μs
t _{RC}	Read Cycle Time	10	–	ns
t _{AA}	Address to Data Valid	–	10	ns
t _{OHA}	Data Hold from Address Change	3	–	ns
t _{ACE}	$\overline{\text{CE}}$ LOW to Data Valid	–	10	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to Data Valid	–	5	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to Low Z	0	–	ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to High Z ^[10, 11]	–	5	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to Low Z ^[11]	3	–	ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to High Z ^[10, 11]	–	5	ns
t _{PU} ^[12]	$\overline{\text{CE}}$ LOW to Power-Up	0	–	ns
t _{PD} ^[12]	$\overline{\text{CE}}$ HIGH to Power-Down	–	10	ns
Write Cycle ^[13, 14]				
t _{WC}	Write Cycle Time	10	–	ns
t _{SCE}	$\overline{\text{CE}}$ LOW to Write End	7	–	ns
t _{AW}	Address Set-Up to Write End	7	–	ns
t _{HA}	Address Hold from Write End	0	–	ns
t _{SA}	Address Set-Up to Write Start	0	–	ns
t _{PWE}	$\overline{\text{WE}}$ Pulse Width	7	–	ns
t _{SD}	Data Set-Up to Write End	6	–	ns
t _{HD}	Data Hold from Write End	0	–	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to Low Z ^[11]	3	–	ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to High Z ^[10, 11]	–	5	ns

Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified $I_{\text{OL}}/I_{\text{OH}}$ and 30-pF load capacitance.
9. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access can be performed.
10. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in (c) of [Figure 2 on page 5](#). Transition is measured when the outputs enter a high impedance state.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
12. This parameter is guaranteed by design and is not tested.
13. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
14. The minimum write cycle time for Write Cycle no. 3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [15, 16]

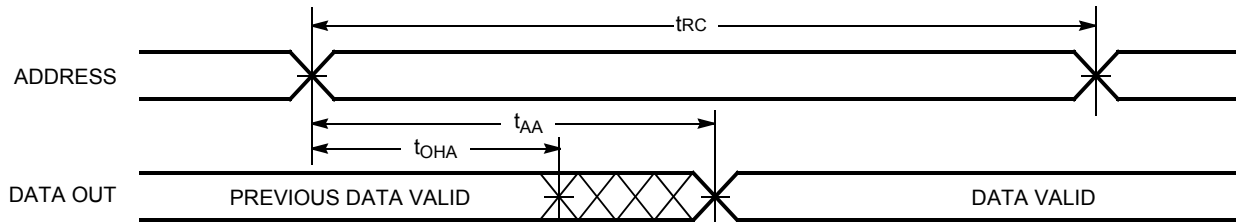
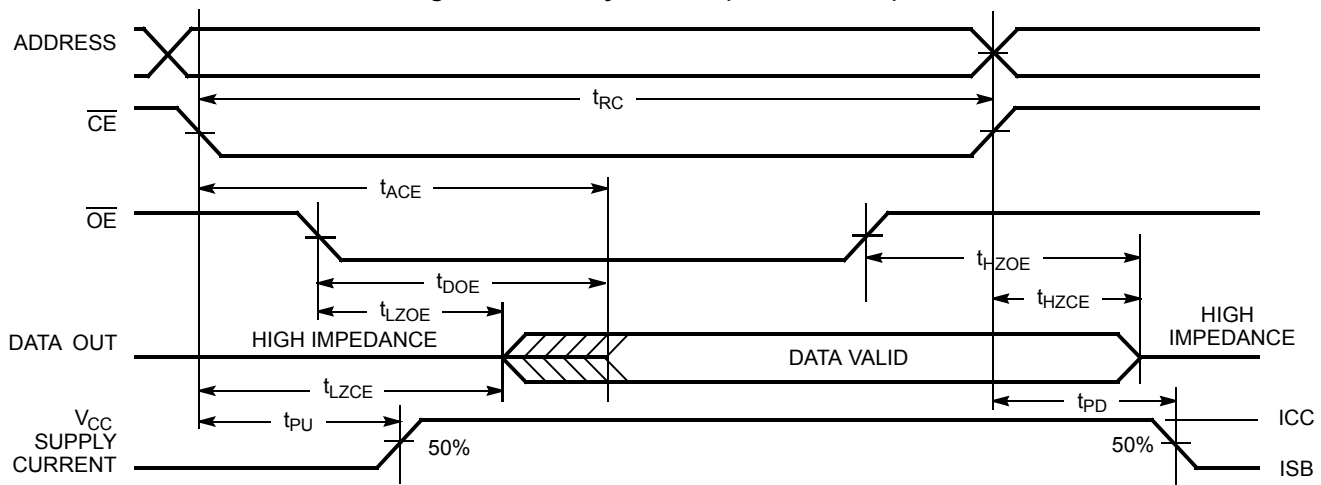


Figure 5. Read Cycle No. 2 (\overline{OE} Controlled) [16, 17]



Notes

15. Device is continuously selected. \overline{OE} , \overline{CE} = V_{IL} .
16. \overline{WE} is HIGH for Read cycle.
17. Address valid prior to or coincident with \overline{CE} transition LOW..

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [18, 19]

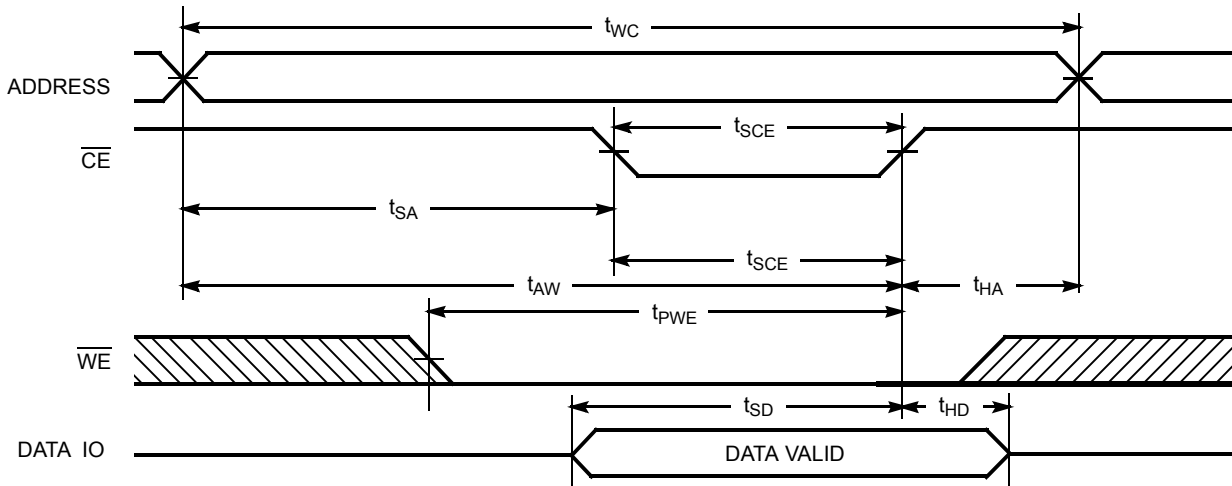
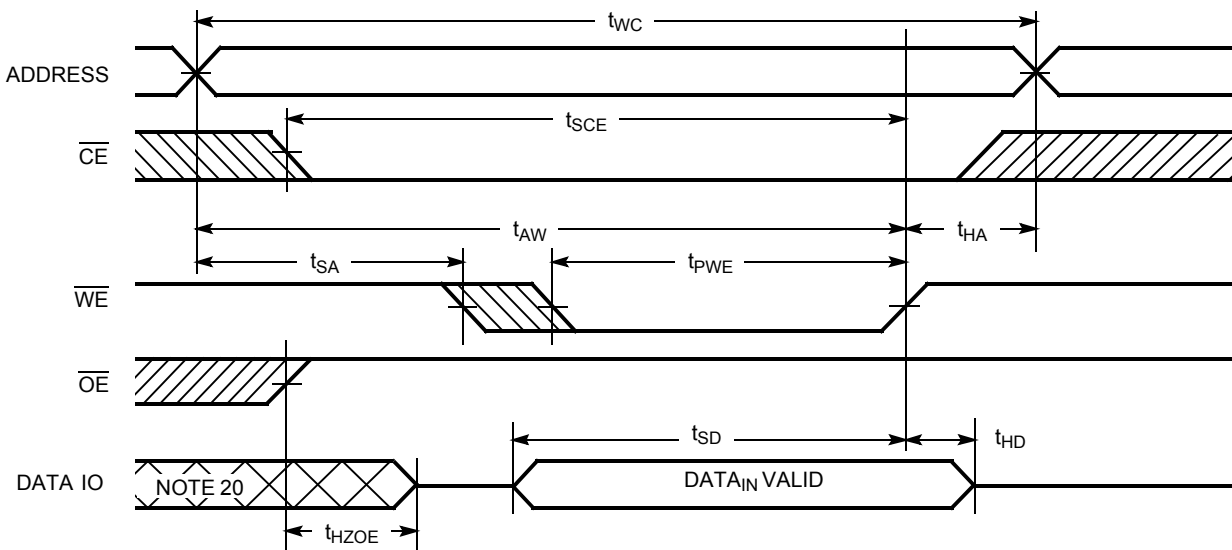


Figure 7. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write) [18, 19]

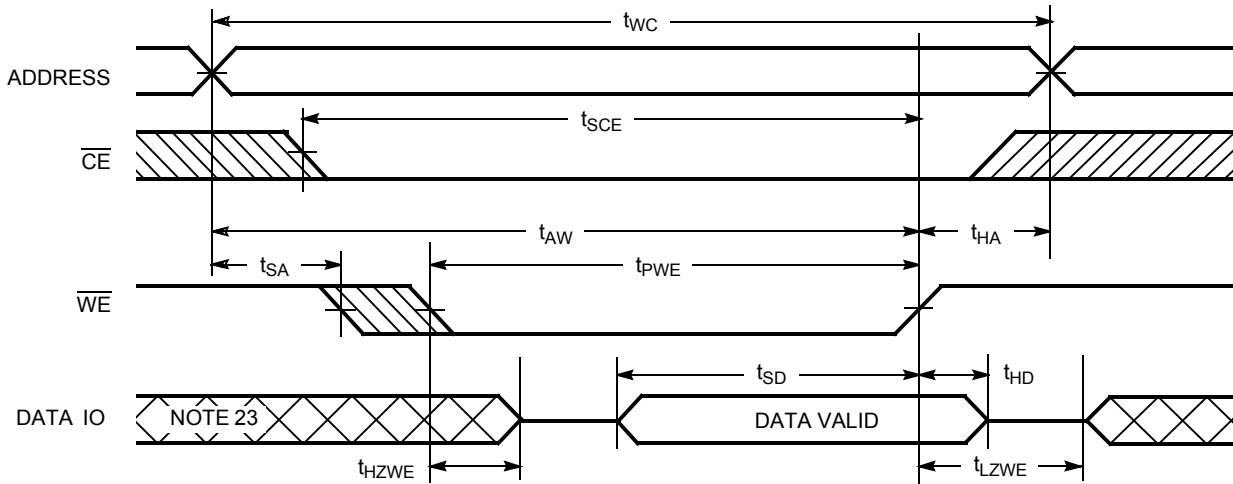


Notes

18. Data IO is high impedance if $\overline{\text{OE}} = V_{\text{IH}}$.
19. If CE goes HIGH simultaneously with WE going HIGH, the output remains in a high-impedance state.
20. During this period the IOs are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [21, 22]



Notes

21. The minimum write cycle time for Write Cycle no. 3 (\overline{WE} controlled, \overline{OE} LOW) is the sum of t_{HZWE} and t_{SD} .

22. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

23. During this period the IOs are in the output state and input signals should not be applied.

Truth Table

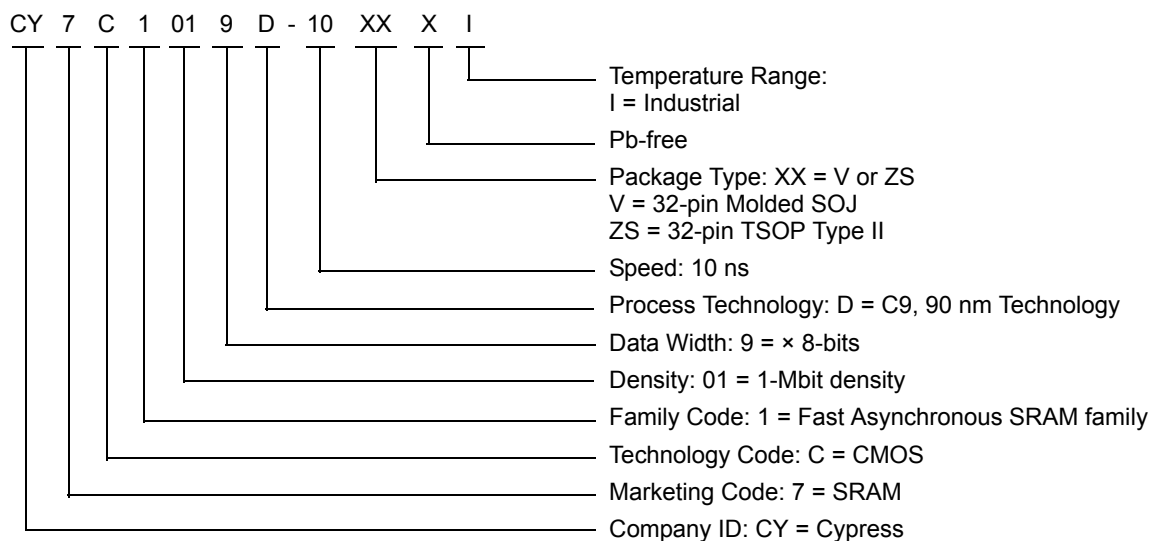
\overline{CE}	\overline{OE}	\overline{WE}	IO_0 – IO_7	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1019D-10VXI	51-85033	32-pin SOJ (400 Mils) Pb-free	Industrial
	CY7C1019D-10ZSXI	51-85095	32-pin TSOP (Type II) Pb-free	

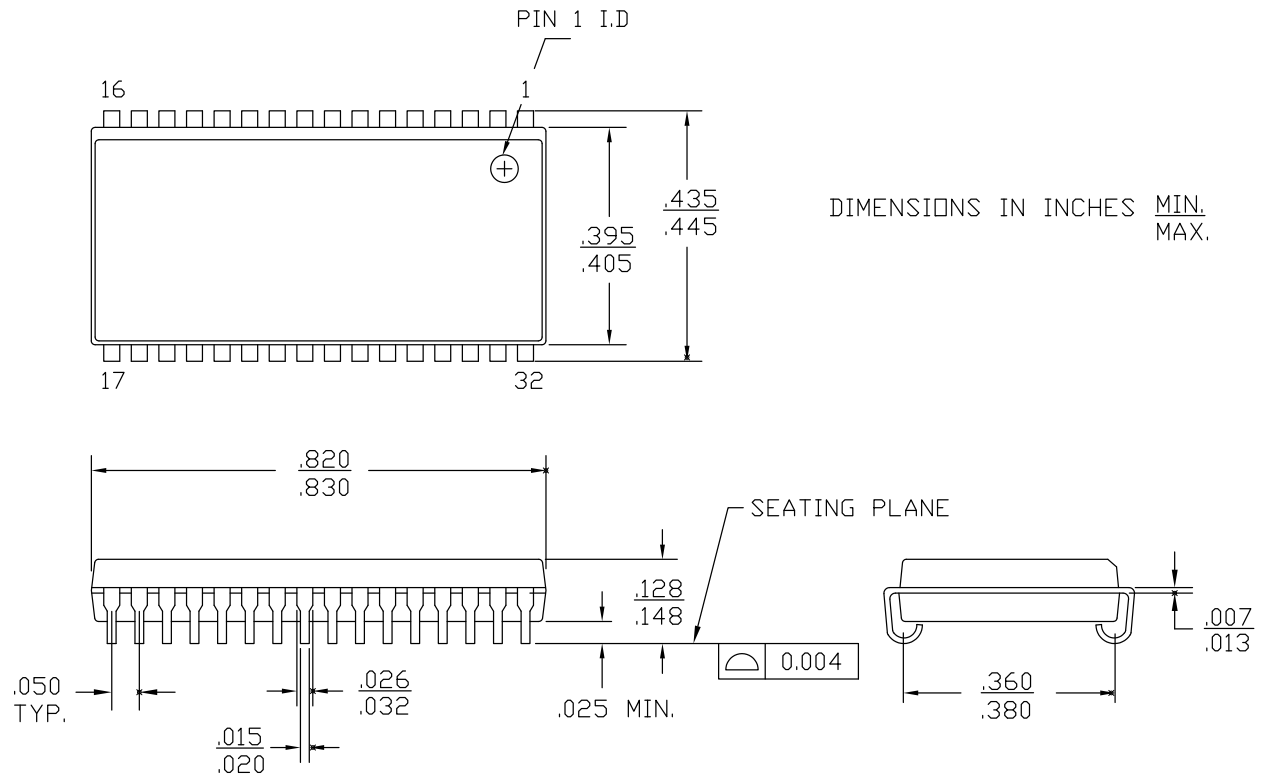
Please contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

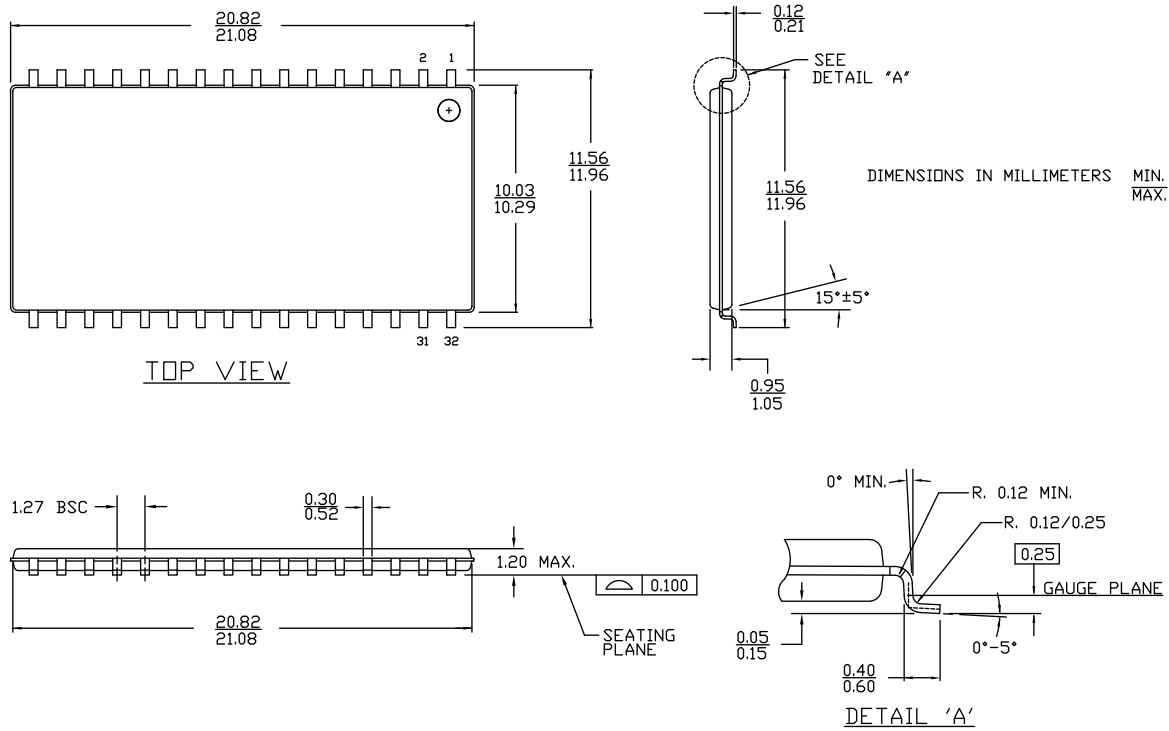
Figure 9. 32-pin SOJ (400 Mils) V32.4 (Molded SOJ V33) Package Outline, 51-85033



51-85033 *E

Package Diagrams (continued)

Figure 10. 32-pin TSOP Type II (20.95 × 11.76 × 1.0 mm) ZS32 Package Outline, 51-85095



51-85095 *B

Acronyms

Acronym	Description
$\overline{\text{CE}}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SOJ	Small Outline J-lead
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
ms	millisecond
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1019D, 1-Mbit (128 K × 8) Static RAM Document Number: 38-05464				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	201560	See ECN	SWI	Advance Information data sheet for C9 IPP
*A	233715	See ECN	RKF	DC parameters are modified as per EROS (Spec # 01-2165) Pb-free offering in the Ordering Information
*B	262950	See ECN	RKF	Added T _{power} Spec in Switching Characteristics table Added Data Retention Characteristics table and waveforms Shaded Ordering Information
*C	307598	See ECN	RKF	Reduced Speed bins to -10 and -12 ns
*D	520647	See ECN	VKN	Converted from Preliminary to Final Removed Commercial Operating range Removed 12 ns speed bin Added I _{CC} values for the frequencies 83MHz, 66MHz and 40MHz Updated Thermal Resistance table Updated Ordering Information Table Changed Overshoot spec from V _{CC} +2V to V _{CC} +1V in footnote #2
*E	802877	See ECN	VKN	Changed I _{CC} spec from 60 mA to 80 mA for 100MHz, 55 mA to 72 mA for 83MHz, 45 mA to 58 mA for 66MHz, 30 mA to 37 mA for 40MHz
*F	3110052	12/14/2010	AJU	Added Ordering Code Definitions . Updated Package Diagrams .
*G	3245896	05/02/2011	PRAS	Updated Package Diagrams . Added Acronyms and Units of Measure . Updated in new template.
*H	4038234	06/24/2013	MEMJ	Updated Functional Description . Updated Electrical Characteristics : Added one more Test Condition "I _{OH} = -0.1 mA" for V _{OH} parameter and added maximum value corresponding to that Test Condition. Added Note 3 and referred the same note in maximum value for V _{OH} parameter corresponding to Test Condition "I _{OH} = -0.1 mA". Updated in new template.
*I	4385827	05/21/2014	MEMJ	Updated Package Diagrams : spec 51-85033 – Changed revision from *D to *E. Completing Sunset Review.
*J	4579569	11/26/2014	MEMJ	Added related documentation hyperlink in page 1.

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