Pin Description for CY2309

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5V-tolerant input
2	CLKA1[2]	Buffered clock output, Bank A
3	CLKA2[2]	Buffered clock output, Bank A
4	V_{DD}	3.3V supply
5	GND	Ground
6	CLKB1[2]	Buffered clock output, Bank B
7	CLKB2[2]	Buffered clock output, Bank B
8	S2[3]	Select input, bit 2
9	S1[3]	Select input, bit 1
10	CLKB3[2]	Buffered clock output, Bank B
11	CLKB4[2]	Buffered clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3V supply
14	CLKA3[2]	Buffered clock output, Bank A
15	CLKA4[2]	Buffered clock output, Bank A
16	CLKOUT[2]	Buffered output, internal feedback on this pin

Pin Description for CY2305

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5V-tolerant input
2	CLK2[2]	Buffered clock output
3	CLK1[2]	Buffered clock output
4	GND	Ground
5	CLK3[2]	Buffered clock output
6	V_{DD}	3.3V supply
7	CLK4[2]	Buffered clock output
8	CLKOUT[2]	Buffered clock output, internal feedback on this pin

Select Input Decoding for CY2309

S2	S1	CLOCK A1–A4	CLOCK B1–B4	CLKOUT[4]	Output Source	PLL Shutdown
0	0	Three-state	Three-state	Driven	PLL	N
0	1	Driven	Three-state	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Notes:

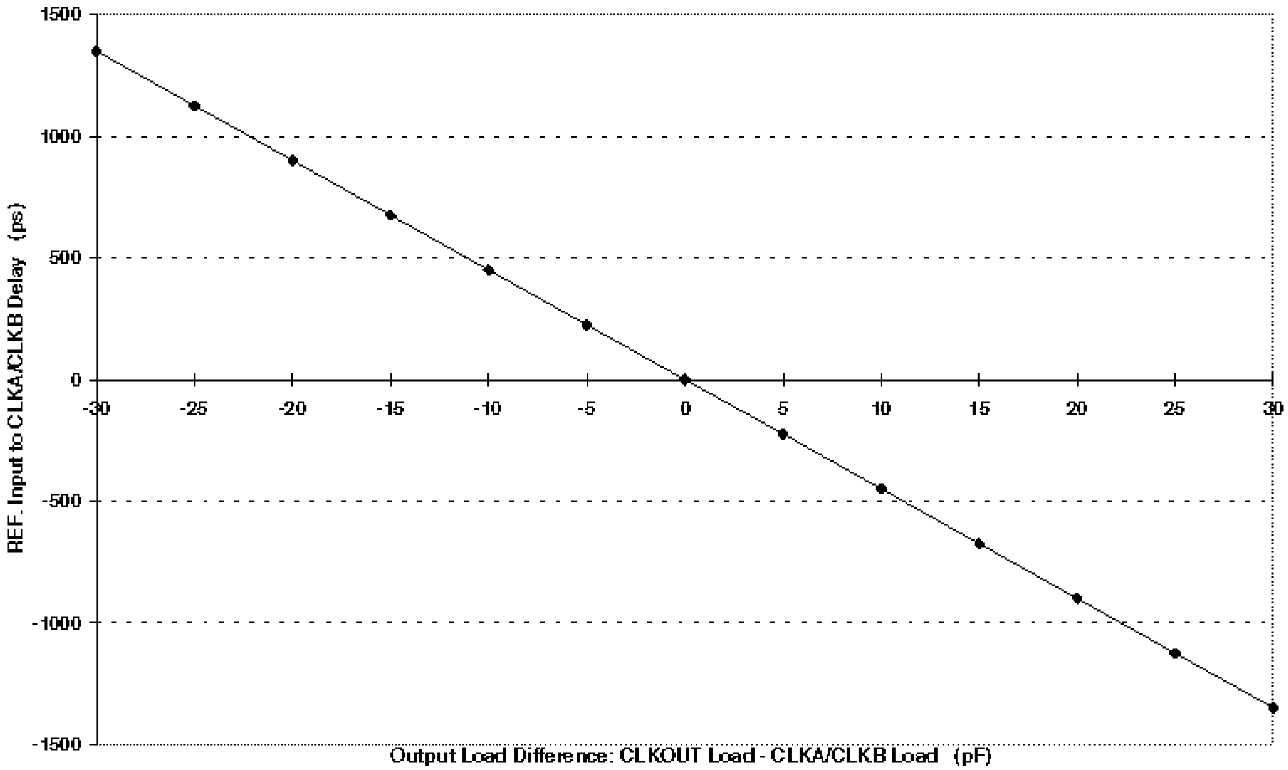
[1] Weak pull-down.

[2] Weak pull-down on all outputs.

[3] Weak pull-ups on these inputs.

[4] This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

REF. Input to CLKA/CLKB Delay vs. Loading Difference between CLKOUT and CLKA/CLKB Pins



Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between the input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay. This is shown in the above graph.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load, equal to that on other outputs, for obtaining zero input-output delay. If input to output delay adjustments are required, use the above graph to calculate loading differences between the CLKOUT pin and other outputs.

For zero output-output skew, be sure to load all outputs equally. For further information refer to the application note entitled “CY2305 and CY2309 as PCI and SDRAM Buffers.”

Absolute Maximum Conditions

Supply Voltage to Ground Potential .... –0.5V to +7.0V

DC Input Voltage (Except REF) ....–0.5V to V_{DD} + 0.5V

DC Input Voltage REF... –0.5V to 7V

Storage Temperature .... –65°C to +150°C

Junction Temperature... 150°C

Static Discharge Voltage
(per MIL-STD-883, Method 3015) .... > 2,000V

Operating Conditions for CY2305SC-XX and CY2309SC-XX Commercial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, below 100 MHz	–	30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz	–	10	pF
C_{IN}	Input Capacitance	–	7	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics for CY2305SC-XX and CY2309SC-XX Commercial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage[5]		–	0.8	V
V_{IH}	Input HIGH Voltage[5]		2.0	–	V
I_{IL}	Input LOW Current	V_{IN} = 0V	–	50.0	μA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$	–	100.0	μA
V_{OL}	Output LOW Voltage[6]	I_{OL} = 8 mA (–1) I_{OH} = 12 mA (–1H)	–	0.4	V
V_{OH}	Output HIGH Voltage[6]	I_{OH} = –8 mA (–1) I_{OL} = –12 mA (–1H)	2.4	–	V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz	–	12.0	μA
I_{DD}	Supply Current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}	–	32.0	mA

Switching Characteristics for CY2305SC-1and CY2309SC-1 Commercial Temperature Devices[7]

Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t1	Output Frequency	30-pF load 10-pF load	10 10	–	100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t3	Rise Time[6]	Measured between 0.8V and 2.0V	–	–	2.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	–	–	2.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	–	85	250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$	–	0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	–	700	ps
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67 MHz, loaded outputs	–	70	200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Notes:

5. REF input has a threshold voltage of $V_{DD}/2$.
6. Parameter is guaranteed by design and characterization. Not 100% tested in production.
7. All parameters specified with loaded outputs.

Switching Characteristics for CY2305SC-1H and CY2309SC-1H Commercial Temperature Devices[7]

Parameter	Name	Description	Min.	Typ.	Max.	Unit
t1	Output Frequency	30-pF load 10-pF load	10 10	–	100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} < 50.0 MHz	45.0	50.0	55.0	%
t3	Rise Time[6]	Measured between 0.8V and 2.0V	–	–	1.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	–	–	1.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	–	85	250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$	–	–	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	–	700	ps
t_8	Output Slew Rate[6]	Measured between 0.8V and 2.0V using Test Circuit #2	1	–		V/ns
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67 MHz, loaded outputs	–	60	200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Operating Conditions for CY2305SI-XX and CY2309SI-XX Industrial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, below 100 MHz	–	30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz	–	10	pF
C_{IN}	Input Capacitance	–	7	pF

Electrical Characteristics for CY2305SI-XX and CY2309SI-XX Industrial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage[5]		–	0.8	V
V_{IH}	Input HIGH Voltage[5]		2.0	–	V
I_{IL}	Input LOW Current	V_{IN} = 0V	–	50.0	µA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$	–	100.0	µA
V_{OL}	Output LOW Voltage[6]	I_{OL} = 8 mA (–1) I_{OH} =12 mA (–1H)	–	0.4	V
V_{OH}	Output HIGH Voltage[6]	I_{OH} = –8 mA (–1) I_{OL} = –12 mA (–1H)	2.4	–	V
I_{DD} (PD mode)	Power-down Supply Current	REF = 0 MHz	–	25.0	µA
I_{DD}	Supply Current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}	–	35.0	mA

Switching Characteristics for CY2305SI-1and CY2309SI-1 Industrial Temperature Devices [7]

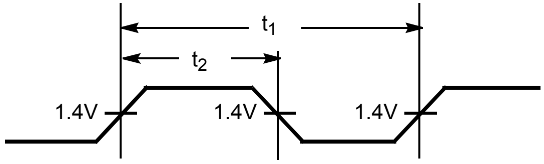
Parameter	Name	Test Conditions	Min.	Typ.	Max.	Unit
t1	Output Frequency	30-pF load 10-pF load	10 10	–	100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
t3	Rise Time[6]	Measured between 0.8V and 2.0V	–	–	2.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	–	–	2.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	–	85	250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$	–	–	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	–	700	ps
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67 MHz, loaded outputs	–	70	200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Switching Characteristics for CY2305SI-1H and CY2309SI-1H Industrial Temperature Devices[7]

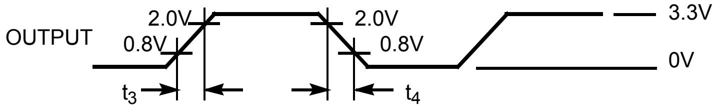
Parameter	Name	Description	Min.	Typ.	Max.	Unit
t_1	Output Frequency	30-pF load 10-pF load	10 10	–	100 133.33	MHz MHz
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} = 66.67 MHz	40.0	50.0	60.0	%
	Duty Cycle[6] = $t_2 \div t_1$	Measured at 1.4V, F_{out} < 50.0 MHz	45.0	50.0	55.0	%
t_3	Rise Time[6]	Measured between 0.8V and 2.0V	–	–	1.50	ns
t_4	Fall Time[6]	Measured between 0.8V and 2.0V	–	–	1.50	ns
t_5	Output to Output Skew[6]	All outputs equally loaded	–	85	250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$	–	–	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[6]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, CY2309 device only.	1	5	8.7	ns
t_7	Device to Device Skew[6]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices	–	–	700	ps
t_8	Output Slew Rate[6]	Measured between 0.8V and 2.0V using Test Circuit #2	1	–	–	V/ns
t_J	Cycle to Cycle Jitter[6]	Measured at 66.67 MHz, loaded outputs	–	60	200	ps
t_{LOCK}	PLL Lock Time[6]	Stable power supply, valid clock presented on REF pin	–	–	1.0	ms

Switching Waveforms

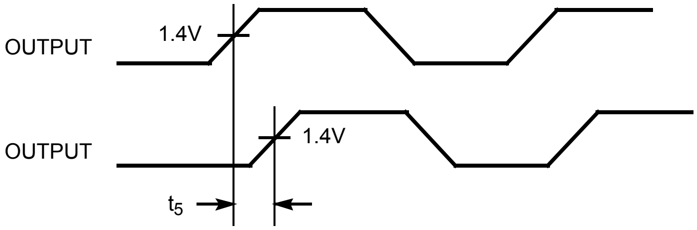
Duty Cycle Timing



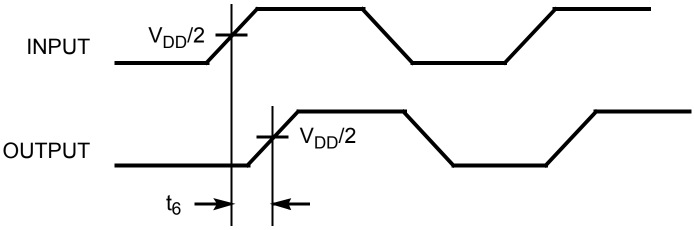
All Outputs Rise/Fall Time



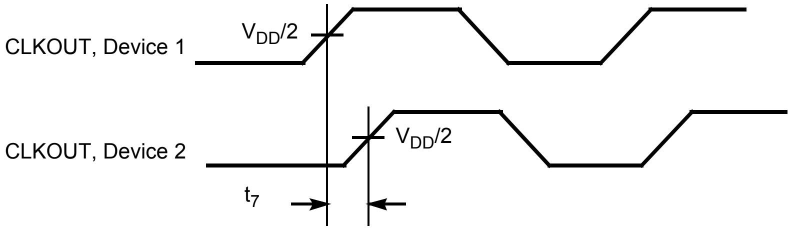
Output-Output Skew



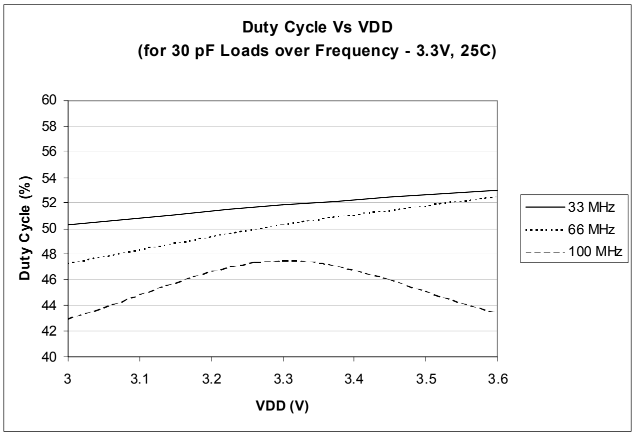
Input-Output Propagation Delay

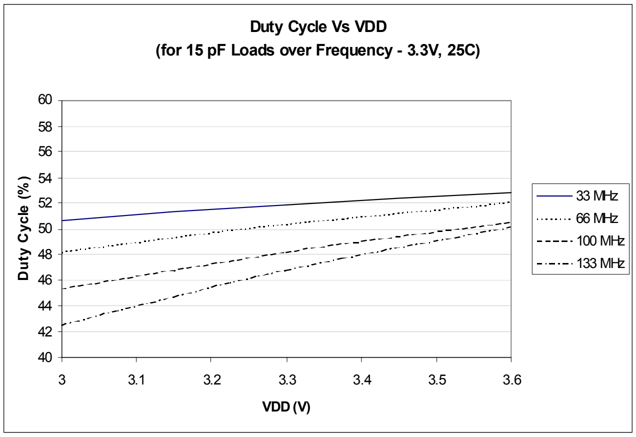


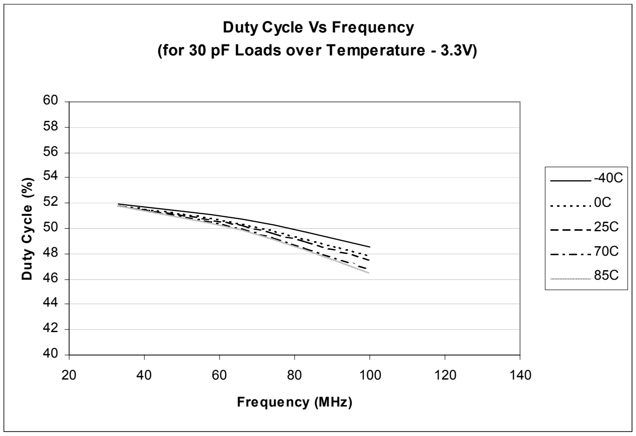
Device-Device Skew

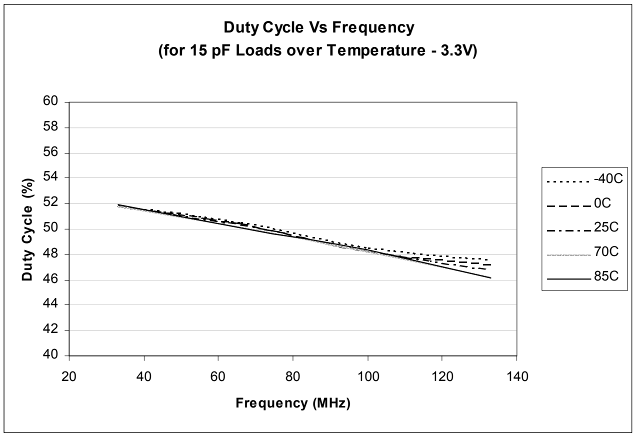


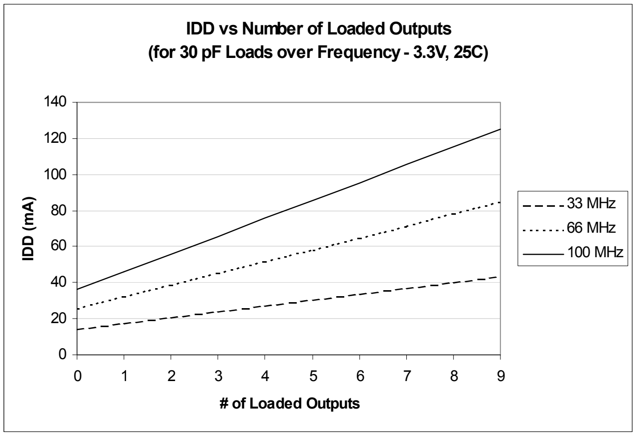
Typical Duty Cycle[8] and I_{DD} Trends[9] for CY2305-1 and CY2309-1

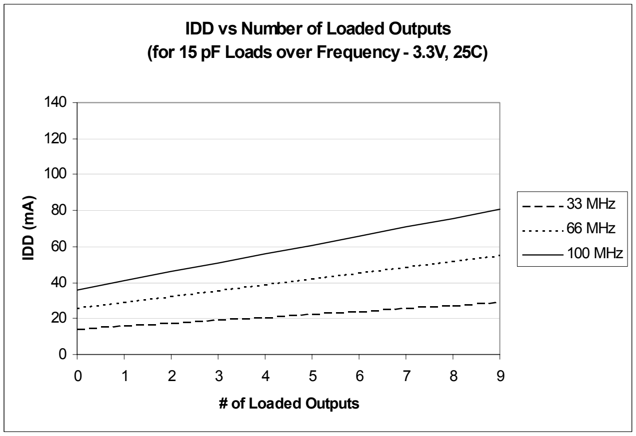








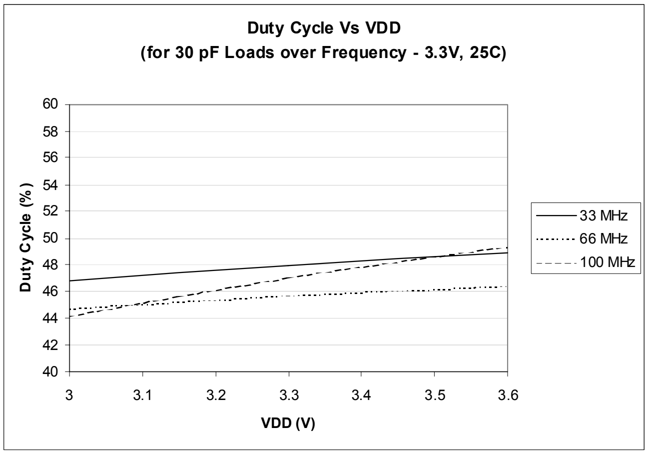


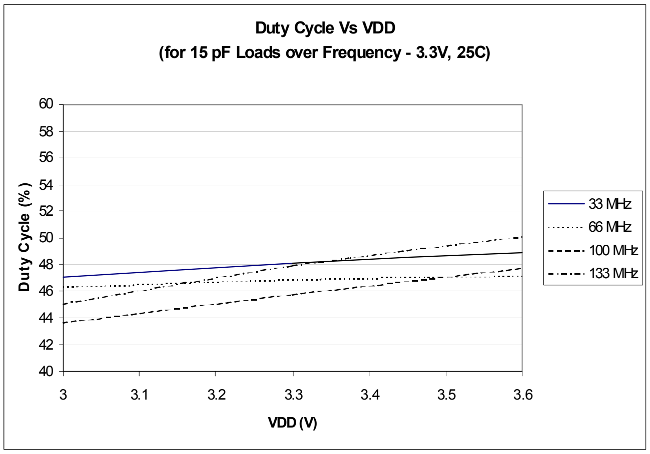


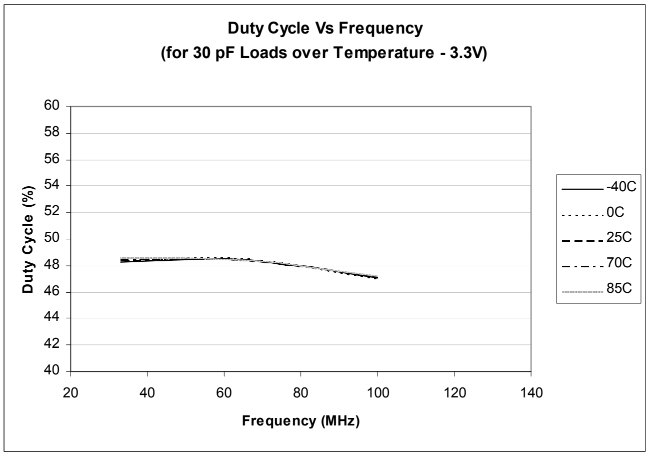
Notes:

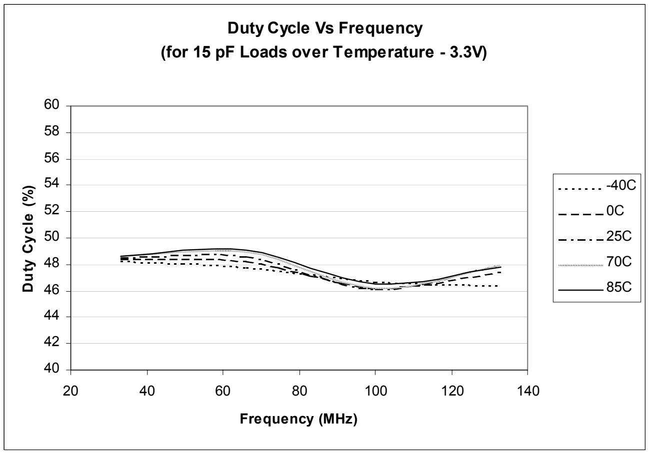
8. Duty Cycle is taken from typical chip measured at 1.4V.
9. I_{DD} data is calculated from $I_{DD} = I_{CORE} + nCVf$, where I_{CORE} is the unloaded current. (n = # of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = frequency (Hz)).

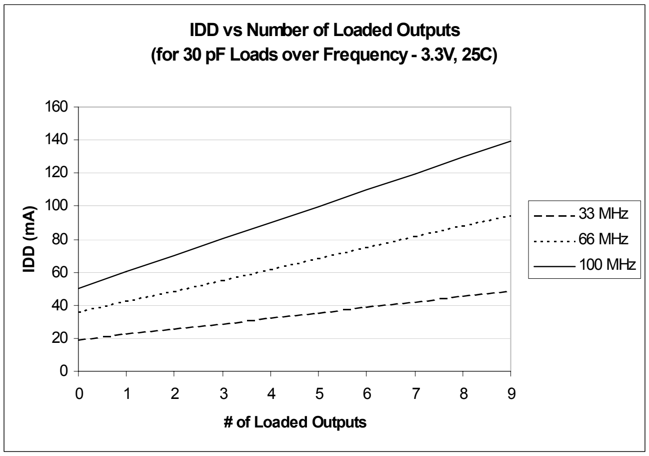
Typical Duty Cycle[8] and IDD Trends[9] for CY2305-1H and CY2309-1H

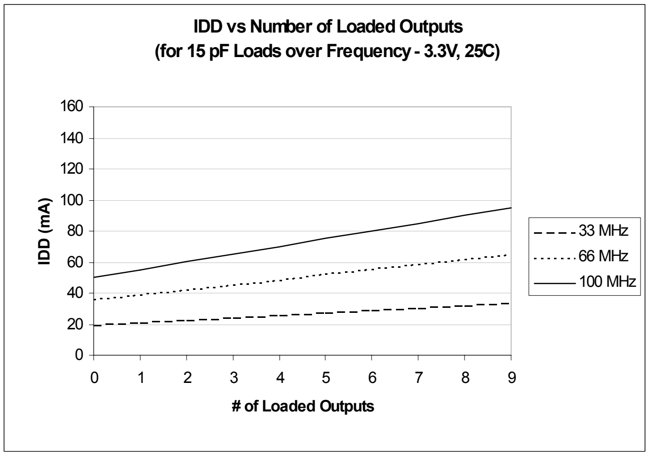






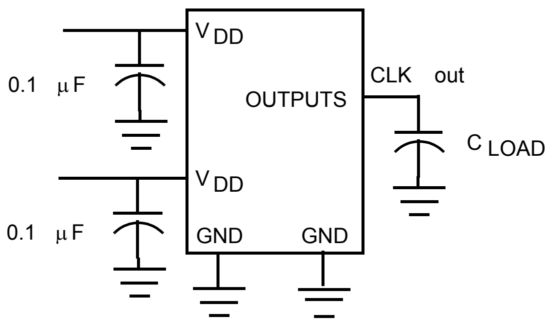




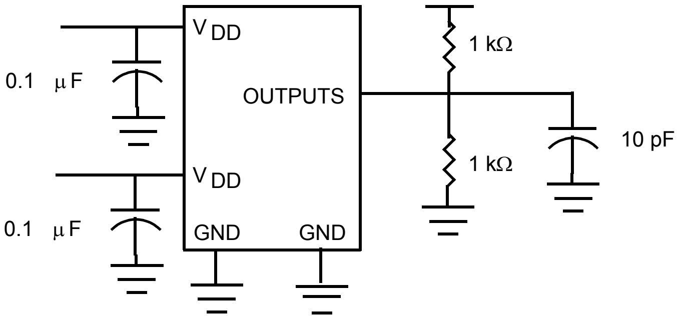


Test Circuits

Test Circuit # 1



Test Circuit # 2



For parameter t_8 (output slew rate) on -1H devices

Ordering Information

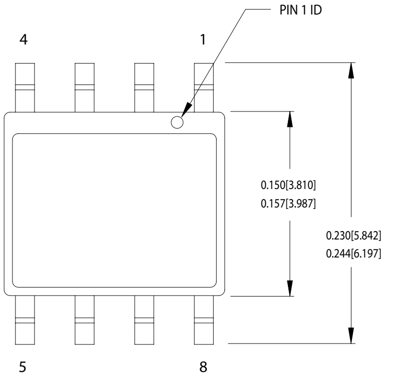
Ordering Code	Package Type	Operating Range
CY2305SC-1	8-pin 150-mil SOIC	Commercial
CY2305SC-1T	8-pin 150-mil SOIC – Tape and Reel	Commercial
CY2305SZC-1	8-pin 150-mil SOIC – (Lead-free)	Commercial
CY2305SZC-1T	8-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Commercial
CY2305SXC-1	8-pin 150-mil SOIC – (Lead-free)	Commercial
CY2305SXC-1T	8-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Commercial
CY2305SI-1	8-pin 150-mil SOIC	Industrial
CY2305SI-1T	8-pin 150-mil SOIC – Tape and Reel	Industrial
CY2305SZI-1	8-pin 150-mil SOIC – (Lead-free)	Industrial
CY2305SZI-1T	8-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Industrial
CY2305SXI-1	8-pin 150-mil SOIC – (Lead-free)	Industrial
CY2305SXI-1T	8-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Industrial
CY2305SC-1H	8-pin 150-mil SOIC	Commercial
CY2305SC-1HT	8-pin 150-mil SOIC – Tape and Reel	Commercial
CY2305SZC-1H	8-pin 150-mil SOIC – (Lead-free)	Commercial
CY2305SZC-1HT	8-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Commercial
CY2305SXC-1H	8-pin 150-mil SOIC – (Lead-free)	Commercial
CY2305SXC-1HT	8-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Commercial
CY2305SI-1H	8-pin 150-mil SOIC	Industrial
CY2305SI-1HT	8-pin 150-mil SOIC – Tape and Reel	Industrial
CY2305SZI-1H	8-pin 150-mil SOIC – (Lead-free)	Industrial
CY2305SZI-1HT	8-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Industrial
CY2305SXI-1H	8-pin 150-mil SOIC – (Lead-free)	Industrial
CY2305SXI-1HT	8-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Industrial
CY2309SC-1	16-pin 150-mil SOIC	Commercial
CY2309SC-1T	16-pin 150-mil SOIC – Tape and Reel	Commercial
CY2309SZC-1	16-pin 150-mil SOIC – (Lead-free)	Commercial
CY2309SZC-1T	16-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Commercial
CY2309SXC-1	16-pin 150-mil SOIC – (Lead-free)	Commercial
CY2309SXC-1T	16-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Commercial

Ordering Information (continued)

Ordering Code	Package Type	Operating Range
CY2309SI-1	16-pin 150-mil SOIC	Industrial
CY2309SI-1	16-pin 150-mil SOIC	Industrial
CY2309SI-1T	16-pin 150-mil SOIC – Tape and Reel	Industrial
CY2309SZI-1	16-pin 150-mil SOIC – (Lead-free)	Industrial
CY2309SZI-1T	16-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Industrial
CY2309SXI-1	16-pin 150-mil SOIC – (Lead-free)	Industrial
CY2309SXI-1T	16-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Industrial
CY2309SC-1H	16-pin 150-mil SOIC	Commercial
CY2309SC-1HT	16-pin 150-mil SOIC – Tape and Reel	Commercial
CY2309SZC-1H	16-pin 150-mil SOIC – (Lead-free)	Commercial
CY2309SZC-1HT	16-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Commercial
CY2309SXC-1H	16-pin 150-mil SOIC – (Lead-free)	Commercial
CY2309SXC-1HT	16-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Commercial
CY2309SI-1H	16-pin 150-mil SOIC	Industrial
CY2309SI-1HT	16-pin 150-mil SOIC – Tape and Reel	Industrial
CY2309SZI-1H	16-pin 150-mil SOIC – (Lead-free)	Industrial
CY2309SZI-1HT	16-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Industrial
CY2309SXI-1H	16-pin 150-mil SOIC – (Lead-free)	Industrial
CY2309SXI-1HT	16-pin 150-mil SOIC – Tape and Reel – (Lead-free)	Industrial
CY2309ZC-1H	16-pin 4.4-mm TSSOP	Commercial
CY2309ZC-1HT	16-pin 4.4-mm TSSOP – Tape and Reel	Commercial
CY2309ZXC-1H	16-pin 4.4-mm TSSOP – (Lead-free)	Commercial
CY2309ZXC-1HT	16-pin 4.4-mm TSSOP – Tape and Reel – (Lead-free)	Commercial
CY2309ZZC-1H	16-pin 4.4-mm TSSOP – (Lead-free)	Commercial
CY2309ZZC-1HT	16-pin 4.4-mm TSSOP – Tape and Reel – (Lead-free)	Commercial
CY2309ZI-1H	16-pin 4.4-mm TSSOP	Industrial
CY2309ZI-1HT	16-pin 4.4-mm TSSOP – Tape and Reel	Industrial
CY2309ZXI-1H	16-pin 4.4-mm TSSOP – (Lead-free)	Industrial
CY2309ZXI-1HT	16-pin 4.4-mm TSSOP – Tape and Reel – (Lead-free)	Industrial
CY2309ZZI-1H	16-pin 4.4-mm TSSOP – (Lead-free)	Industrial
CY2309ZZI-1HT	16-pin 4.4-mm TSSOP – Tape and Reel – (Lead-free)	Industrial

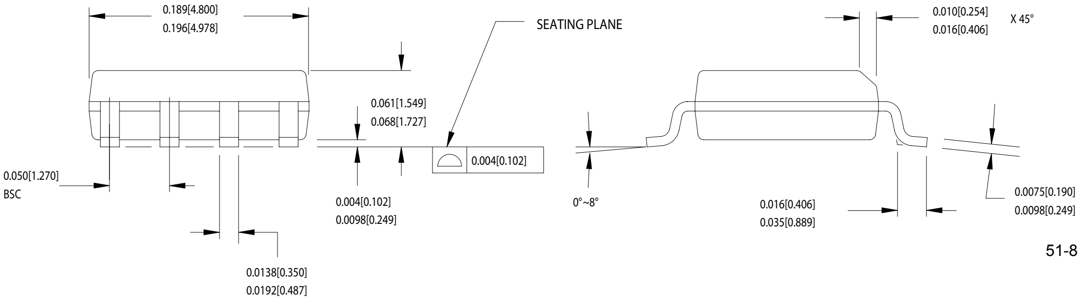
Package Drawing and Dimensions

8-lead (150-Mil) SOIC S8



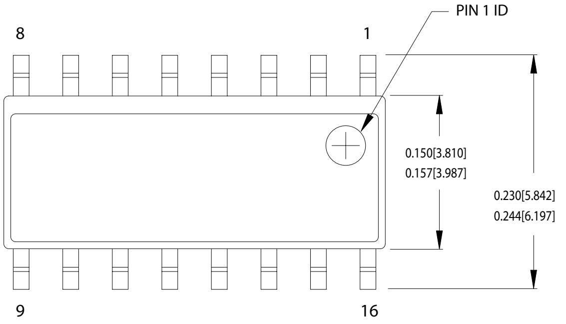
1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #
S08.15 STANDARD PKG.
SZ08.15 LEAD FREE PKG.



51-85066-*C

16-Lead (150-Mil) SOIC S16

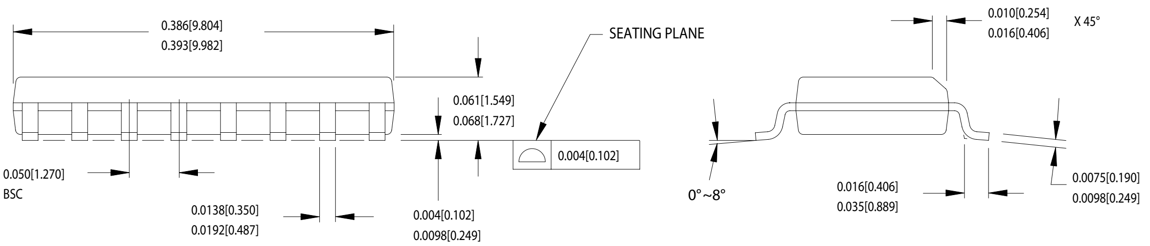


DIMENSIONS IN INCHES[MM] MIN.
MAX.

REFERENCE JEDEC MS-012

PACKAGE WEIGHT 0.15gms

PART #
S16.15 STANDARD PKG.
SZ16.15 LEAD FREE PKG.

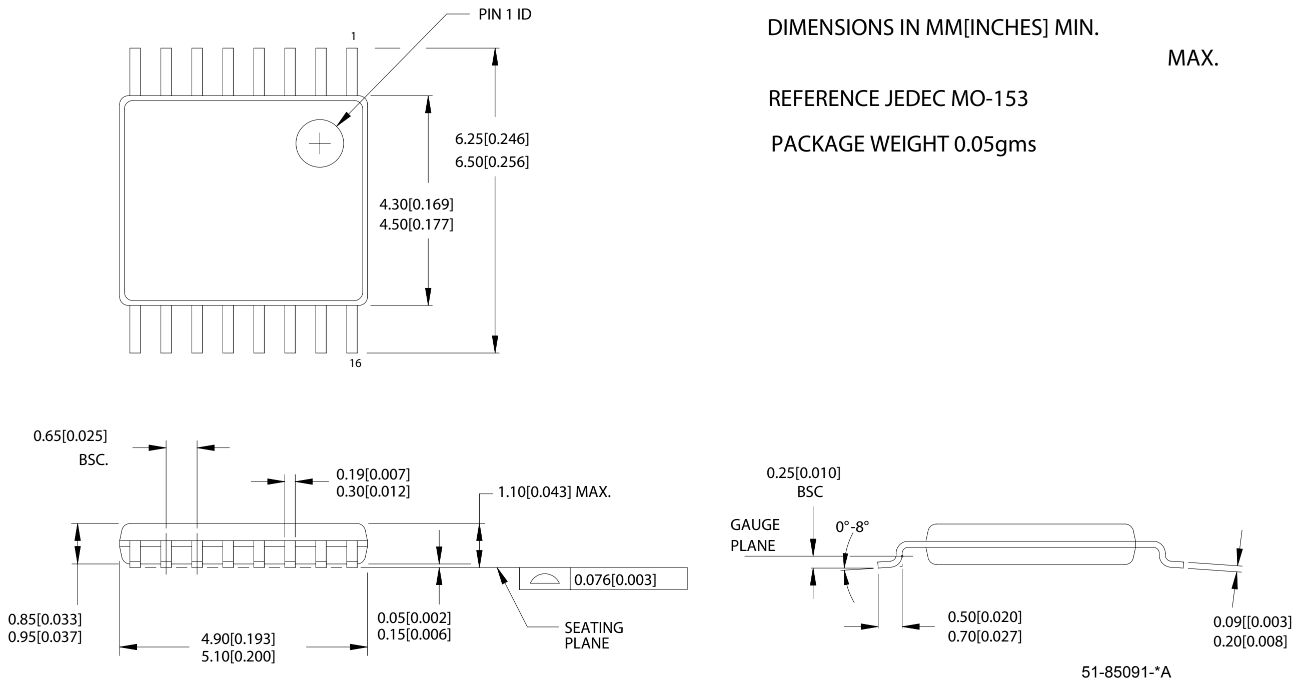


51-85068-*B

[+] Feedback

Package Drawing and Dimensions (continued)

16-lead TSSOP 4.40 MM Body Z16.173



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Document History Page

Document Title: CY2305/CY2309 Low-Cost 3.3V Zero Delay Buffer **Document Number: 38-07140**				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110249	10/19/01	SZV	Change from Spec number: 38-00530 to 38-07140
*A	111117	03/01/02	CKN	Added t6B row to the Switching Characteristics Table; also added the letter “A” to the t6A row Corrected the table title from CY2305SC-IH and CY2309SC-IH to CY2305SI-IH and CY2309SI-IH
*B	117625	10/21/02	HWT	Added eight-pin TSSOP packages (CY2305ZC-1 and CY2305ZC-1T) to the ordering information table. Added the Tape and Reel option to all the existing packages: CY2305SC-1T, CY2305SI-1T, CY2305SC-1HT, CY2305SI-1HT, CY2305ZC-1T, CY2309SC-1T, CY2309SI-1T, CY2309SC-1HT, CY2309SI-1HT, CY2309ZC-1HT, CY2309ZI-1HT
*C	121828	12/14/02	RBI	Power-up requirements added to Operating Conditions information
*D	131503	12/12/03	RGL	Added Lead-free for all the devices in the ordering information table
*E	214083	See ECN	RGL	Added a Lead-free with the new coding for all SOIC devices in the ordering information table
*F	291099	See ECN	RGL	Added TSSOP Lead-free devices
*G	390582	See ECN	RGL	Added typical values for jitter