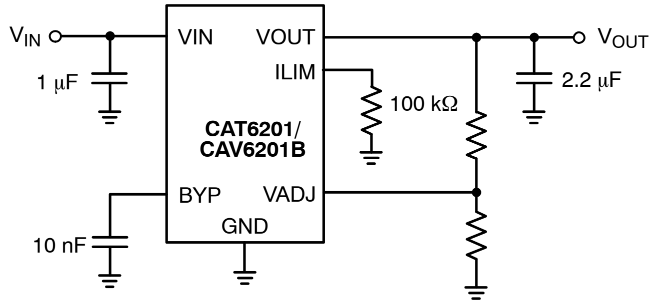


Figure 1. CAT6201/CAV6201B Typical Application

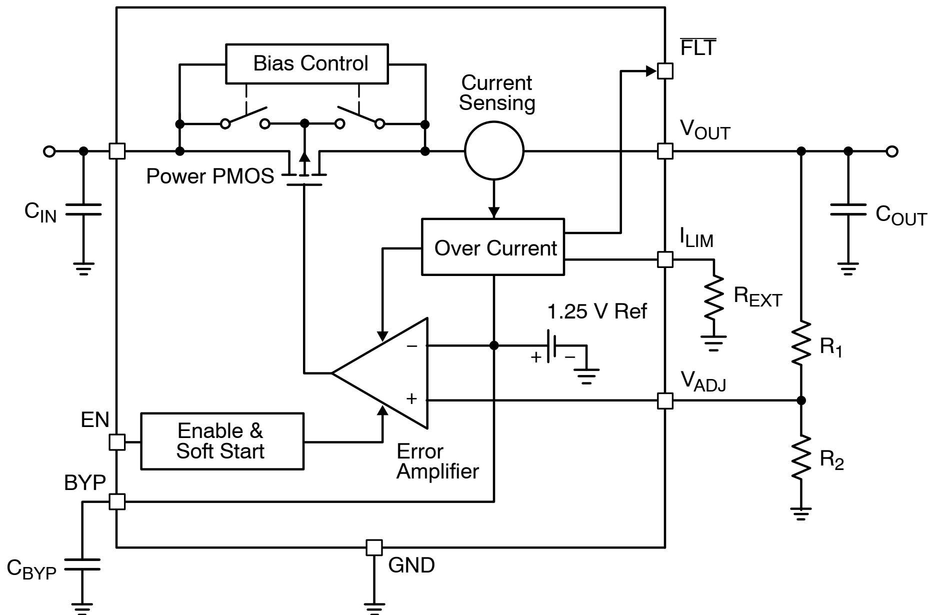


Figure 2. CAT6201/CAV6201B Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	VIN	Supply voltage input
2	$\overline{FLT}$	Fault indicator (active low)
3	EN	Enable input (active high)
4	BYP	A capacitor between BYP and GND controls the regulator's turn−on speed and improves PSRR
5	GND	Ground reference
6	ILIM	Current limit control pin
7	VADJ	Output voltage adjustment
8	VOUT	LDO Output Voltage
Pad	–	Backside pad in center of package provides thermal contact for cooling, typically via the PCB ground plane. This pad is electrically active and connected to GND internally. An external Ground connection is not required and the pad may be left floating.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
V_{IN}, V_{OUT}, EN	0 to 16	V
All other pins	−0.3 to +6.0	V
Junction Temperature, T_J	+150	°C
Power Dissipation, P_D	Internally Limited (Note 1)	mW
Storage Temperature Range, T_S	−65 to +150	°C
Lead Temperature (soldering, 5 sec.)	260	°C
ESD Rating (Human Body Model)	1000	V
ESD Rating (Machine Model)	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The maximum allowable power dissipation at any T_A (ambient temperature) is $P_{Dmax} = (T_{Jmax} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.

Table 3. RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter	Range	Unit
V_{IN}, V_{OUT}, EN	3.3 to 13.5	V
All other pins	0 to 6.0	V
Junction Temperature Range, T_J	−40 to +125	°C
Package Thermal Resistance (SOIC), θ_{JA}	235	°C/W
Package Thermal Resistance (TDFN), θ_{JA}	92	°C/W

2. The device is not guaranteed to work outside its operating rating.

Pin Function

VIN is the supply pin for both the LDO's operation and the load the LDO is driving. It is recommended that a 1 μF ceramic bypass capacitor be placed between the V_{IN} pin and ground in close proximity to the device. When using longer connections to the power supply, C_{IN} value can be increased without limit. The operating input voltage range is from 3.3 V to 13.5 V.

$\overline{\text{FLT}}$ is an active low open−drain output indicating one of 3 fault conditions:

1. Input under−voltage: input is below the intended output voltage
2. Over−current. Brief over−current events are masked by a 3 ms time delay. CAT6201/CAV6201B will limit current anytime the load tries to draw more than the maximum allowed, however reporting of this event will occur only if the event lasts longer than the delay timer. Events terminating before the timer reaches its full count are ignored and the timer is reset.
3. Over−temperature shutdown has occurred.

EN is an active HIGH logic level input for switching the regulator's output between ON and OFF. A weak internal pull down assures that if EN pin is left open, the circuit is disabled.

BYP controls the soft−start feature for the regulator. When large capacitive loads are present at the regulator's output, enabling the regulator will produce large current surges on the V_{IN} supply line. To reduce these surges the regulator can be turned on gently by connecting a capacitor between the BYP pin and ground. The larger the capacitance value the more slowly V_{OUT} approaches its programmed value. The table below gives a list of common capacitor values and their resulting turn−on times. If the soft−start feature is not desired, this pin should be left floating.

Capacitance [nF]	t_{ON} [ms]
0	0.2
10	1
100	10

GND is the ground reference for the LDO in the TDFN package, center metal pad is internally connected to GND. If electrical contact is made with this pad, it should be to GND and/or the ground plane of the PCB. Connection to the ground plane enhances thermal conductivity drawing heat out of the package and into the surrounding PCB.

ILIM stands for Current Limit and is the control input for setting the point at which the current limit is invoked. I_{LIM} is defined as the current at which V_{OUT} is still within 80% of its nominal value and should not be confused with I_{SC}, the short circuit current, measured at V_{OUT} = 0 V, which is typically 100 mA greater than I_{LIM}.

A resistor R_{EXT} placed between I_{LIM} and GND selects the trip current according to a formula:

$$I_{LIM} = I_{LIM0} + \frac{\text{Current\_Limit\_Factor(CLF)}}{R_{EXT}} \qquad \text{(eq. 1)}$$

I_{LIM0} is the built−in minimum current limit (typically 150 mA), and CLF is a numerical value (typical 30,000 Volts) which relates the allowable load current to a resistance value. The value of this resistor is determined by the following equation:

$$R_{EXT}(\Omega) = \frac{CLF(V)}{I_{LIM}(A) - I_{LIM0}(A)} \qquad \text{(eq. 2)}$$

It is recommended that I_{LIM} be set to at least 50% higher than the maximum intended continuous I_{OUT}.

Example: Set I_{LIMIT} = 600 mA

$$R_{EXT}(\Omega) = \frac{30,000\ V}{0.6\ A - 0.15\ A} = 68\ K\Omega \qquad \text{(eq. 3)}$$

VADJ is the output voltage control pin. A resistor divider placed between VOUT and GND whose center point connects to VADJ sets the LDO regulator's output voltage. Typical VADJ value is 1.25 V. The current through the resistor divider can be anywhere between 10 μA and 1 mA. The higher this current is, the lower the noise.

For best performance R1 and R2 should have similar temperature coefficients, otherwise output voltage accuracy will be compromised.

$$V_{OUT} = V_{ADJ}\left(1 + \frac{R_1}{R_2}\right) \qquad \text{(eq. 4)}$$

VOUT is the LDO regulator output. A small 2.2 μF ceramic bypass capacitor is required between VOUT and ground. For better transient response, its value can be increased to 4.7 μF. This capacitor should be located near the device.

VOUT is protected against short circuits and over−temp operation by internal circuitry. In the event of an over−current, the LDO behaves like a current source, limiting current at the output. The maximum current allowed is set by R_{EXT}, the resistor between I_{LIM} and GND. If the load attempts to draw more than the allowed current, VOUT and IOUT decrease together and thus limit the total power delivered.

VOUT is protected against the application of voltages greater than VIN. For example, in automotive applications, if CAT6201/CAV6201B is powering a remote load and damage occurs to a wiring harness shorting a powered line, Battery + for instance, to VOUT, CAT6201/CAV6201B will not be damaged by this higher voltage being applied to VOUT.

Table 4. ELECTRICAL CHARACTERISTICS
(V_{IN} = V_{OUT} + 1 V, V_{EN} = High, I_{OUT} = 1 mA, C_{IN} = 1 μF, C_{OUT} = 2.2 μF, R_{EXT} = 68 kΩ, ambient temperature of 25°C (over recommended operating conditions unless specified otherwise). **Bold numbers** apply for the entire junction temperature range.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage		**3.3**		**13.5**	V
V_{OUT}	Output Voltage		**V_{ADJ}**		**12.5**	
V_{ADJ}	ADJ Voltage		1.232	1.250	1.268	V
I_{ADJ}	ADJ Input Current			0.5	**2.0**	μA
TC_{OUT}	Output Voltage Temp. Coefficient	I_{OUT} = 10 mA		100		ppm/°C
V_{R-LINE}	Line Regulation	V_{OUT} + 1 V < V_{IN} < 13.5 V	−0.2	±0.1	+0.2	%/V
			−0.4		**+0.4**	
V_{R-LOAD}	Load Regulation	I_{OUT} = 1 mA to 300 mA		0.7	**2**	%
V_{DROP}	Dropout Voltage (Note 3)	I_{OUT} = 300 mA		250	**350**	mV
I_{GND}	Ground Current	I_{OUT} = 0 mA		100	**150**	μA
		I_{OUT} = 300 mA		160	**300**	
I_{GND-SD}	Shutdown Ground Current	V_{EN} < 0.4 V		0.5	**2**	μA
PSRR	Power Supply Rejection Ratio	f = 1 kHz, C_{BYP} = 10 nF		62		dB
		f = 20 kHz, C_{BYP} = 10 nF		52		
T_{ON}	Turn−On Time	C_{BYP} = 10 nF V_{OUT} = 0% − 100%		700		μs
I_{SC}	Output short circuit current	V_{OUT} < 0.8 V R_{EXT} = 68 K	500	650	800	mA
		V_{OUT} < 0.8 V I_{LIM} = OPEN		200		
I_{LIM}	Output current limit	V_{OUT} = 80% of V_{OUT} measured at a load of 1 mA R_{EXT} = 68 K	400	450	600	mA
		V_{OUT} = 80% of V_{OUT} measured at a load of 1 mA I_{LIM} = OPEN	120	150	180	
CLF	Current Limit Factor	V_{OUT} < 0.8 V	**24**	30	**36**	KV
t_{FD}	Fault Delay		1.5	3	6	ms
$V_{IN-UVLO}$	Under voltage lockout threshold		**2.85**	3.1	**3.25**	V
ESR	R_{OUT} equivalent series resistance		5		500	mΩ
ENABLE INPUT						
V_{HI}	Logic High Level	V_{IN} = 3.3 to 13.5 V	**2**			V
V_{LO}	Logic Low Level	V_{IN} = 3.3 to 13.5 V			**0.4**	V
I_{EN}	Enable Input Current	V_{EN} = 0.4 V		0.15	1	μA
		V_{EN} = V_{IN}		3	5	
THERMAL PROTECTION						
T_{SD}	Thermal Shutdown			140		°C
T_{HYS}	Thermal Hysteresis			10		°C

3. Dropout voltage is defined as the input−to−output differential at which the output voltage drops 2% below its nominal value. During test, the input voltage stays always above the minimum 3.3 V. The given values are for V_{OUT} = 7.5 V.

TYPICAL CHARACTERISTICS (shown for 7.5 V output)

(V_{IN} = 8.5 V, R_1 = 5.1 kΩ, R_2 = 1 kΩ, C_{IN} = 1 μF, C_{OUT} = 2.2 μF, C_{BYP} = 10 nF, R_{EXT} = 68 kΩ, $\overline{FLT}$ not connected, T_A = 25°C unless otherwise specified.)

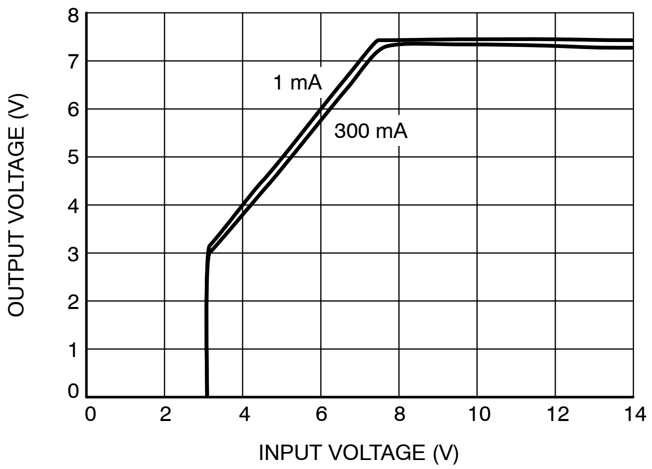


Figure 3. Dropout Characteristics

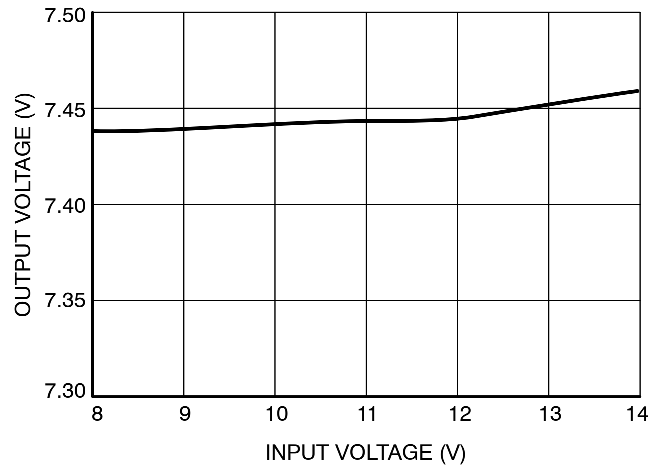


Figure 4. Line Regulation

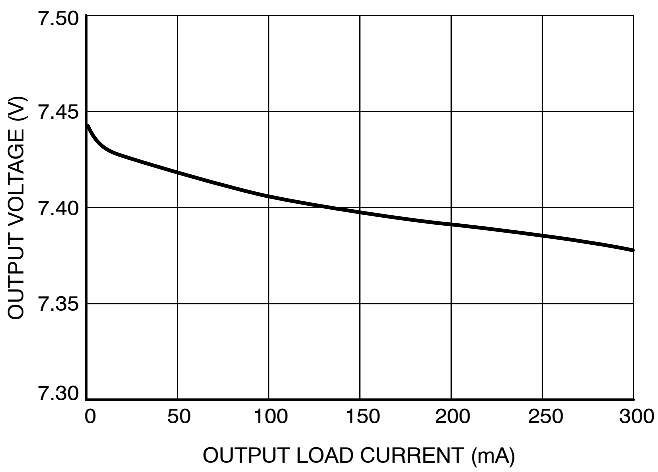


Figure 5. Load Regulation

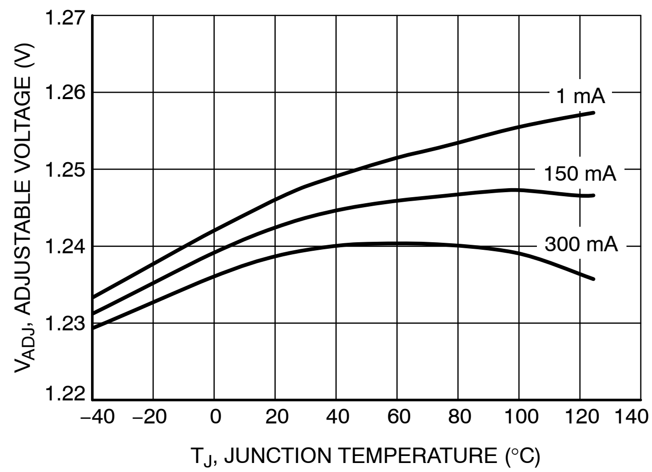


Figure 6. Adjustable Voltage vs. Temperature

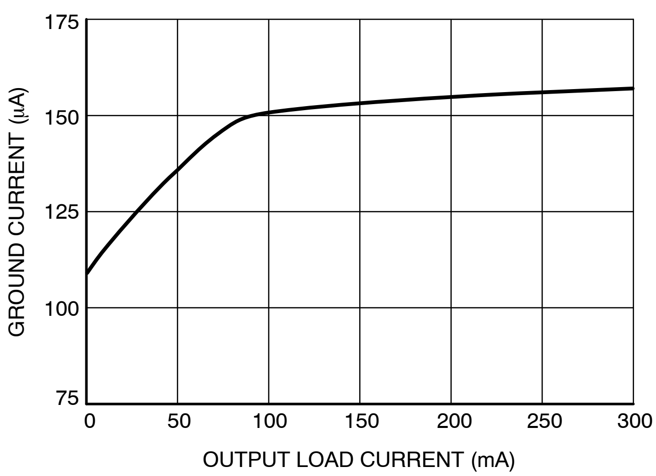


Figure 7. Ground Current vs. Load Current

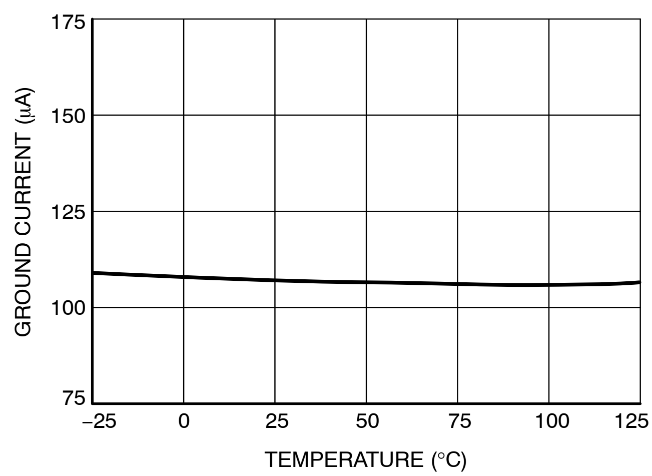


Figure 8. Ground Current vs. Temperature

TYPICAL CHARACTERISTICS (shown for 7.5 V output)

(V_{IN} = 8.5 V, R_1 = 5.1 kΩ, R_2 = 1 kΩ, C_{IN} = 1 μF, C_{OUT} = 2.2 μF, C_{BYP} = 10 nF, R_{EXT} = 68 kΩ, $\overline{FLT}$ not connected, T_A = 25°C unless otherwise specified.)

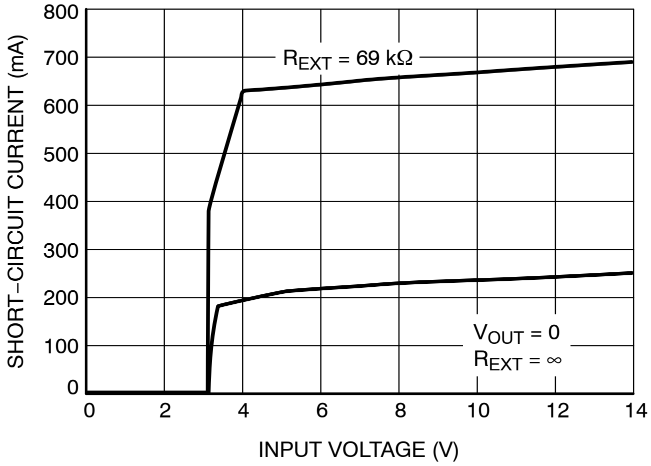


Figure 9. Output Short−circuit Current vs. Input Voltage

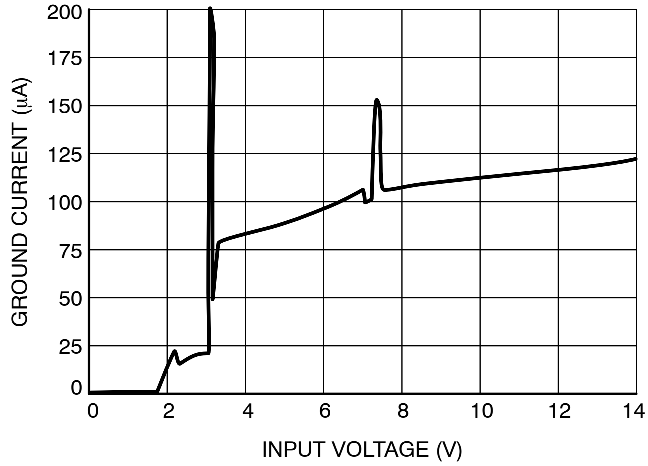


Figure 10. Ground Current vs. Input Voltage

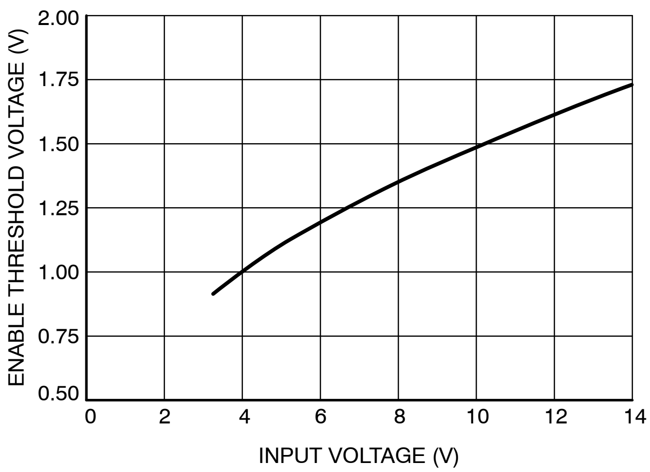


Figure 11. Enable Threshold vs. Input Voltage

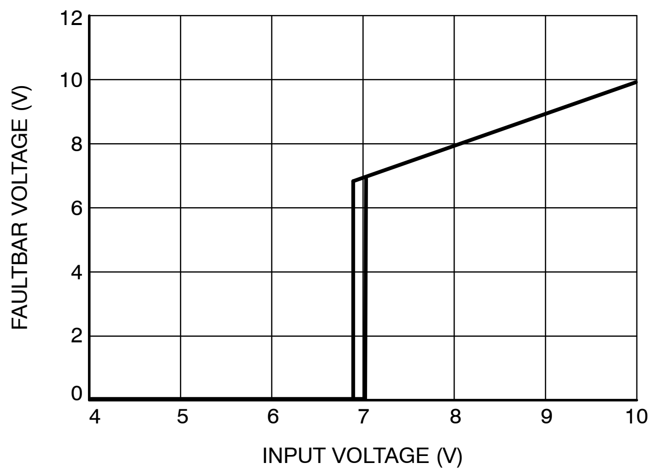


Figure 12. Fault Bar Voltage vs. Input Voltage

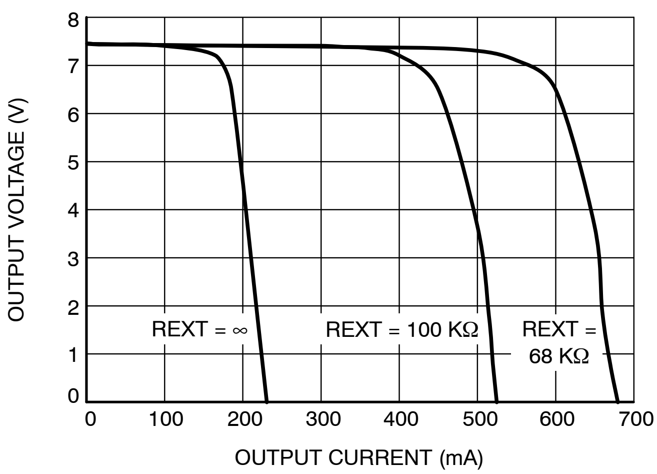


Figure 13. Output Voltage vs. Load Current

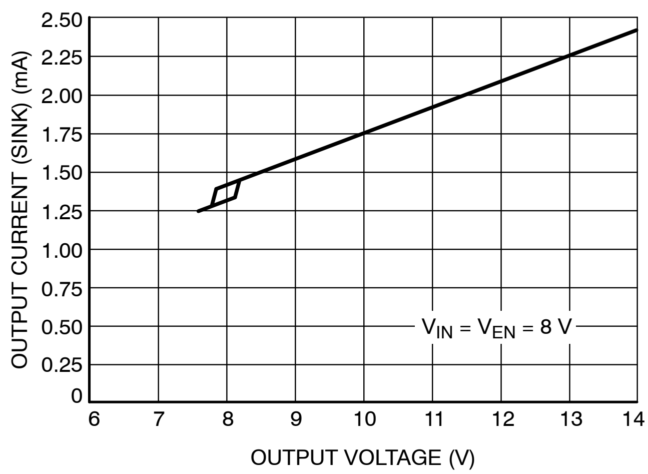


Figure 14. Output Current (Sink) vs. Output Voltage

TYPICAL CHARACTERISTICS (shown for 7.5 V output)

(V_{IN} = 8.5 V, R_1 = 5.1 kΩ, R_2 = 1 kΩ, C_{IN} = 1 μF, C_{OUT} = 2.2 μF, C_{BYP} = 10 nF, R_{EXT} = 68 kΩ, T_A = 25°C unless otherwise specified. All transient characteristics are generated using the evaluation board CAT6201EVAL1.)

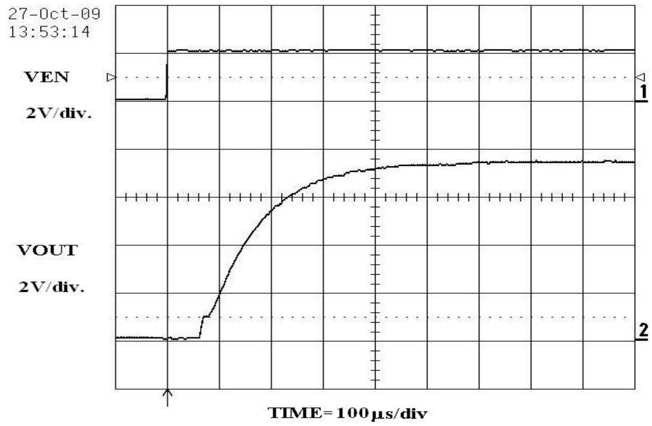


Figure 15. Enable Turn−On (No Load)

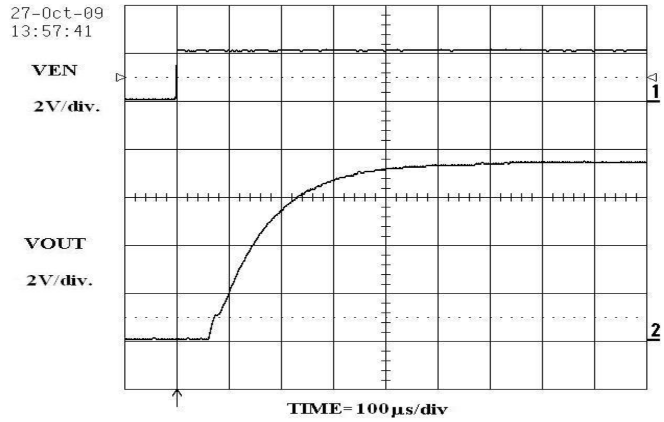


Figure 16. Enable Turn−On (22 Ω Load)

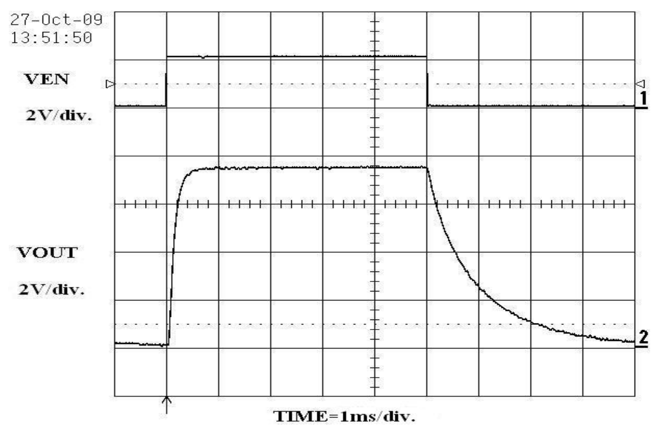


Figure 17. Enable Operation (No Load)

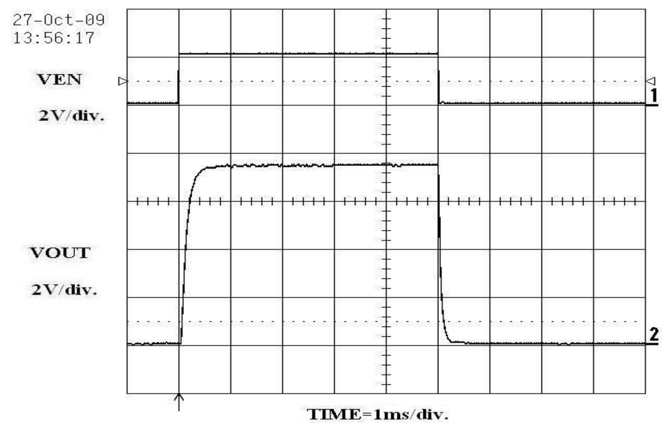


Figure 18. Enable Operation (22 Ω Load)

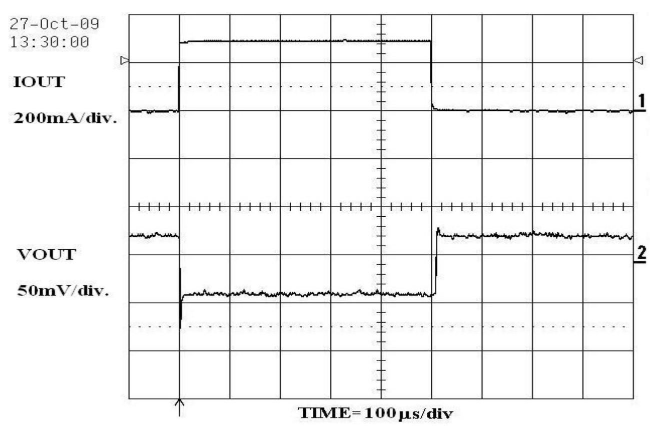


Figure 19. Load Transient Response (1 mA to 330 mA)

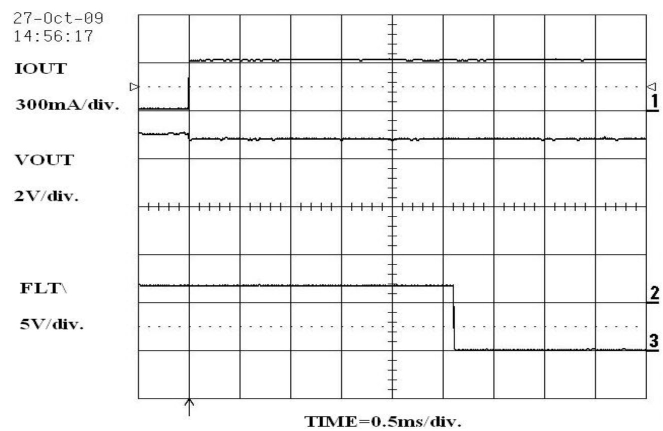
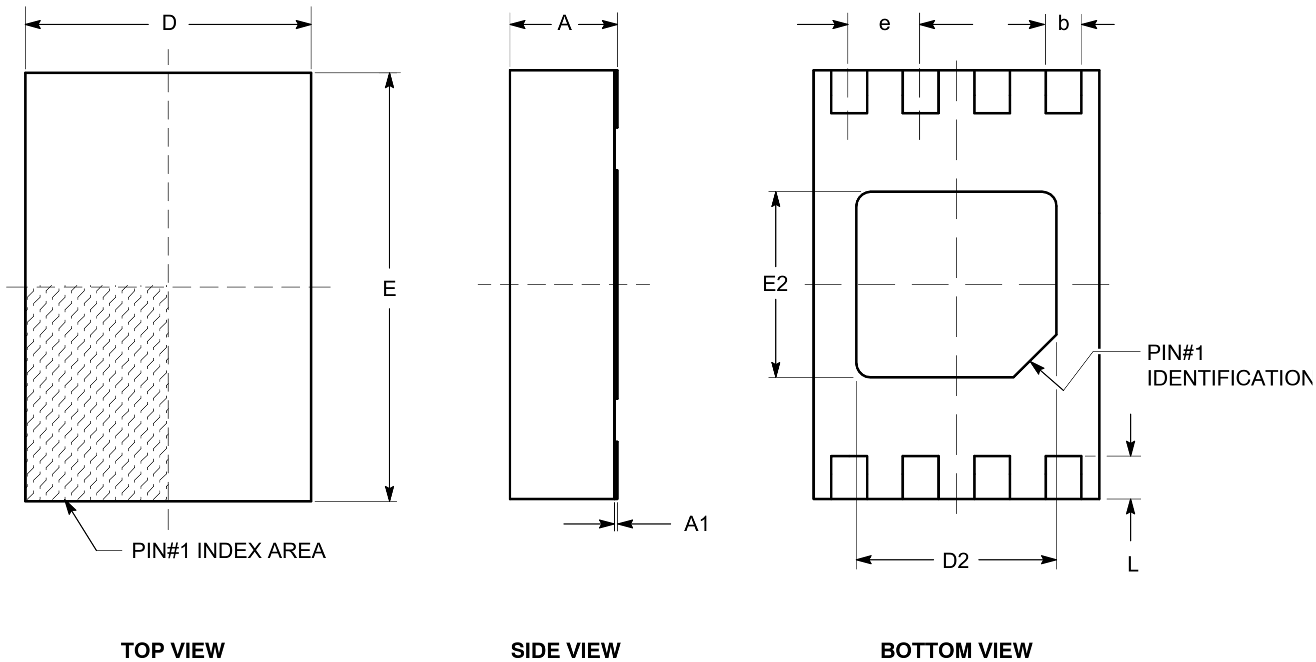


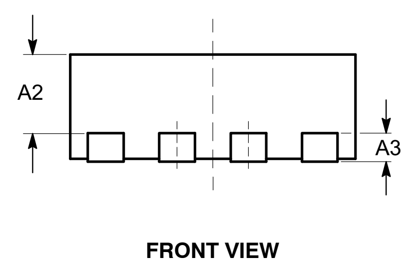
Figure 20. Fault Operation (VIN = 7 V and 22 Ω Load)

PACKAGE DIMENSIONS

TDFN8, 2x3
CASE 511AK−01
ISSUE A



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e		0.50 TYP	
L	0.20	0.30	0.40



Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Lead Finish	Shipping (Note 5)
CAT6201VP2−GT3	HKB	TDFN−8	NiPdAu	3,000 / Tape & Reel
CAV6201BVP2−GT3	HKB	TDFN−8	NiPdAu	3,000 / Tape & Reel

4. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
5. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
6. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

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Europe, Middle East and Africa Technical Support:
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