

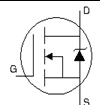
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 3.5\text{mA}$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	10.3	12.1	m Ω	$V_{GS} = 10V, I_D = 62A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Trans conductance	97	—	—	S	$V_{DS} = 50V, I_D = 62A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 150V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 150V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance	—	2.3	—	Ω	

Dynamic Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Q_g	Total Gate Charge	—	77	120	nC	$I_D = 62A$ $V_{DS} = 75V$ $V_{GS} = 10V$ ④
Q_{gs}	Gate-to-Source Charge	—	28	—		
Q_{gd}	Gate-to-Drain Charge	—	26	—		
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)	—	51	—		
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	$V_{DD} = 98V$ $I_D = 62A$ $R_G = 2.2\Omega$ $V_{GS} = 10V$ ④
t_r	Rise Time	—	73	—		
$t_{d(off)}$	Turn-Off Delay Time	—	41	—		
t_f	Fall Time	—	39	—		
C_{iss}	Input Capacitance	—	5270	—	pF	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	490	—		
C_{rss}	Reverse Transfer Capacitance	—	105	—		
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)	—	460	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$ ⑥
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)	—	530	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 120V$ ⑤

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	99	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	396		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 62A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	86	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 130V$ $T_J = 125^\circ\text{C}$ $I_F = 62A$,
		—	110	—		
Q_{rr}	Reverse Recovery Charge	—	300	—	nC	$T_J = 25^\circ\text{C}$ $di/dt = 100A/\mu s$ ④ $T_J = 125^\circ\text{C}$
		—	450	—		
I_{RRM}	Reverse Recovery Current	—	6.5	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax} , starting $T_J = 25^\circ\text{C}$, $L = 0.115\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 63A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- ③ $I_{SD} \leq 62A$, $di/dt \leq 1040A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ\text{C}$.
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧ R_θ is measured at T_J approximately 90°C .
- ⑨ $R_{\theta JC}$ value shown is at time zero.

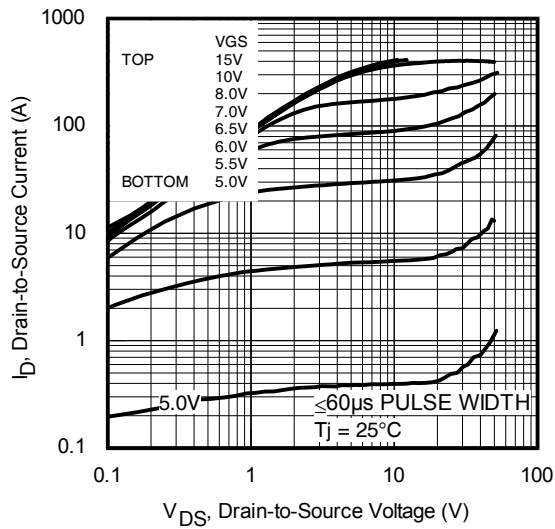


Fig. 1 Typical Output Characteristics

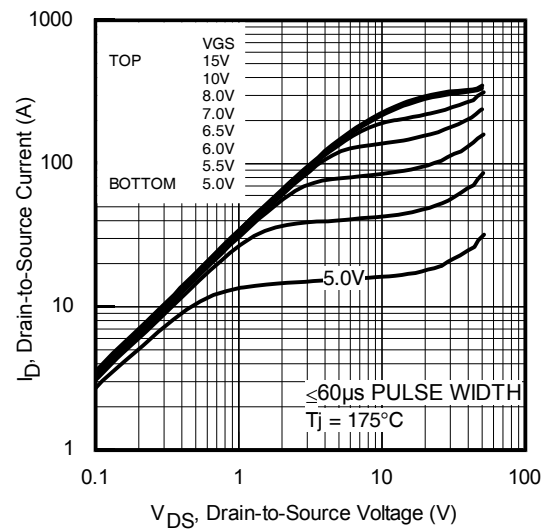


Fig. 2 Typical Output Characteristics

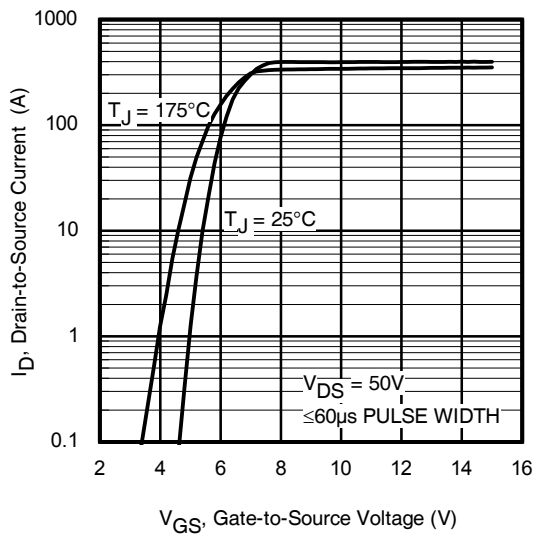


Fig. 3 Typical Transfer Characteristics

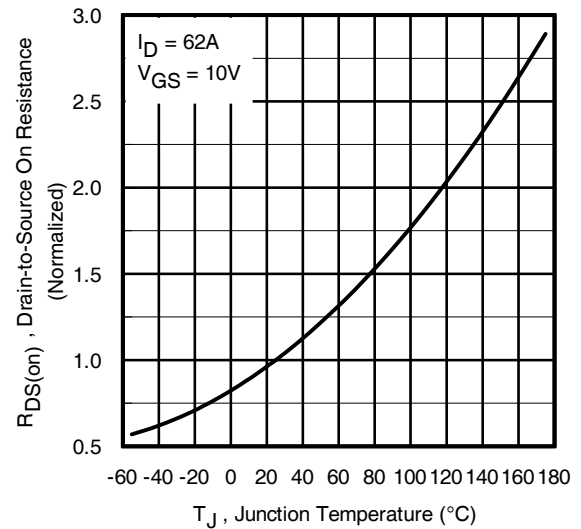


Fig. 4 Normalized On-Resistance vs. Temperature

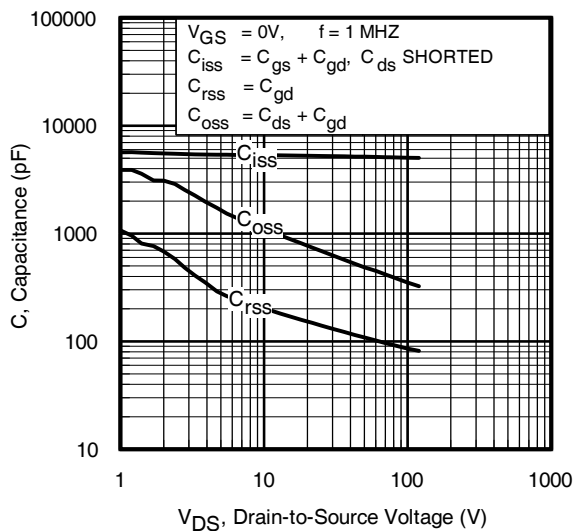


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

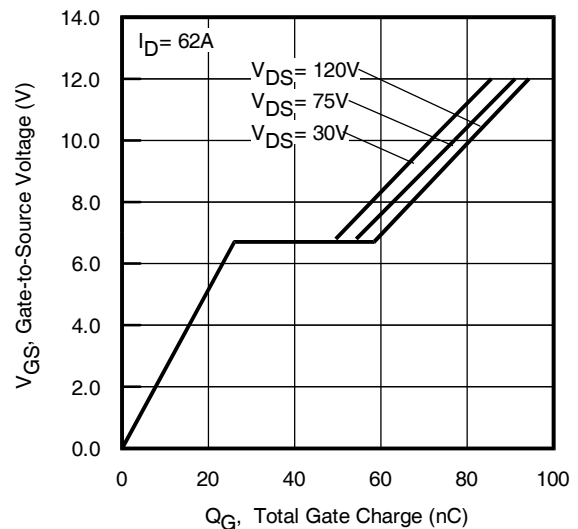


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

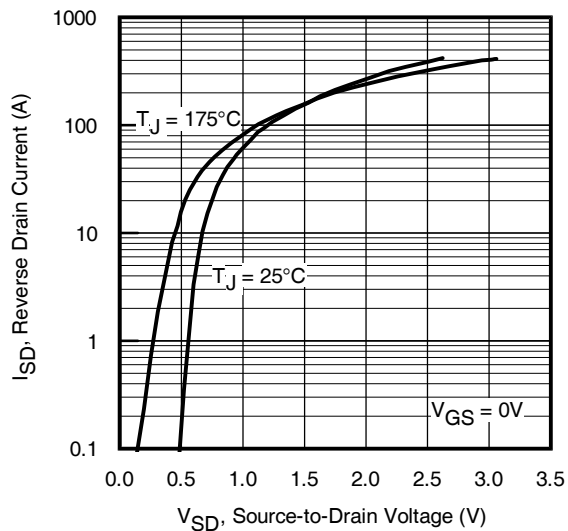


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

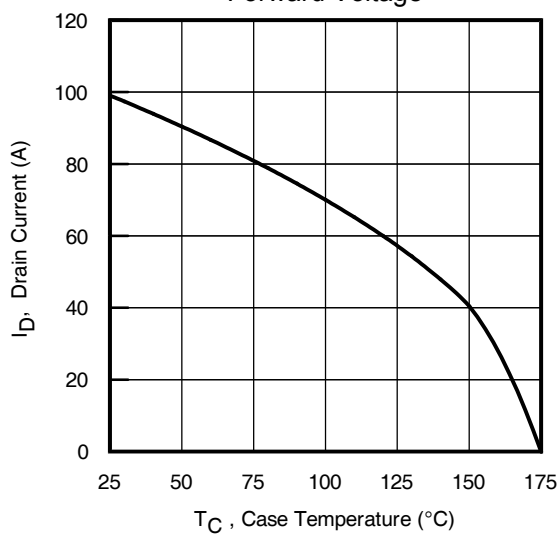


Fig 9. Maximum Drain Current vs. Case Temperature

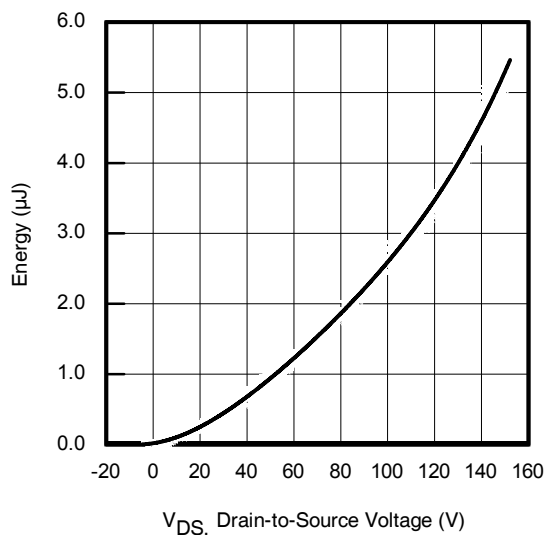


Fig 11. Typical C_{oss} Stored Energy

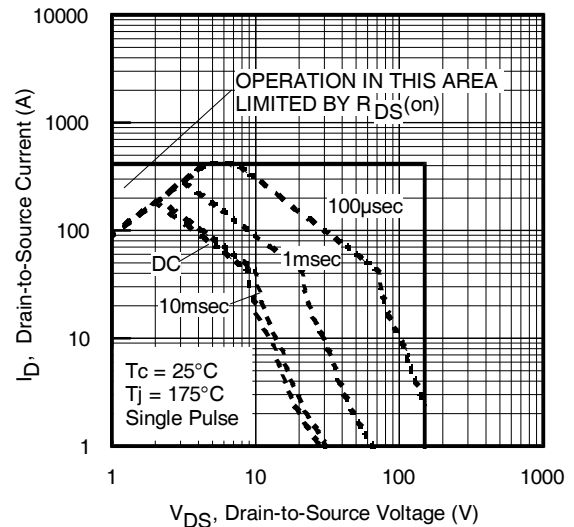


Fig 8. Maximum Safe Operating Area

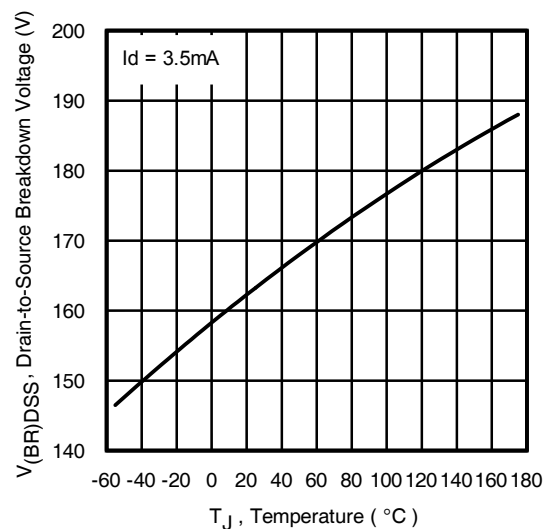


Fig 10. Drain-to-Source Breakdown Voltage

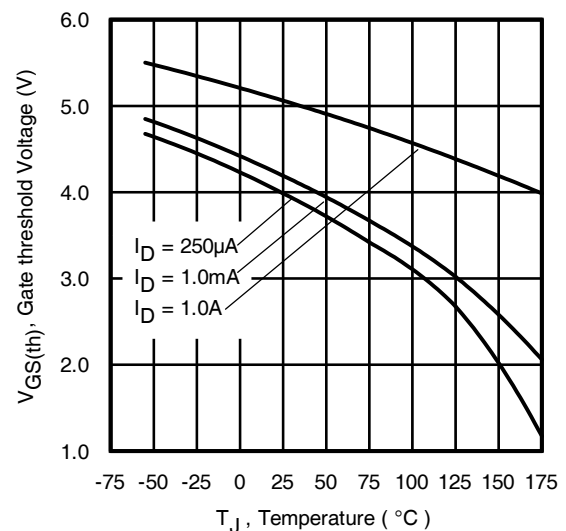
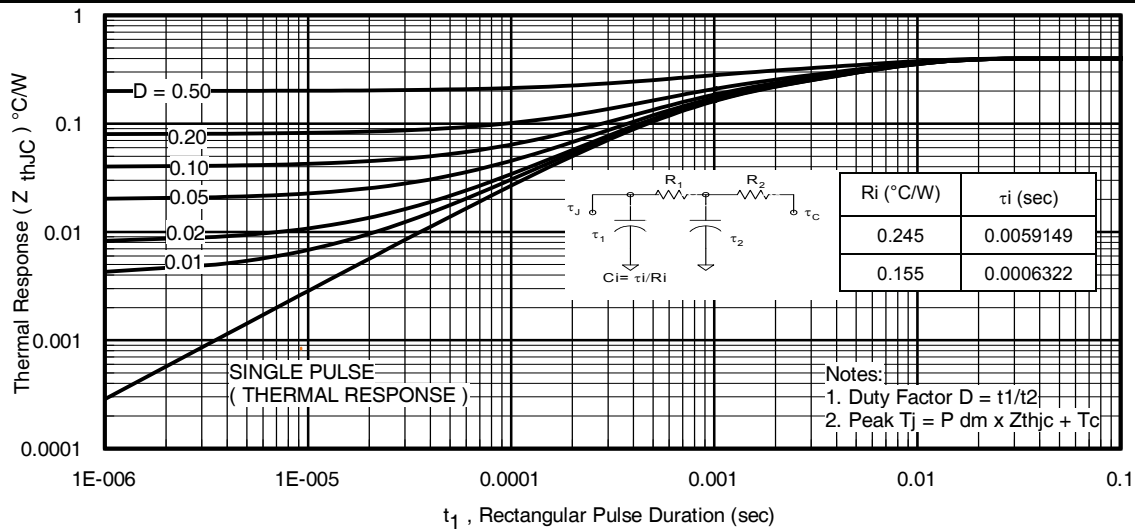
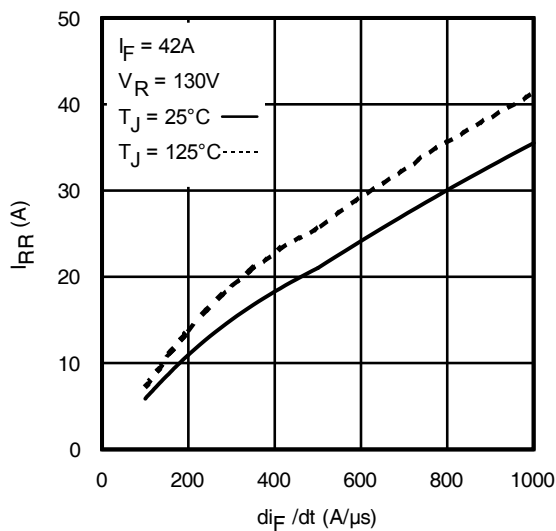
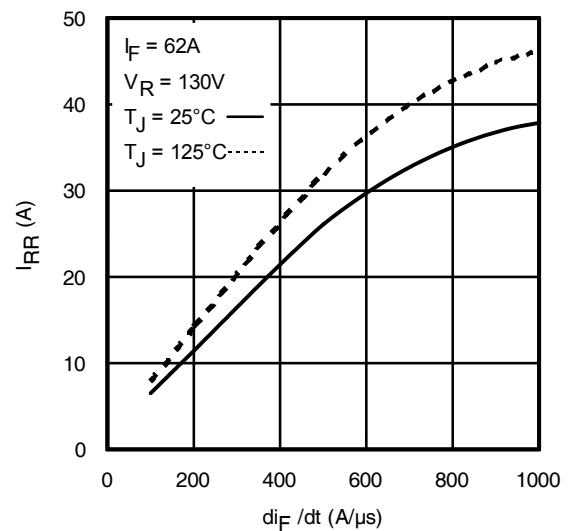
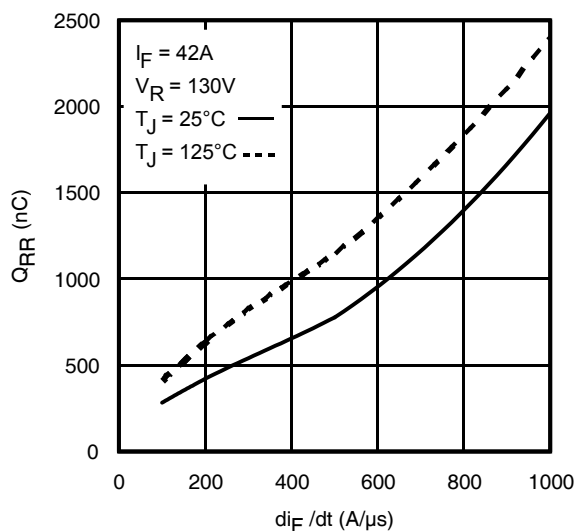
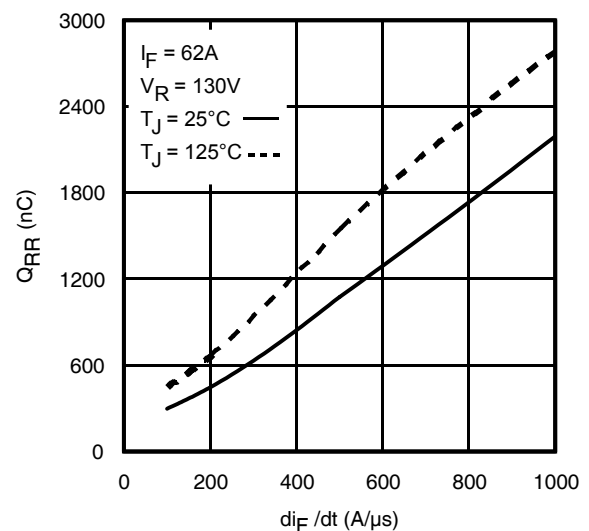


Fig 12. Maximum Avalanche Energy vs. Drain Current


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 14 - Typical Recovery Current vs. di_F/dt

Fig. 15 - Typical Recovery Current vs. di_F/dt

Fig. 16 - Typical Stored Charge vs. di_F/dt

Fig. 17 - Typical Stored Charge vs. di_F/dt

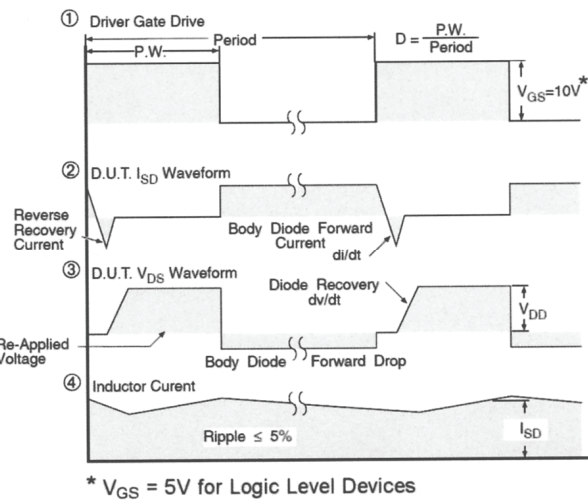
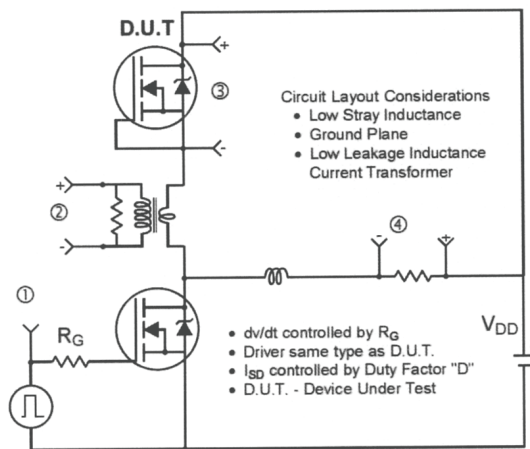


Fig 18. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

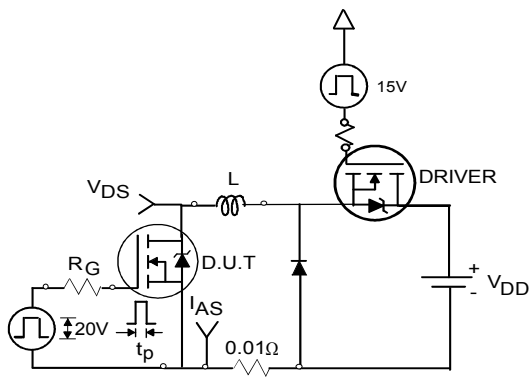


Fig 19a. Unclamped Inductive Test Circuit

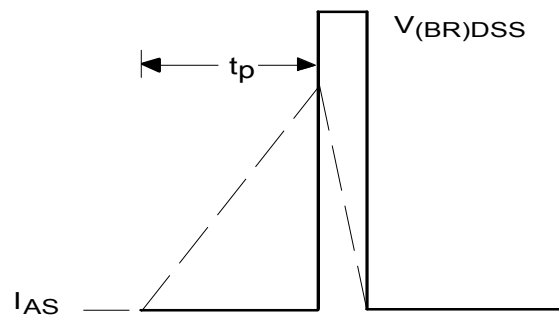


Fig 19b. Unclamped Inductive Waveforms

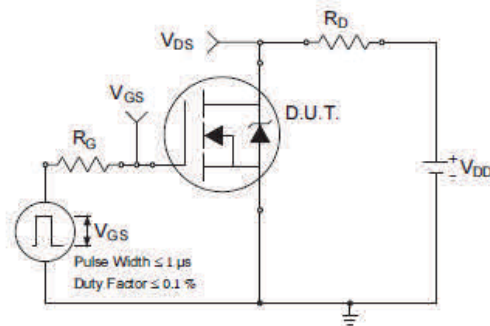


Fig 20a. Switching Time Test Circuit

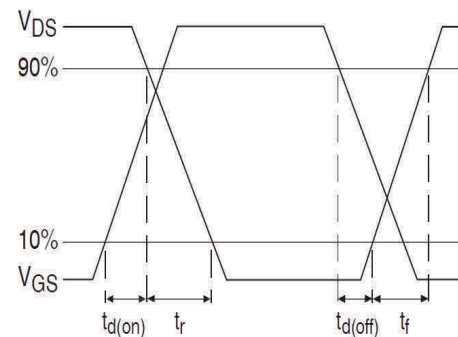


Fig 20b. Switching Time Waveforms

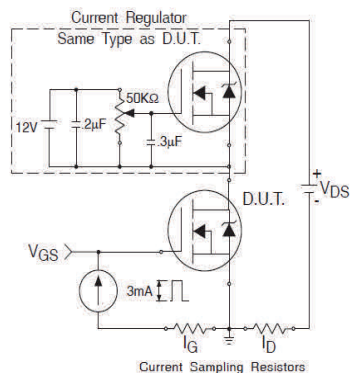


Fig 21a. Gate Charge Test Circuit

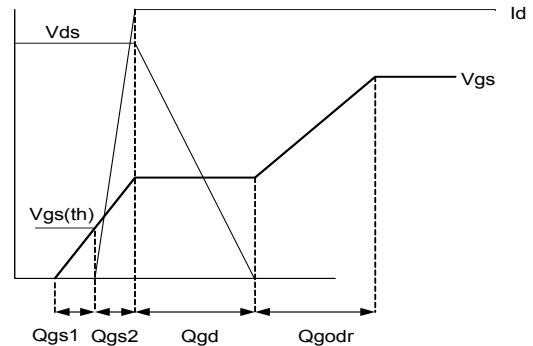
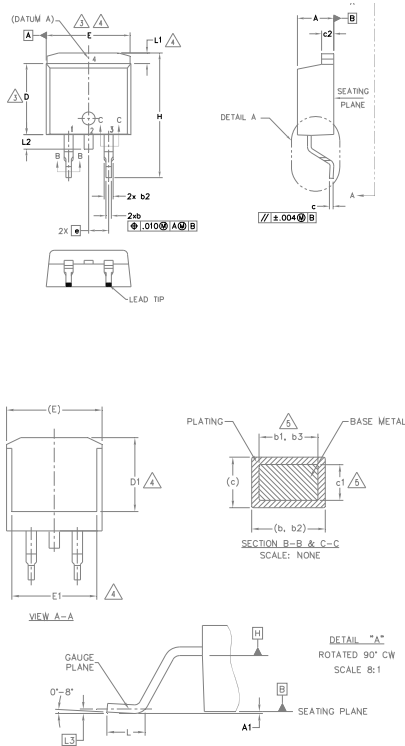


Fig 21b. Gate Charge Waveform

D²Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1, b3 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

S Y M B O L	DIMENSIONS				N O T E S
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	
D1	6.86	—	.270	—	
E	9.65	10.67	.380	.420	3,4
E1	6.22	—	.245	—	4
e	2.54 BSC		.100 BSC		4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	—	1.68	—	.066	
L2	—	1.78	—	.070	
L3	0.25 BSC		.010 BSC		

LEAD ASSIGNMENTS

DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2.- CATHODE
- 3.- ANODE

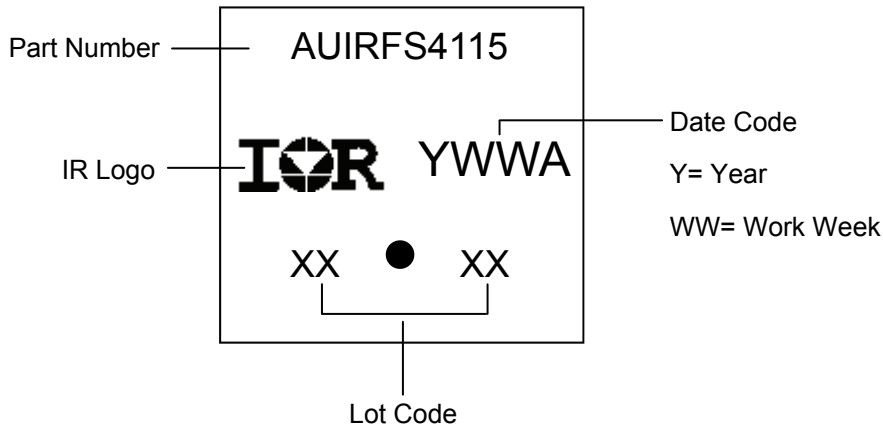
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

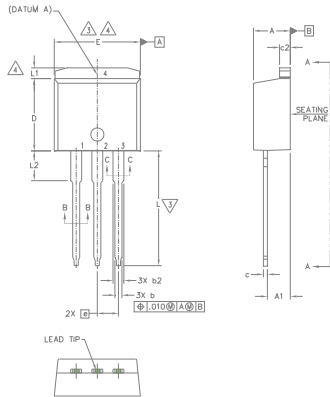
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

D²Pak (TO-263AB) Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

TO-262 Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

IGBTs, CoPACK

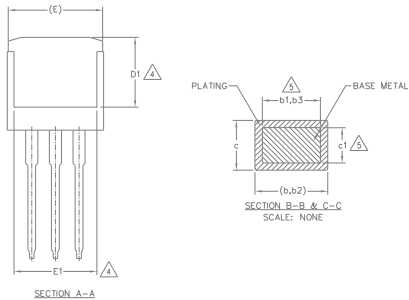
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

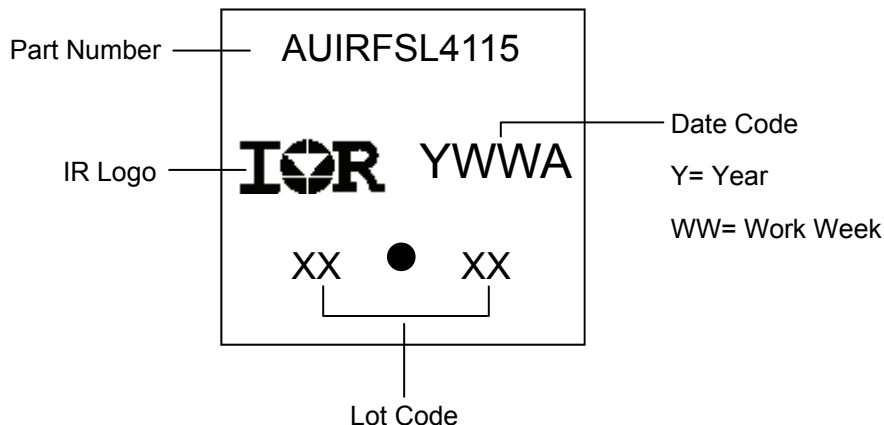
DIODES

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

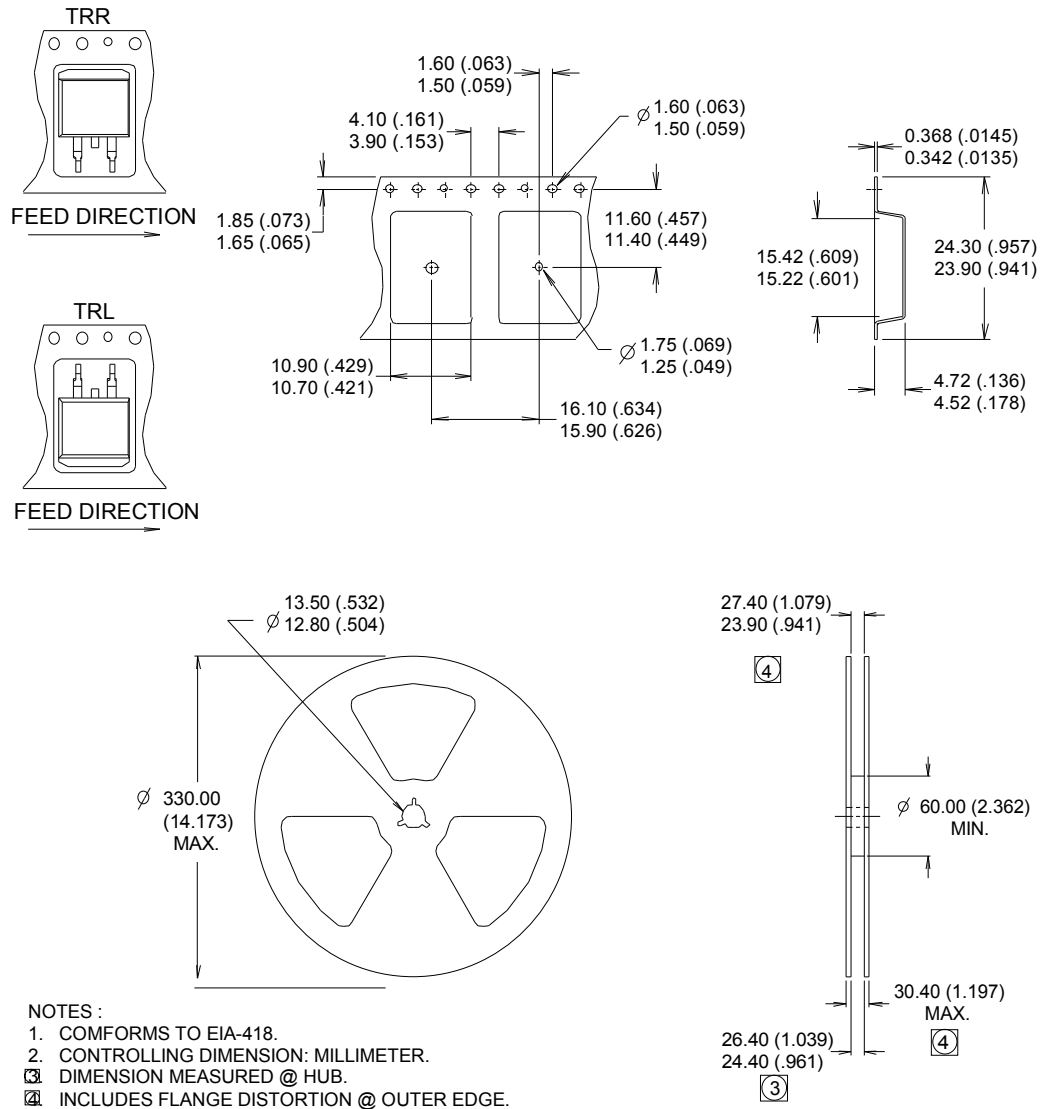


S Y M B O L	DIMENSIONS				N O T E S	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	4.06	4.83	.160	.190	5	
A1	2.03	3.02	.080	.119		
b	0.51	0.99	.020	.039		
b1	0.51	0.89	.020	.035		
b2	1.14	1.78	.045	.070	5	
b3	1.14	1.73	.045	.068		
c	0.38	0.74	.015	.029		
c1	0.38	0.58	.015	.023		
c2	1.14	1.65	.045	.065	3 4 3,4 4	
D	8.38	9.65	.330	.380		
D1	6.86	—	.270	—		
E	9.65	10.67	.380	.420		
E1	6.22	—	.245		4	
e	2.54 BSC		.100 BSC			
L	13.46	14.10	.530	.555		4
L1	—	1.65	—	.065		
L2	3.56	3.71	.140	.146		

TO-262 Part Marking Information



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D²Pak (TO-263AB) Tape & Reel Information (Dimensions are shown in millimeters (inches))


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D ² -Pak	MSL1
		TO-262	
ESD	Human Body Model	Class H2 (+/- 4000V) [†] AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 2000V) [†] AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
10/27/2015	- Updated datasheet with corporate template - Corrected ordering table on page 1.

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