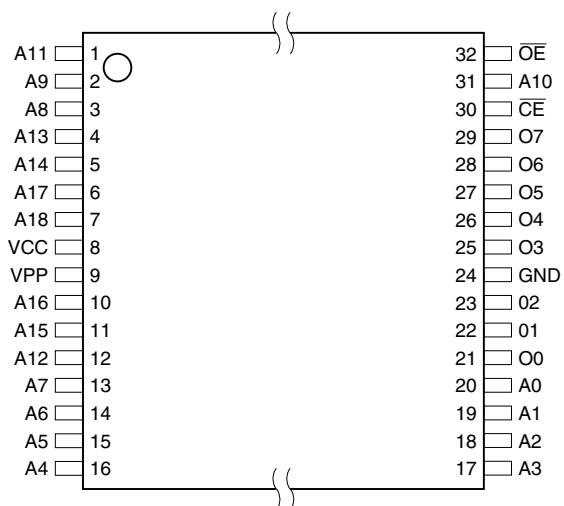


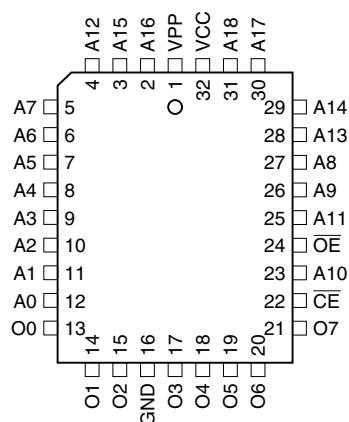
2. Pin Configurations

Pin Name	Function
A0 - A18	Addresses
O0 - O7	Outputs
\overline{CE}	Chip Enable
\overline{OE}	Output Enable

2.1 32-lead TSOP/VSOP (Type 1) Top View



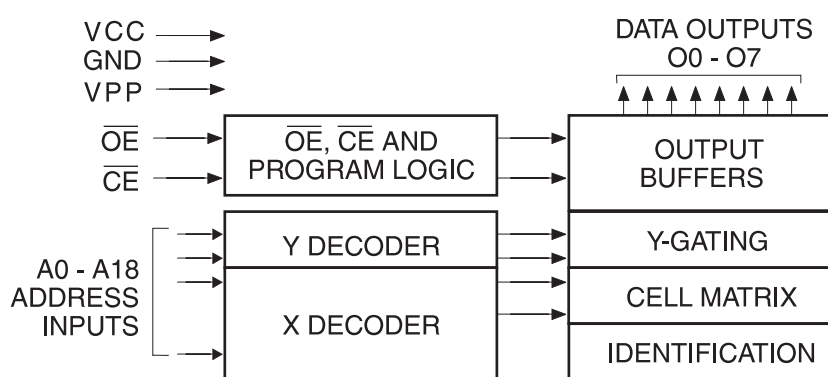
2.2 32-lead PLCC Top View



3. System Considerations

Switching between active and standby conditions via the Chip Enable pin may produce transient voltage excursions. Unless accommodated by the system design, these transients may exceed datasheet limits, resulting in device non-conformance. At a minimum, a 0.1 μF high frequency, low inherent inductance, ceramic capacitor should be utilized for each device. This capacitor should be connected between the V_{CC} and Ground terminals of the device, as close to the device as possible. Additionally, to stabilize the supply voltage level on printed circuit boards with large EPROM arrays, a 4.7 μF bulk electrolytic capacitor should be utilized, again connected between the V_{CC} and Ground terminals. This capacitor should be positioned as close as possible to the point where the power supply is connected to the array.

4. Block Diagram



5. Absolute Maximum Ratings*

Temperature Under Bias.....	-40°C to +85°C
Storage Temperature	-65°C to +125°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V ⁽¹⁾
Voltage on A9 with Respect to Ground	-2.0V to +14.0V ⁽¹⁾
V_{PP} Supply Voltage with Respect to Ground	-2.0V to +14.0V ⁽¹⁾

***NOTICE:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Note: 1. Minimum voltage is -0.6V DC which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC} + 0.75\text{V}$ DC which may be exceeded if certain precautions are observed (consult application notes) and which may overshoot to +7.0V for pulses of less than 20 ns.

6. Operating Modes

Mode/Pin	\overline{CE}	\overline{OE}	Ai	V _{PP}	V _{CC}	Outputs
Read ⁽²⁾	V _{IL}	V _{IL}	Ai	X ⁽¹⁾	V _{CC}	D _{OUT}
Output Disable ⁽²⁾	X	V _{IH}	X	X	V _{CC}	High Z
Standby ⁽²⁾	V _{IH}	X	X	X	V _{CC}	High Z
Rapid Program ⁽³⁾	V _{IL}	V _{IH}	Ai	V _{PP}	V _{CC}	D _{IN}
PGM Verify ⁽³⁾	X	V _{IL}	Ai	V _{PP}	V _{CC}	D _{OUT}
PGM Inhibit ⁽³⁾	V _{IH}	V _{IH}	X	V _{PP}	V _{CC}	High Z
Product Identification ⁽³⁾⁽⁵⁾	V _{IL}	V _{IL}	A9 = V _H ⁽⁴⁾ A0 = V _{IH} or V _{IL} A1 - A18 = V _{IL}	X	V _{CC}	Identification Code

- Notes:
1. X can be V_{IL} or V_{IH}.
 2. Read, output disable, and standby modes require, 3.0V ≤ V_{CC} ≤ 3.6V, or 4.5V ≤ V_{CC} ≤ 5.5V.
 3. Refer to Programming Characteristics. Programming modes require V_{CC} = 6.5V.
 4. V_H = 12.0 ± 0.5V.
 5. Two identifier bytes may be selected. All Ai inputs are held low (V_{IL}), except A9 which is set to V_H and A0 which is toggled low (V_{IL}) to select the Manufacturer's Identification byte and high (V_{IH}) to select the Device Code byte.

7. DC and AC Operating Conditions for Read Operation

	AT27LV040A-90
Industrial Operating Temperature (Case)	-40°C - 85°C
V _{CC} Power Supply	3.0V to 3.6V
	5V ± 10%

8. DC and Operating Characteristics for Read Operation

Symbol	Parameter	Condition	Min	Max	Units
V_{CC} = 3.0V to 3.6V					
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC}		±1	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0V to V _{CC}		±5	μA
I _{PP1} ⁽²⁾	V _{PP} ⁽¹⁾ Read/Standby Current	V _{PP} = V _{CC}		10	μA
I _{SB}	V _{CC} ⁽¹⁾ Standby Current	I _{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		20	μA
		I _{SB2} (TTL), $\overline{CE} = 2.0$ to V _{CC} + 0.5V		100	μA
I _{CC}	V _{CC} Active Current	f = 5 MHz, I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$		10	mA
V _{IL}	Input Low Voltage		-0.6	0.8	V
V _{IH}	Input High Voltage		2.0	V _{CC} + 0.5	V
V _{OL}	Output Low Voltage	I _{OL} = 2.0 mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -2.0 mA	2.4		V
V_{CC} = 4.5V to 5.5V					
I _{LI}	Input Load Current	V _{IN} = 0V to V _{CC}		±1	μA
I _{LO}	Output Leakage Current	V _{OUT} = 0V to V _{CC}		±5	μA
I _{PP1} ⁽²⁾	V _{PP} ⁽¹⁾ Read/Standby Current	V _{PP} = V _{CC}		10	μA
I _{SB}	V _{CC} ⁽¹⁾ Standby Current	I _{SB1} (CMOS), $\overline{CE} = V_{CC} \pm 0.3V$		100	μA
		I _{SB2} (TTL), $\overline{CE} = 2.0$ to V _{CC} + 0.5V		1	mA
I _{CC}	V _{CC} Active Current	f = 5 MHz, I _{OUT} = 0 mA, $\overline{CE} = V_{IL}$		30	mA
V _{IL}	Input Low Voltage		-0.6	0.8	V
V _{IH}	Input High Voltage		2.0	V _{CC} + 0.5	V
V _{OL}	Output Low Voltage	I _{OL} = 2.1 mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -400 μA	2.4		V

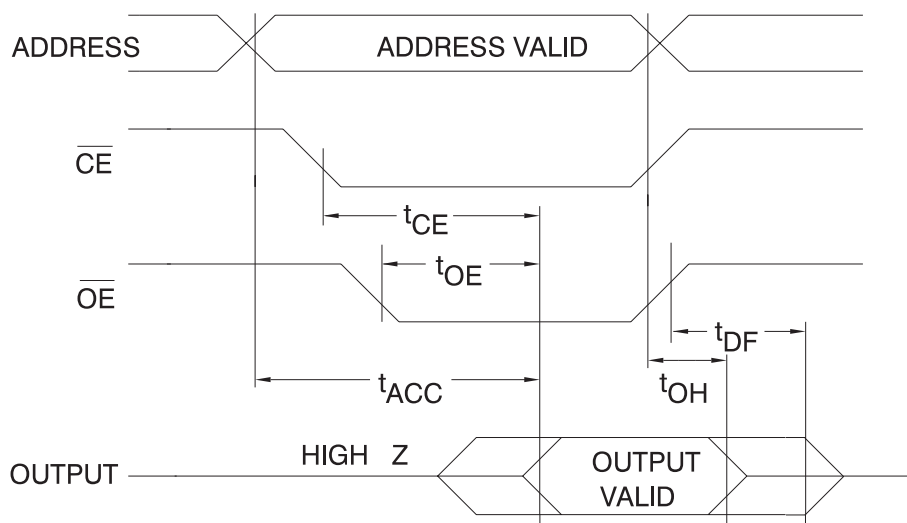
- Notes: 1. V_{CC} must be applied simultaneously with or before V_{PP} and removed simultaneously with or after V_{PP}
2. V_{PP} may be connected directly to V_{CC}, except during programming. The supply current would then be the sum of I_{CC} and I_{PP}

9. AC Characteristics for Read Operation

$V_{CC} = 3.0V$ to $3.6V$ and $4.5V$ to $5.5V$

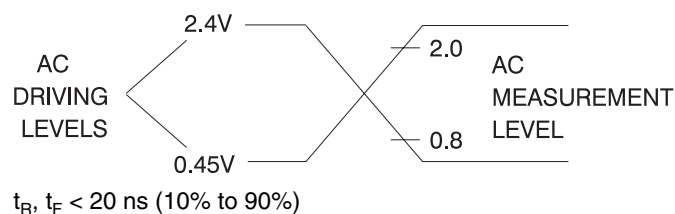
Symbol	Parameter	Condition	AT27LV040A-90		Units
			Min	Max	
$t_{ACC}^{(3)}$	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		90	ns
$t_{CE}^{(2)}$	\overline{CE} to Output Delay	$\overline{OE} = V_{IL}$		90	ns
$t_{OE}^{(2)(3)}$	\overline{OE} to Output Delay	$\overline{CE} = V_{IL}$		50	ns
$t_{DF}^{(4)(5)}$	\overline{OE} or \overline{CE} High to Output Float, Whichever Occurred First			60	ns
t_{OH}	Output Hold from Address, \overline{CE} or \overline{OE} , Whichever Occurred First		0		ns

10. AC Waveforms for Read Operation⁽¹⁾

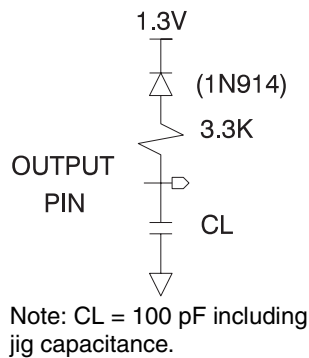


- Notes:
1. Timing measurement references are 0.8V and 2.0V. Input AC drive levels are 0.45V and 2.4V. See Input Test Waveforms and Measurement Levels.
 2. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} .
 3. \overline{OE} may be delayed up to $t_{ACC} - t_{OE}$ after the address is valid without impact on t_{ACC} .
 4. This parameter is only sampled and is not 100% tested.
 5. Output float is defined as the point when data is no longer driven.

11. Input Test Waveforms and Measurement Level



12. Output Test Load



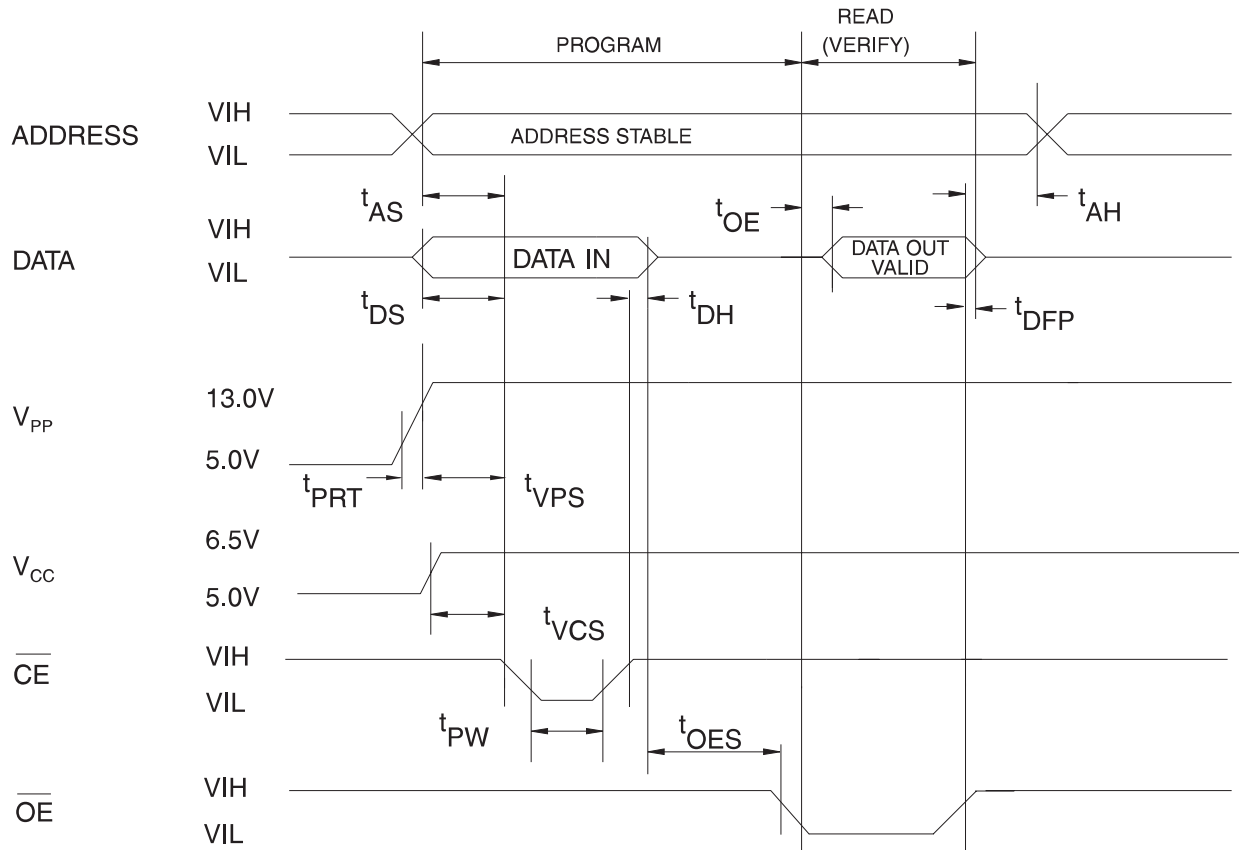
13. Pin Capacitance

$f = 1 \text{ MHz}$, $T = 25^\circ\text{C}$ ⁽¹⁾

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	8	pF	$V_{IN} = 0V$
C_{OUT}	8	12	pF	$V_{OUT} = 0V$

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

14. Programming Waveforms⁽¹⁾



- Notes:
1. The Input Timing Reference is 0.8V for V_{IL} and 2.0V for V_{IH} .
 2. t_{OE} and t_{DFP} are characteristics of the device but must be accommodated by the programmer.
 3. When programming the AT27LV040A a 0.1 μ F capacitor is required across V_{PP} and ground to suppress spurious voltage transients.

15. DC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions	Limits		Units
			Min	Max	
I_{LI}	Input Load Current	$V_{IN}=V_{IL}, V_{IH}$		± 10	μA
V_{IL}	Input Low Level		-0.6	0.8	V
V_{IH}	Input High Level		2.0	$V_{CC} + 0.5$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1 \text{ mA}$		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400 \mu\text{A}$	2.4		V
I_{CC2}	V_{CC} Supply Current (Program and Verify)			40	mA
I_{PP2}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$		20	mA
V_{ID}	A9 Product Identification Voltage		11.5	12.5	V

16. AC Programming Characteristics

$T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.5 \pm 0.25\text{V}$, $V_{PP} = 13.0 \pm 0.25\text{V}$

Symbol	Parameter	Test Conditions ⁽¹⁾	Limits		Units
			Min	Max	
t_{AS}	Address Setup Time	Input Rise and Fall Times: (10% to 90%) 20 ns	2		μs
t_{OES}	\overline{OE} Setup Time		2		μs
t_{DS}	Data Setup Time		2		μs
t_{AH}	Address Hold Time	Input Pulse Levels: 0.45V to 2.4V	0		μs
t_{DH}	Data Hold Time		2		μs
t_{DFP}	\overline{OE} High to Output Float Delay ⁽²⁾		0	130	ns
t_{VPS}	V_{PP} Setup Time	Input Timing Reference Level: 0.8V to 2.0V	2		μs
t_{VCS}	V_{CC} Setup Time		2		μs
t_{PW}	\overline{CE} Program Pulse Width ⁽³⁾	Output Timing Reference Level: 0.8V to 2.0V	95	105	μs
t_{OE}	Data Valid from \overline{OE} ⁽²⁾			150	ns
t_{PRT}	V_{PP} Pulse Rise Time During Programming		50		ns

- Notes:
- V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}
 - This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
 - Program Pulse width tolerance is 100 $\mu\text{sec} \pm 5\%$.

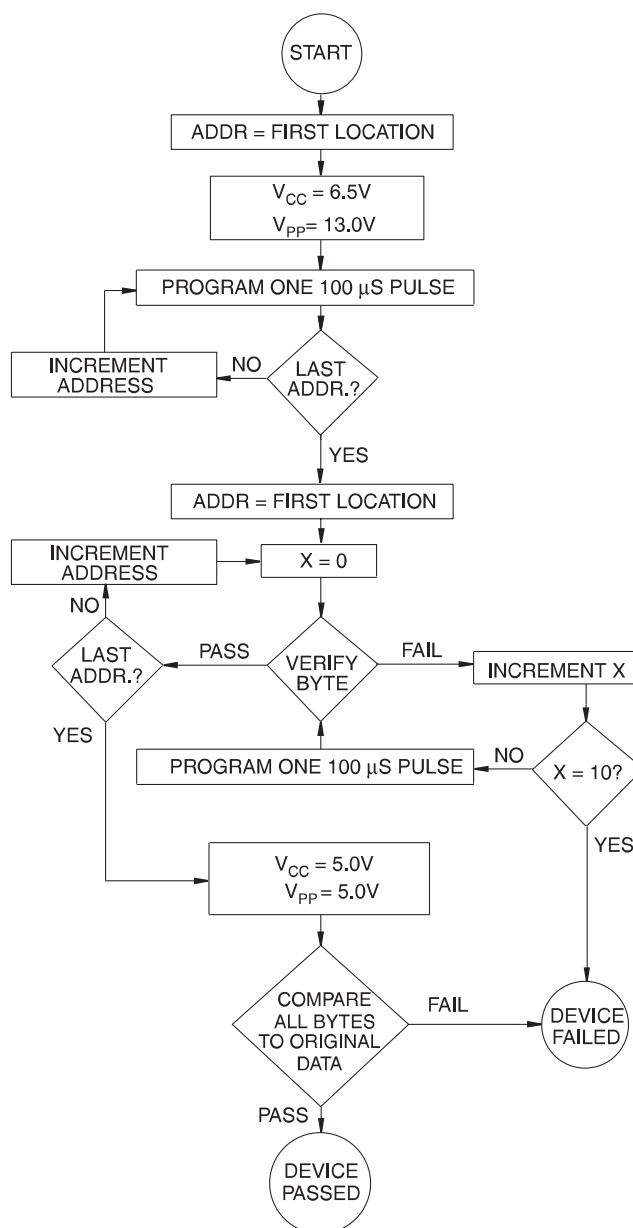
17. Atmel's AT27LV040A Integrated Product Identification Code⁽¹⁾

Codes	Pins									Hex Data
	A0	O7	O6	O5	O4	O3	O2	O1	O0	
Manufacturer	0	0	0	0	1	1	1	1	0	1E
Device Type	1	0	0	0	0	1	0	1	1	0B

Note: 1. The AT27LV040A has the same Product Identification Code as the AT27C040. Both are programming compatible.

18. Rapid Programming Algorithm

A 100 μs $\overline{\text{CE}}$ pulse width is used to program. The address is set to the first location. V_{CC} is raised to 6.5V and V_{PP} is raised to 13.0V. Each address is first programmed with one 100 μs $\overline{\text{CE}}$ pulse without verification. Then a verification/reprogramming loop is executed for each address. In the event a byte fails to pass verification, up to 10 successive 100 μs pulses are applied with a verification after each pulse. If the byte fails to verify after 10 pulses have been applied, the part is considered failed. After the byte verifies properly, the next address is selected until all have been checked. V_{PP} is then lowered to 5.0V and V_{CC} to 5.0V. All bytes are read again and compared with the original data to determine if the device passes or fails.



19. Ordering Information

19.1 Standard Package

t _{ACC} (ns)	I _{CC} (mA) V _{CC} = 3.6V		Ordering Code	Package	Operation Range
	Active	Standby			
90	8	0.02	AT27LV040A-90JI AT27LV040A-90TI AT27LV040A-90VI	32J 32T 32V ⁽¹⁾	Industrial (-40°C to 85°C)

Note: Not recommended for new designs. Use Green package option.

19.2 Green Package Option (Pb/Halide-free)

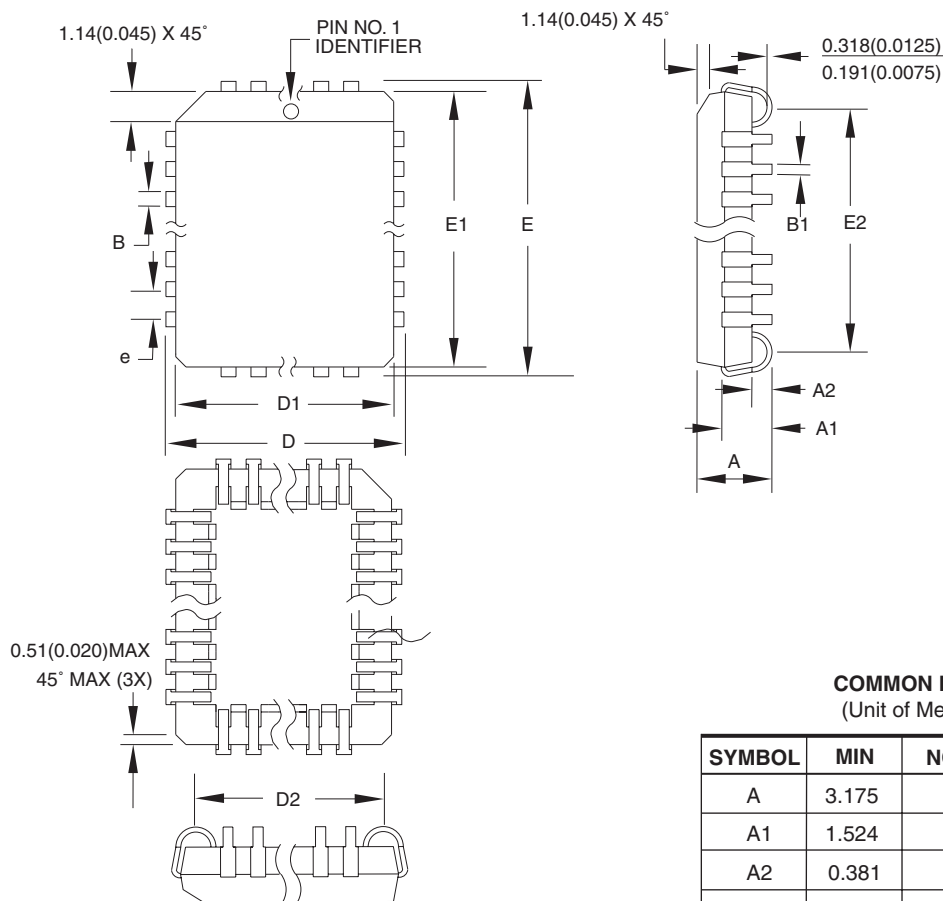
t _{ACC} (ns)	I _{CC} (mA) V _{CC} = 3.6V		Ordering Code	Package	Operation Range
	Active	Standby			
90	8	0.02	AT27LV040A-90JU AT27LV040A-90TU	32J 32T	Industrial (-40°C to 85°C)

Note: 1. The 32-lead VSOP package is not recommended for new designs.

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
32T	32-lead, Plastic Thin Small Outline Package (TSOP)
32V	32-lead, Plastic Thin Small Outline Package (VSOP)

20. Packaging Information

20.1 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

- Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)

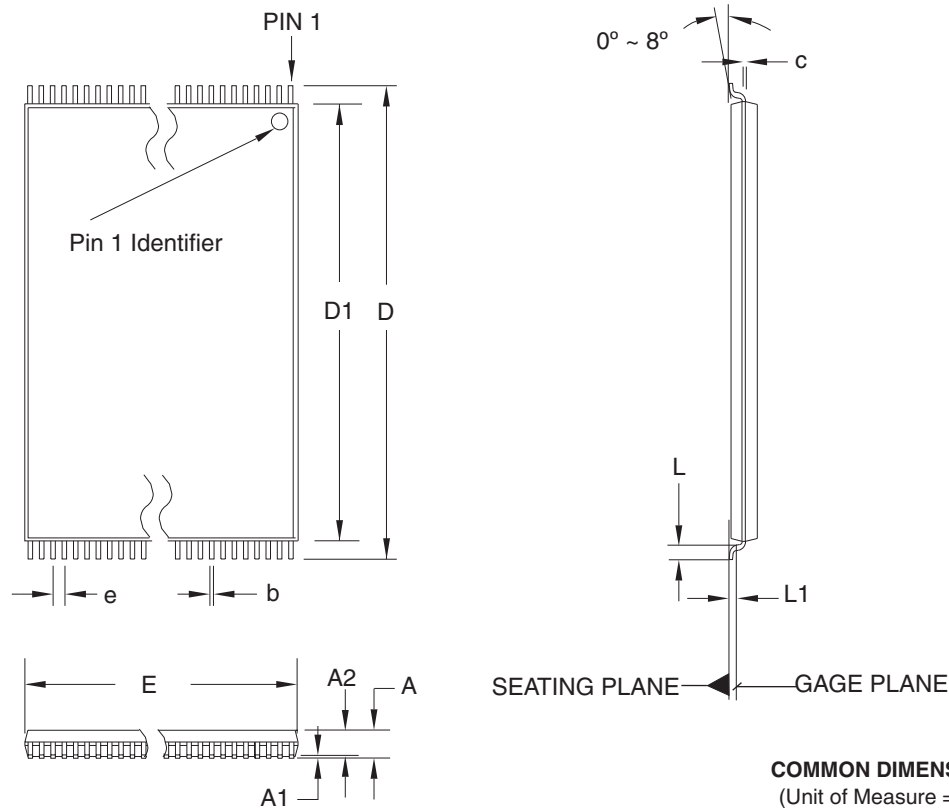
DRAWING NO.

32J

REV.

B

20.2 32T – TSOP



- Notes:
1. This package conforms to JEDEC reference MO-142, Variation BD.
 2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
 3. Lead coplanarity is 0.10 mm maximum.

10/18/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32T, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline
Package, Type I (TSOP)

DRAWING NO.

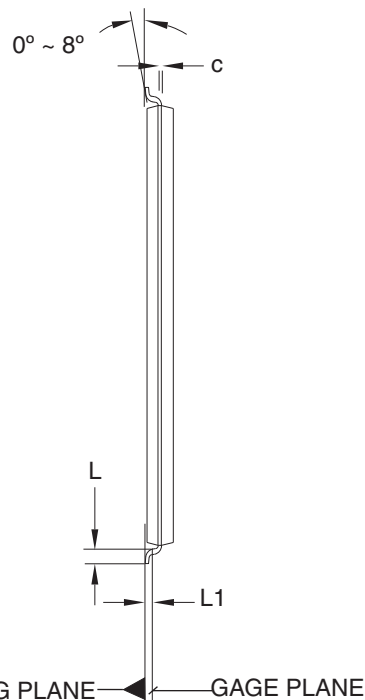
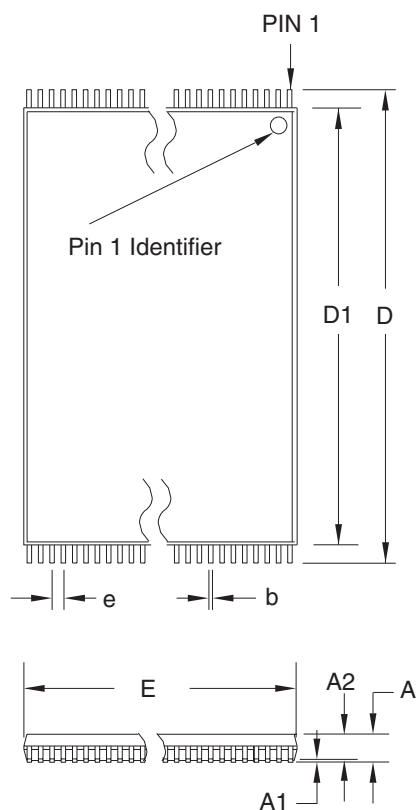
32T

REV.

B



20.3 32V – VSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	—	—	1.20	
A1	0.05	—	0.15	
A2	0.95	1.00	1.05	
D	13.80	14.00	14.20	
D1	12.30	12.40	12.50	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	—	0.21	
e	0.50 BASIC			

- Notes:
1. This package conforms to JEDEC reference MO-142, Variation BA.
 2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
 3. Lead coplanarity is 0.10 mm maximum.

10/18/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32V, 32-lead (8 x 14 mm Package) Plastic Thin Small Outline
Package, Type I (VSOP)

DRAWING NO.

32V

REV.

B



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