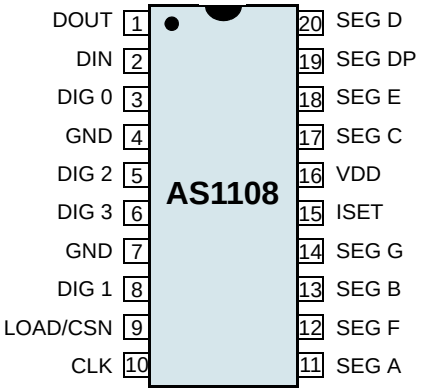
4 Pinout

Pin Assignments

Figure 2. DIP and SO Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	DOUT	**Serial-Data Output**. The data into pin DIN is valid at pin DOUT 16.5 clock cycles later. This pin is used to daisy-chain several AS1108 devices and is never high-impedance.
2	DIN	**Serial-Data Input**. Data is loaded into the internal 16-bit shift register on the rising edge of pin CLK.
3, 5, 6, 8	DIG 0:DIG 3	**Digit Drive Lines**. 4 four-digit drive lines that sink current from the display common cathode. The AS1108 pulls the digit outputs to V_{DD} when turned off.
4, 7	GND	**Ground**. Both GND pins must be connected.
9	LOAD/CSN	**Load-Data Input**. The last 16 bits of serial data are latched on the rising edge of this pin. **Chip-Select Input** (AS1108 SPI-enabled only). Serial data is loaded into the shift register while this pin is low. The last 16 bits of serial data are latched on the rising edge of this pin.
10	CLK	**Serial-Clock Input**. 10MHz maximum rate. Data is shifted into the internal shift register on the rising edge of this pin. Data is clocked out of DOUT on the falling edge of this pin. On the AS1108 SPI-enabled, the CLK input is active only while pin LOAD/CSN is low.
11, 12, 13, 14, 17, 18, 19, 20	SEG A:SEG G, SEG DP	**Seven Segment and Decimal Point Drive Lines**. 8 seven-segment drives and decimal point drive that source current to the display. When a segment driver is turned off it is pulled to GND.
15	ISET	**Set Segment Current**. Connect to V_{DD} through R_{SET} to set the peak segment current (see Selecting RSET Resistor Value and Using External Drivers on page 13).
16	VDD	**Positive Supply Voltage**. Connect to +2.7 to +5.5V supply.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 4 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Min	Max	Units	Notes
Voltage (with respect to GND)	V_{DD}	-0.3	7	V	
	DIN, CLK, LOAD/CSN	-0.3	7	V	
	All Other Pins	-0.3	7 or V_{DD} + 0.3	V	
Current	DIG 0:DIG 3 Sink Current		500	mA	
	SEG A:SEG G, SEG DP		100	mA	
Continuous Power Dissipation (T_{AMB} = +85ºC)	Narrow Plastic DIP		1066	mW	Derate 13.3mW/ºC above +70ºC
	Wide SOIC		941	mW	Derate 11.8mW/ºC above +70ºC
Operating Temperature Ranges (T_{MIN} toT_{MAX})		0	+70	ºC	
Storage Temperature Range		-65	+150	ºC	
Package Body Temperature (Wide SOIC) [1]			+260	ºC	
Soldering Temperature (Narrow DIP) [2]			+260	ºC	
Humidity		5	85	%	Non-condensing
Electrostatic Discharge [3]	Digital Outputs		1000	V	
	All Other Pins		1000	V	
Latch-Up Immunity [4]			±200	mA	All pins. Except pin 11: ±180mA.

1. The reflow peak soldering temperature (body temperature) is specified according to *IPC/JEDEC J-STD-020D "Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices"*.
2. Specified according *JESD22-B106 "Resistance to Soldering Temperature for Through-Hole Mounted Devices"*.
3. Norm: *MIL 883 E method 3015*.
4. Norm: *JEDEC 17*.

6 Electrical Characteristics

Conditions: V_{DD} = 2.7 to 5.5V, R_{SET} = 9.53kΩ±1%, T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified).

Table 3. Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Supply Voltage	V_{DD}		2.7	5.0	5.5	V
Shutdown Supply Current	I_{DDSD}	All digital inputs at V_{DD} or GND, T_{AMB} = +25ºC			10	µA
Operating Supply Current	I_{DD}	R_{SET} = open circuit.			1	mA
		All segments and decimal point on; I_{SEG} = -40mA.		330		
Display Scan Rate	f_{OSC}	4 digits scanned	1000	1600	2600	Hz
Digit Drive Sink Current	I_{DIGIT}	V_{OUT} = 0.65V	320			mA
Segment Drive Source Current	I_{SEG}	V_{DD} = 5.0V, V_{OUT} = (V_{DD} -1V)	-30	-40	-45	mA
Segment Drive Current Matching	ΔI_{SEG}			3.0		%
Digit Drive Source Current	I_{DIGIT}	Digit off, V_{DIGIT} = (V_{DD} - 0.3V)	-2			mA
Segment Drive Sink Current	I_{SEG}	Segment off, V_{SEG} = 0.3V	5			mA
Slow Segment Blink Period (ON phase, Internal Oscillator)	$t_{SLOWBLINK}$		0.64	1	1.65	s
Fast Segment Blink Period (ON phase, Internal Oscillator)	$t_{FASTBLINK}$		0.32	0.5	0.83	s
Fast or Slow Segment Blink Duty Cycle (Guaranteed by design)			49.9	50	50.1	%

Table 4. Logic Inputs/Outputs Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Current DIN, CLK, LOAD/CSN	I_{IH}, I_{IL}	V_{IN} = 0V or V_{DD}	-1		1	µA
Logic High Input Voltage	V_{IH}		0.7 x V_{DD}			V
Logic Low Input Voltage	V_{IL}	V_{DD} = 5.0V ± 10%			0.8	V
		V_{DD} = 3.0V ± 10%			0.6	
Output High Voltage	V_{OH}	DOUT, I_{SOURCE} = -1mA, V_{DD} = 5.0V ± 10%	V_{DD} - 1			V
		DOUT, I_{SOURCE} = -1mA, V_{DD} = 3.0V ± 10%	V_{DD} - 0.5			
Output Low Voltage	V_{OL}	DOUT, I_{SINK} = 1.6mA			0.4	V
Hysteresis Voltage	ΔV_I	DIN, CLK, LOAD/CSN		1		V

Table 5. Timing Characteristics (see Figure 10 on page 7)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CLK Clock Period	t_{CP}		100			ns
CLK Pulse Width High	t_{CH}		50			ns
CLK Pulse Width Low	t_{CL}		50			ns
CSMFall-to-CLK Rise Setup Time (AS1108 SPI-programmed)	t_{CSS}		25			ns
CLK Rise-to -LOAD/CSN Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		25			ns
DIN Hold Time	t_{DH}		0			ns
Output Data Propagation Delay	t_{DO}	C_{LOAD} = 50pF			25	ns
LOAD Rising Edge-to-Next Clock Rising Edge	t_{LDCK}		50			ns
Minimum LOAD/CSN Pulse High	t_{CSW}		50			ns
Data-to-Segment Delay	t_{DSPD}				2.25	ms

Note: All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

7 Typical Operating Characteristics

V_{DD} = 5V, R_{SET} = 9.53kΩ, T_{AMB} = 25ºC (unless otherwise specified).

Figure 3. Scan Frequency vs.Temperature

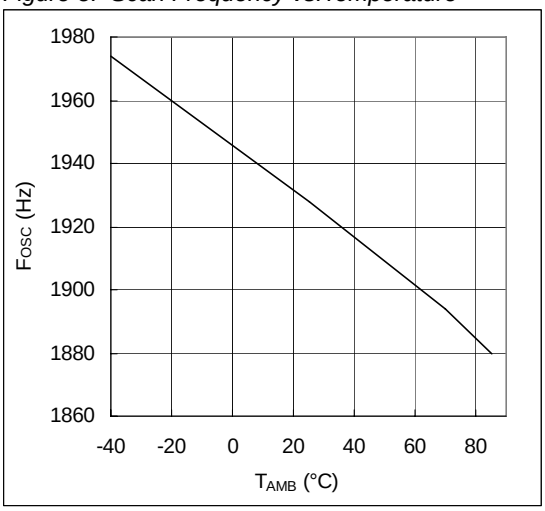


Figure 4. Scan Frequency vs. V_{DD}

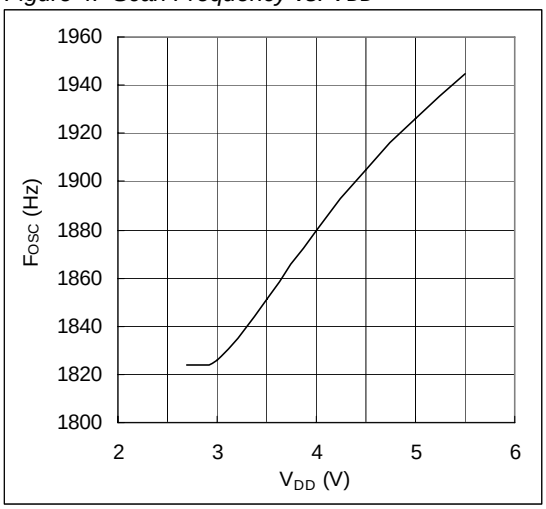


Figure 5. I_{SEG} vs. Temperature

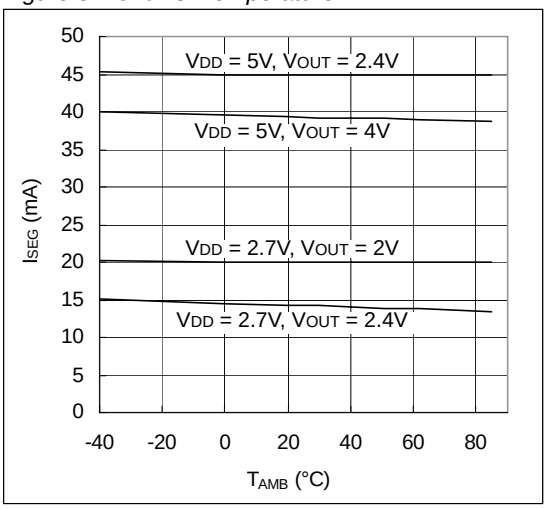


Figure 6. I_{SEG} vs. V_{DD}

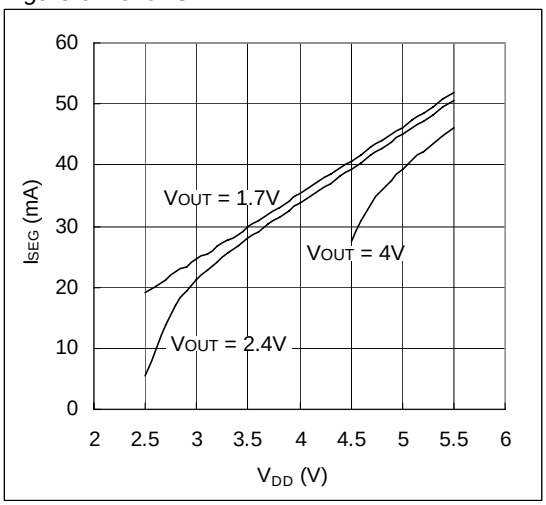


Figure 7. I_{SEG} vs. V_{OUT}

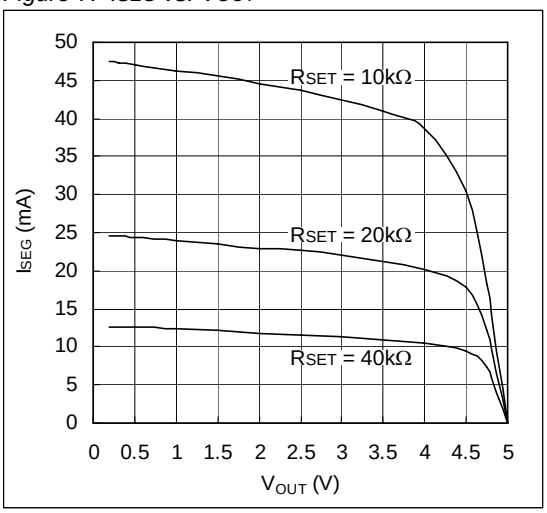


Figure 8. I_{SEG} vs. V_{OUT}

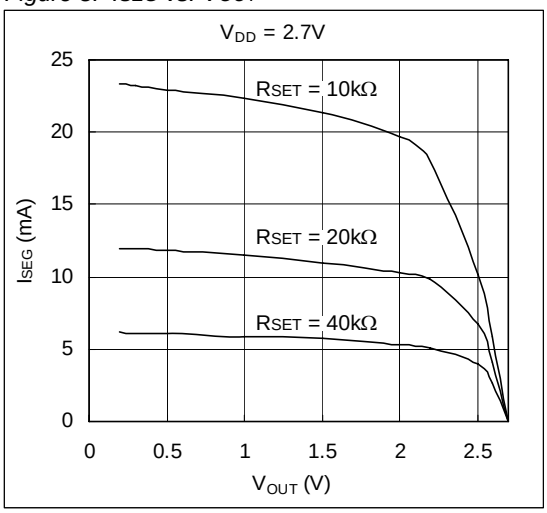
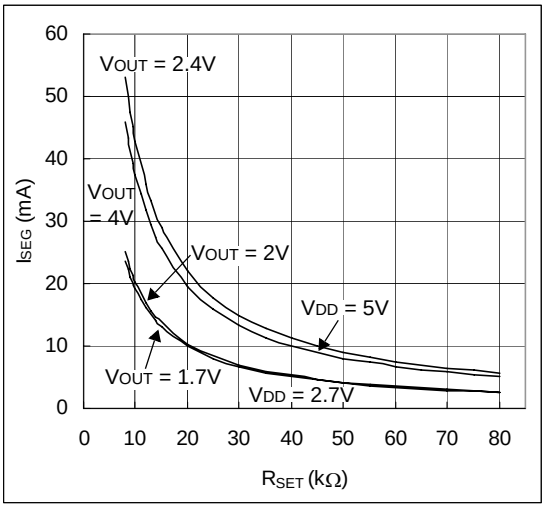


Figure 9. ISEG vs. RSET



8 Detailed Description

Serial-Addressing Format

Programming the AS1108 is accomplished by writing to the device's internal registers (see Digit- and Control-Registers on page 8) via the 4-wire serial interface. A programming sequence consists of 16-bit packages as depicted in Table 6.

The data is shifted into the internal 16-bit register with the rising edge of the CLK signal. With the rising edge of the LOAD/CSN signal the data is latched into a digit- or control-register. The LOAD/CSN signal must go high after the 16th rising clock edge.

The LOAD/CSN signal can also come later but this must happen just before the next rising edge of CLK, otherwise the data will be lost. The contents of the internal shift register are applied 16.5 clock cycles later to pin DOUT. The data is clocked out at the falling edge of CLK.

The first 4 bits (D15:D12) are "don't care" settings, bits D11:D8 contain the register address, and bits D7:D0 contain the data. The first bit is D15, the most significant bit (MSB). The exact timing is shown in Figure 10.

Table 6. 16-Bit Serial Data Format

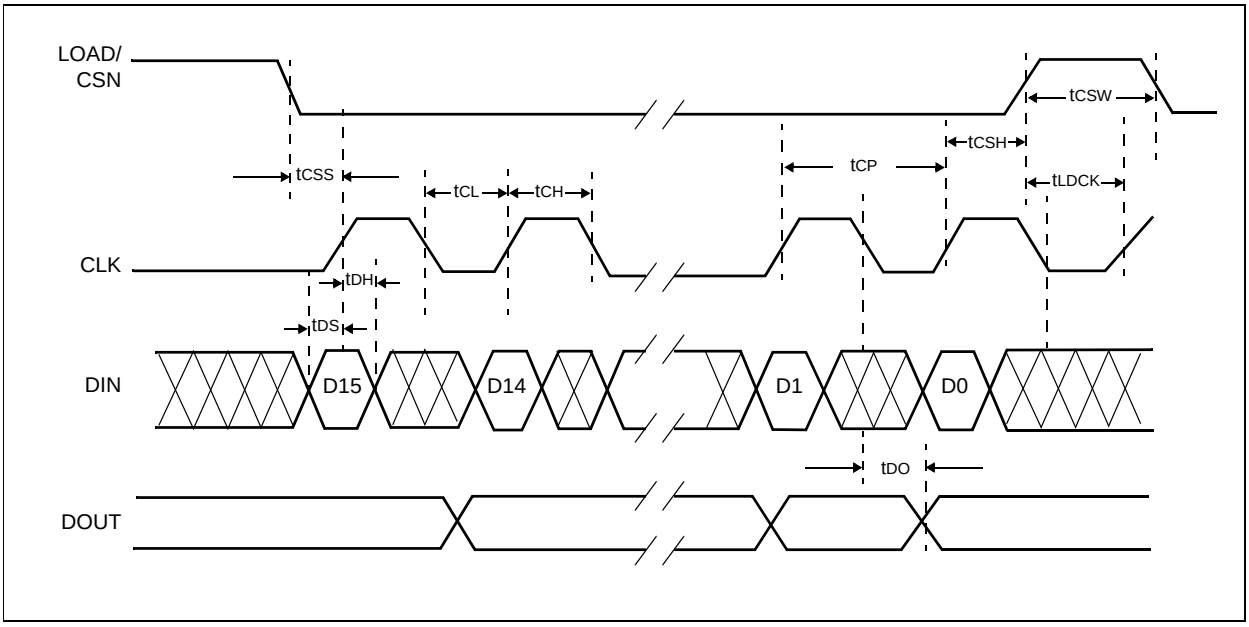
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	Register Address (see Table 7)				MSB	Data						LSB

Initial Power-Up

On initial power-up, the AS1108 registers are reset to their default values, the display is blanked, and the device goes into shutdown mode. All registers should be programmed for normal operation at this time.

Note: The default settings enable only scanning of one digit; the internal decoder is disabled and the Intensity Control Register (see page 11) is set to the minimum values.

Figure 10. Interface Timing



Shutdown Mode

The AS1108 features a shutdown mode, consuming only 10µA (max) current. Shutdown mode is entered via a write to the Shutdown Register (see Table 8). At that point, all segment current sources are pulled to ground and all digit drivers are connected to VDD, so that all segments are blanked.

Note: During shutdown mode the Digit-Registers maintain their data.

Shutdown mode can either be used as a means to reduce power consumption or for generating a flashing display (repeatedly entering and leaving shutdown mode). For minimum supply current in shutdown mode, logic input should be at GND or VDD (CMOS logic level).

The device needs typically 250µs to exit shutdown mode, and during shutdown mode the AS1108 is fully programmable. Only the display test mode (see page 10) overrides shutdown mode.

When entering or leaving shutdown mode, the Feature Register is reset to its default values (all 0s) when Shutdown Register bit D7 (page 9) = 0. When bit D7 = 1, the Feature Register is left unchanged when entering or leaving shutdown mode.

Note: If the AS1108 is used with an external clock, Shutdown Register bit D7 should be set to 1 when writing to the Shutdown Register.

Digit- and Control-Registers

The AS1108 contains four Digit-Registers and six control-registers, which are listed in Table 7. All registers are selected using a 4-bit address word, and communication is done via the serial interface.

- Digit Registers – These registers are realized with an on-chip 32-bit memory. Each digit can be controlled directly without rewriting the whole register contents.
- Control Registers – These registers consist of decode mode, display intensity, number of scanned digits, shutdown, display test and features selection registers.

Table 7. Register Address Map

Register	HEX Code	Address					Page
		D15:D12	D11	D10	D9	D8	
No-Op	0xX0	X	0	0	0	0	12
Digit 0	0xX1	X	0	0	0	1	N/A
Digit 1	0xX2	X	0	0	1	0	N/A
Digit 2	0xX3	X	0	0	1	1	N/A
Digit 3	0xX4	X	0	1	0	0	N/A
Decode-Mode	0xX9	X	1	0	0	1	9
Intensity Control	0xXA	X	1	0	1	0	11
Scan Limit	0xXB	X	1	0	1	1	11
Shutdown	0xXC	X	1	1	0	0	9
N/A	0xXD	X	1	1	0	1	N/A
Feature	0xXE	X	1	1	1	0	12
Display Test	0xXF	X	1	1	1	1	10

Shutdown Register (0xXC)

The Shutdown Register controls AS1108 shutdown mode (see Shutdown Mode on page 8).

Table 8. Shutdown Register Format (Address (HEX) = 0xXC))

Mode	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Mode, Reset Feature Register to Default Settings	0x00	0	X	X	X	X	X	X	0
Shutdown Mode, Feature Register Unchanged	0x80	1	X	X	X	X	X	X	0
Normal Operation, Reset Feature Register to Default Settings	0x01	0	X	X	X	X	X	X	1
Normal Operation, Feature Register Unchanged	0x81	1	X	X	X	X	X	X	1

Decode Enable Register (0xX9)

The Decode Enable Register sets the decode mode. BCD/HEX decoding (either BCD code – characters 0:9, E, H, L, P, and -, or HEX code – characters 0:9 and A:F) is selected by bit D2 (page 12) of the Feature Register. The Decode Enable Register is used to select the decode mode or no-decode for each digit. Each bit in the Decode Enable Register corresponds to its respective display digit (i.e., bit D0 corresponds to digit 0, bit D1 corresponds to digit 1 and so on). Table 10 lists some examples of the possible settings for the Decode Enable Register bits.

Note: A logic high enables decoding and a logic low bypasses the decoder altogether.

When decode mode is used, the decoder looks only at the lower-nibble (bits D3:D0) of the data in the Digit-Registers, disregarding bits D6:D4. Bit D7 sets the decimal point (SEG DP) independent of the decoder and is positive logic (bit D7 = 1 turns the decimal point on). Table 10 lists the code-B font; Table 11 lists the HEX font.

When no-decode mode is selected, data bits D7:D0 of the Digit-Registers correspond to the segment lines of the AS1108. Table 12 shows the 1:1 pairing of each data bit and the appropriate segment line.

Table 9. Decode Enable Register Format (Address (HEX) = 0xX9))

Decode Mode	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
No decode for digits 3:0	0x00	X	X	X	X	0	0	0	0
Code-B/HEX decode for digit 0. No decode for digits 3:1	0x01	X	X	X	X	0	0	0	1
Code-B/HEX decode for digits 3:0	0xFF	X	X	X	X	1	1	1	1

Figure 11. Standard 7-Segment LED Intensity Control and Inter-Digit Blanking

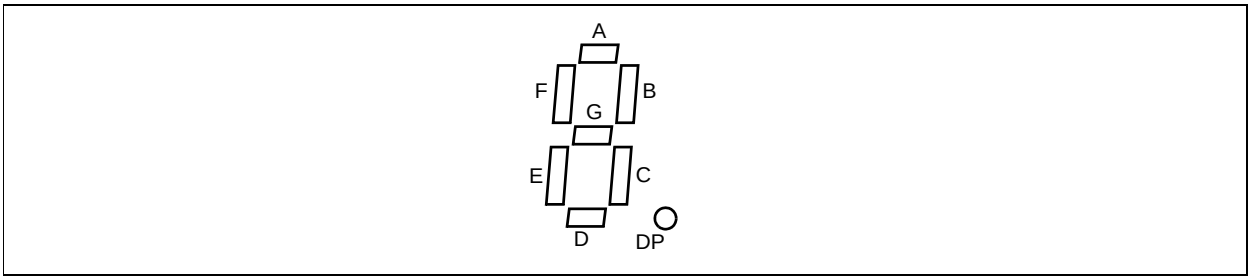


Table 10. Code-B Font

7-Segment Character	Register Data							On Segments = 1						
	D7 †	D6:D4	D3	D2	D1	D0	DP †	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1

Table 10. Code-B Font (Continued)

7-Segment Character	Register Data							On Segments = 1						
	D7 †	D6:D4	D3	D2	D1	D0	DP †	A	B	C	D	E	F	G
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
-		X	1	0	1	0		0	0	0	0	0	0	1
E		X	1	0	1	1		1	0	0	1	1	1	1
H		X	1	1	0	0		0	1	1	0	1	1	1
L		X	1	1	0	1		0	0	0	1	1	1	0
P		X	1	1	1	0		1	1	0	0	1	1	1
Blank		X	1	1	1	1		0	0	0	0	0	0	0

† The decimal point is enabled by setting bit D7 = 1.

Table 11. HEX Font

7-Segment Character	Register Data							On Segments = 1						
	D7 †	D6:D4	D3	D2	D1	D0	DP †	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
A		X	1	0	1	0		1	1	1	0	1	1	1
b		X	1	0	1	1		0	0	1	1	1	1	1
C		X	1	1	0	0		1	0	0	1	1	1	0
d		X	1	1	0	1		0	1	1	1	1	0	1
E		X	1	1	1	0		1	0	0	1	1	1	1
F		X	1	1	1	1		1	0	0	0	1	1	1

† The decimal point is enabled by setting bit D7 = 1.

Table 12. No-Decode Mode Data Bits and Corresponding Segment Lines

	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding Segment Line	DP	A	B	C	D	E	F	G

Display-Test Register (0xXF)

The AS1108 can operate in two modes: normal mode and display test mode. In display test mode all LEDs are switched on at maximum brightness (duty cycle is 15/16). The device remains in display-test mode until the Display-Test Register is set for normal operation.

Note: All settings of the Digit- and Control-Registers are maintained.

Table 13. Display-Test Register Format (Address (HEX) = 0xXF))

Mode	Register Data							
	D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation	X	X	X	X	X	X	X	0
Display Test Mode	X	X	X	X	X	X	X	1

Intensity Control Register (0xXA)

The brightness of the display can be controlled by digital means using the Intensity Control Register and by analog means using RSET (see Selecting RSET Resistor Value and Using External Drivers on page 13).

Display brightness is controlled by an integrated pulse-width modulator which is controlled by the lower-nibble of the Intensity Control Register. The modulator scales the average segment-current in 16 steps from a maximum of 31/32 down to 1/32 of the peak current set by RSET.

Table 14. Intensity Register Format (Address (HEX) = 0xXA))

Duty Cycle	HEX Code	Register Data							
AS1108		D7	D6	D5	D4	D3	D2	D1	D0
1/32 (min on)	0xX0	X	X	X	X	0	0	0	0
3/32	0xX1	X	X	X	X	0	0	0	1
5/32	0xX2	X	X	X	X	0	0	1	0
7/32	0xX3	X	X	X	X	0	0	1	1
9/32	0xX4	X	X	X	X	0	1	0	0
11/32	0xX5	X	X	X	X	0	1	0	1
13/32	0xX6	X	X	X	X	0	1	1	0
15/32	0xX7	X	X	X	X	0	1	1	1
17/32	0xX8	X	X	X	X	1	0	0	0
19/32	0xX9	X	X	X	X	1	0	0	1
21/32	0xXA	X	X	X	X	1	0	1	0
23/32	0xXB	X	X	X	X	1	0	1	1
25/32	0xXC	X	X	X	X	1	1	0	0
27/32	0xXD	X	X	X	X	1	1	0	1
29/32	0xXE	X	X	X	X	1	1	1	0
31/32 (max on)	0xXF	X	X	X	X	1	1	1	1

Scan-Limit Register (0x0B)

The Scan-Limit Register controls which of the digits are to be displayed. When all 4 digits are to be displayed, the update frequency is typically 1600Hz. If the number of digits displayed is reduced, the update frequency is increased. The frequency can be calculated using 8fOSC/N, where N is the number of digits. Since the number of displayed digits influences the brightness, RSET should be adjusted accordingly. Table 16 lists the maximum allowed current when fewer than 4 digits are used.

Note: To avoid differences in brightness this register should not be used to blank parts of the display (leading zeros).

Table 15. Scan-Limit Register Format (Address (HEX) = 0xXB))

Scan Limit	HEX Code	Register Data							
		D7	D6	D5	D4	D3	D2	D1	D0
Display digit 0 only (see Table 16)	0xX0	X	X	X	X	X	0	0	0
Display digits 0:1 (see Table 16)	0xX1	X	X	X	X	X	0	0	1
Display digits 0:2 (see Table 16)	0xX2	X	X	X	X	X	0	1	0
Display digits 0:3	0xX3	X	X	X	X	X	0	1	1

Table 16. Maximum Segment Current for 1-, 2-, or 3-Digit Displays

Number of Digits Displayed	Maximum Segment Current (mA)
1	10
2	20
3	30

Feature Register (0xXE)

The Feature Register is used for switching the device into external clock mode, applying an external reset, selecting code-B or HEX decoding, enabling or disabling blinking, enabling or disabling the SPI-compatible interface, setting the blinking rate, and resetting the blink timing.

Note: At power-up the Feature Register is initialized to 0.

Table 17. Feature Register Summary

D7	D6	D5	D4	D3	D2	D1	D0
blink_ start	sync	blink_ freq_sel	blink_en	spi_en	decode_sel	reg_res	clk_en

Table 18. Feature Register Bit Descriptions (Address (HEX) = 0xXE))

Addr: 0xXE		Feature Register		
		Enables and disables various device features.		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
D0	clk_en	0	R/W	External clock select. 0 = Internal oscillator is used for system clock. 1 = Pin CLK of the serial interface operates as system clock input.
D1	reg_res	0	R/W	Resets all control registers except the Feature Register. 0 = Reset Disabled. Normal operation. 1 = All control registers are reset to default state (except the Feature Register) identically after power-up. **Note:** The Digit Registers maintain their data.
D2	decode_sel	0	R/W	Selects display decoding. 0 = Enable Code-B decoding (see Table 10 on page 9). 1 = Enable HEX decoding (see Table 11 on page 10).
D3	spi_en	0	R/W	Enables the SPI-compatible interface. 0 = Disable SPI-compatible interface. 1 = Enable the SPI-compatible interface.
D4	blink_en	0	R/W	Enables blinking. 0 = Disable blinking. 1 = Enable blinking.
D5	blink_freq_sel	0	R/W	Sets blink with low frequency (with the internal oscillator enabled): 0 = Blink period typically is 1 second (0.5s on, 0.5s off). 1 = Blink period is 2 seconds (1s on, 1s off).
D6	sync	0	R/W	Synchronizes blinking on the rising edge of pin LOAD/CSN. The multiplex and blink timing counter is cleared on the rising edge of pin LOAD/CSN. By setting this bit in multiple AS1108 devices, the blink timing can be synchronized across all the devices.
D7	blink_start	0	R/W	Start Blinking with display enabled phase. When bit D4 (blink_en) is set, bit D7 determines how blinking starts. 0 = Blinking starts with the display turned off. 1 = Blinking starts with the display turned on.

No-Op Register (0xX0)

The No-Op Register is used when multiple AS1108 devices are cascaded in order to support displays with more than 4 digits. The cascading must be done in such a way that all DOUT pins are connected to DIN of the next AS1108 (see Figure 12 on page 15). The LOAD/CSN and CLK signals are connected to all devices.

For example, if five devices are cascaded, in order to perform a write operation to the fifth device, the write-command must be followed by four no-operation commands. When the LOAD/CSN signal goes high, all shift registers are latched. The first four devices will receive no-operation commands and only the fifth device will receive the intended operation command, and subsequently update its register.

9 Typical Application

Supply Bypassing and Wiring

In order to achieve optimal performance the AS1108 should be placed very close to the LED display to minimize effects of electromagnetic interference and wiring inductance.

Furthermore, a 10µF electrolytic and a 0.1µF ceramic capacitor should be connected between pins VDD and GND to avoid power supply ripple (see Figure 12 on page 15).

Note: Both GND pins must be connected to ground.

Selecting RSET Resistor Value and Using External Drivers

Brightness of the display segments is controlled via RSET. The current that flows between VDD and ISET defines the current that flows through the LEDs.

Segment current is about 200 times the current in ISET. Typical values for RSET for different segment currents, operating voltages, and LED voltage drop (VLED) are given in Tables 19 - 23. The maximum current the AS1108 can drive is 40mA. If higher currents are needed, external drivers must be used, in which case it is no longer necessary that the device drive high currents.

In cases where the device drives only a few digits, Table 16 specifies the maximum currents, and RSET must be set accordingly.

Note: The display brightness can also be logically controlled (see Selecting RSET Resistor Value and Using External Drivers on page 13).

Table 19. RSET vs. Segment Current and LED Forward Voltage, VDD = 2.7V

ISEG (mA)	VLED(V)	
	1.5	2.0
40	5kΩ	4.4kΩ
30	6.9kΩ	5.9kΩ
20	10.7kΩ	9.6kΩ
10	22.2kΩ	20.7kΩ

Table 20. RSET vs. Segment Current and LED Forward Voltage, VDD = 3.3V

ISEG (mA)	VLED(V)		
	1.5	2.0	2.5
40	6.7kΩ	6.4kΩ	5.7kΩ
30	9.1kΩ	8.8kΩ	8.1kΩ
20	13.9kΩ	13.3kΩ	12.6kΩ
10	28.8kΩ	27.7kΩ	26kΩ

Table 21. RSET vs. Segment Current and LED Forward Voltage, VDD = 3.6V

ISEG (mA)	VLED(V)			
	1.5	2.0	2.5	3.0
40	7.5kΩ	7.2kΩ	6.6kΩ	5.5kΩ
30	10.18kΩ	9.8kΩ	9.2kΩ	7.5kΩ
20	15.6kΩ	15kΩ	14.3kΩ	13kΩ
10	31.9kΩ	31kΩ	29.5kΩ	27.3kΩ

Table 22. RSET vs. Segment Current and LED Forward Voltage, VDD = 4.0V

ISEG (mA)	VLED(V)				
	1.5	2.0	2.5	3.0	3.5
40	8.6kΩ	8.3kΩ	7.9kΩ	7.6kΩ	5.2kΩ
30	11.6kΩ	11.2kΩ	10.8kΩ	9.9kΩ	7.8kΩ

Table 22. R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD} = 4.0V (Continued)

I_{SEG} (mA)	V_{LED}(V)				
	1.5	**2.0**	**2.5**	**3.0**	**3.5**
20	17.7kΩ	17.3kΩ	16.6kΩ	15.6kΩ	13.6kΩ
10	36.89kΩ	35.7kΩ	34.5kΩ	32.5kΩ	29.1kΩ

Table 23. R_{SET} vs. Segment Current and LED Forward Voltage, V_{DD} = 5.0V

I_{SEG} (mA)	V_{LED} (V)					
	1.5	**2.0**	**2.5**	**3.0**	**3.5**	**4.0**
40	11.35kΩ	11.12kΩ	10.84kΩ	10.49kΩ	10.2kΩ	9.9kΩ
30	15.4kΩ	15.1kΩ	14.7kΩ	14.4kΩ	13.6kΩ	13.1kΩ
20	23.6kΩ	23.1kΩ	22.6kΩ	22kΩ	21.1kΩ	20.2kΩ
10	48.9kΩ	47.8kΩ	46.9kΩ	45.4kΩ	43.8kΩ	42kΩ

Table 24. Package Thermal Data

Package	Thermal Resistance (Θ_{JA})
20 Narrow DIP	+75°C/W
20 Wide SOIC	+85°C/W

4x8 LED Dot Matrix Driver

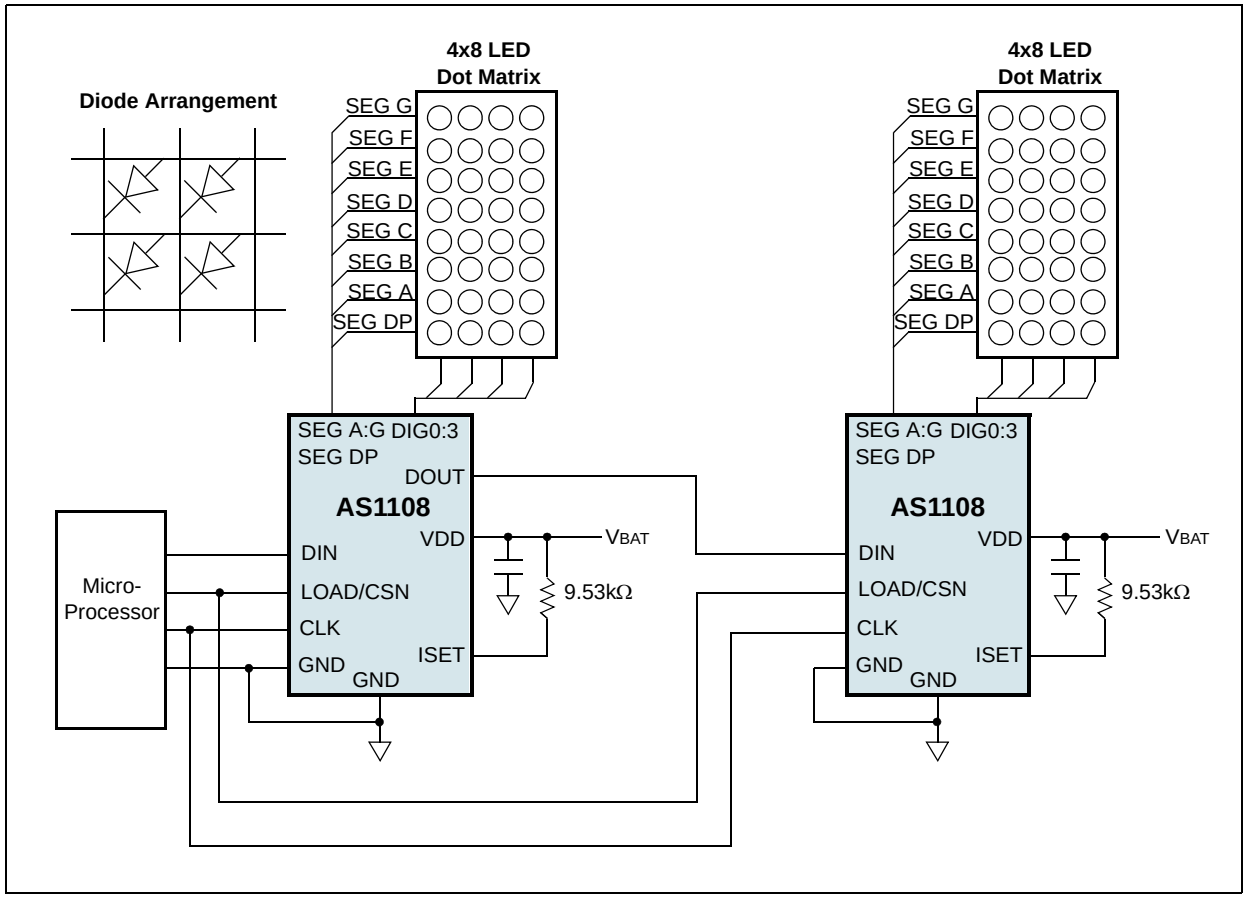
The application example in Figure 12 shows the AS1108 as a 4x8 LED dot matrix driver.

The LED columns have common cathodes and are connected to the DIG0:3 outputs. The rows are connected to the segment drivers. Each of the 32 LEDs can be addressed separately. The columns are selected via the digits as listed in Table 7 on page 8.

The Decode Enable Register (see page 9) must be set to '00000000' as described in Table 9 on page 9. Single LEDs in a column can be addressed as described in Table 12 on page 10, where bit D0 corresponds to segment G and bit D7 corresponds to segment DP.

Note: For a multiple-digit dot matrix, multiple AS1108 devices must be cascaded.

Figure 12. Application Example as LED Dot Matrix Driver



Cascading Drivers

If more than 4 digits or 32 LEDs are needed, it is recommended to use the AS1106/AS1107, although several AS1108 devices can be cascaded.

The example in Figure 4 drives 2 dot matrix digits using a 4-wire microprocessor interface. All Scan-Limit Registers should be set to the same value so that one display will not appear brighter than the other.

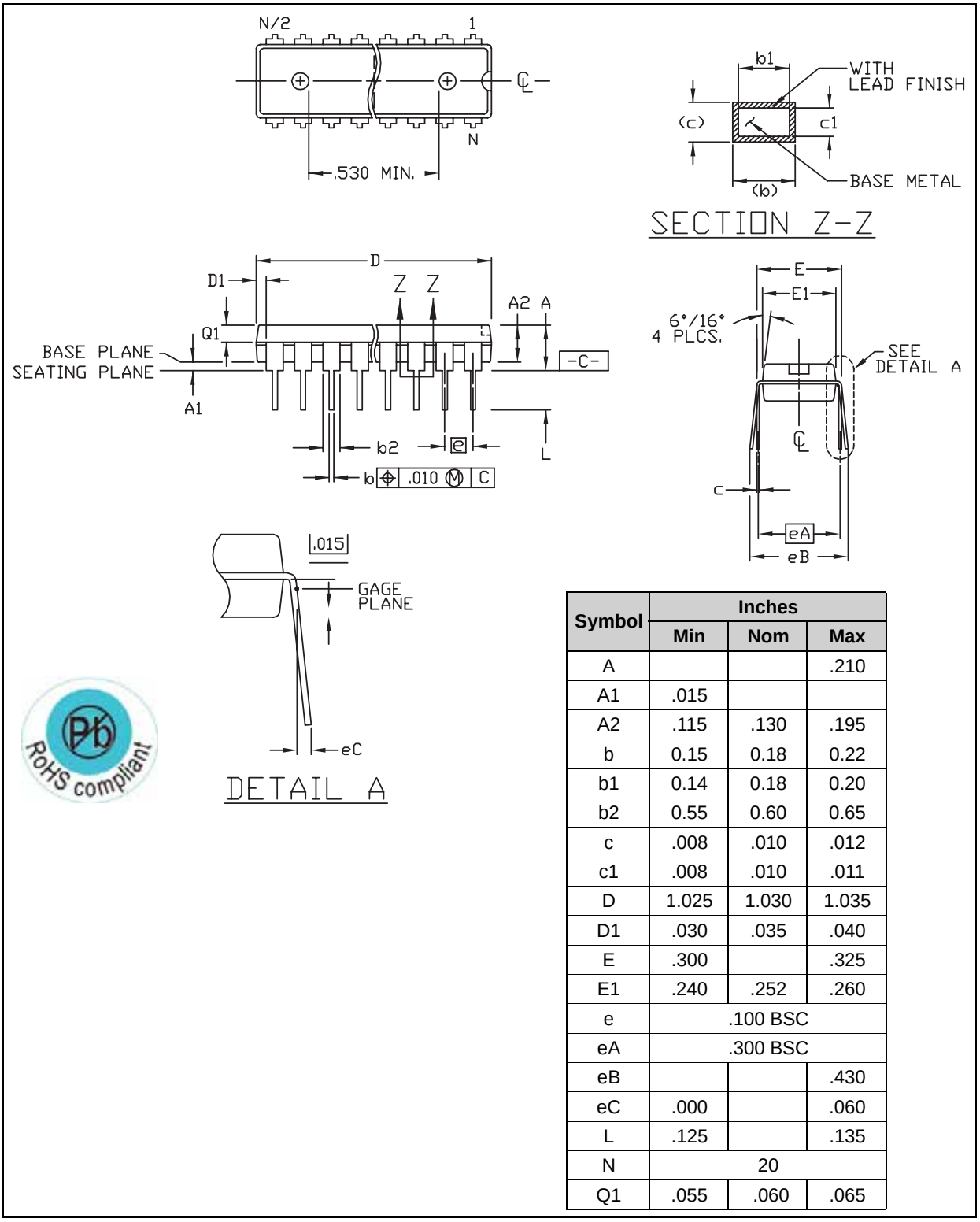
For example, to display 6 digits, set both Scan-Limit Registers to display 3 digits so that both displays have a 1/3 duty cycle per digit. If 5 digits are needed, set both Scan-Limit Registers to display 3 digits and leave one digit unconnected. Otherwise, if one driver is set to display 3 digits and the other to display 2 digits one display will appear brighter because its duty cycle per digit will be 1/2 and the other display's duty cycle will be 1/3.

Note: Refer to No-Op Register (0xX0) on page 12 for additional information.

10 Package Drawings and Markings

The AS1108 is available in a PDIP 20-pin[1] and a SOIC 20-pin package.

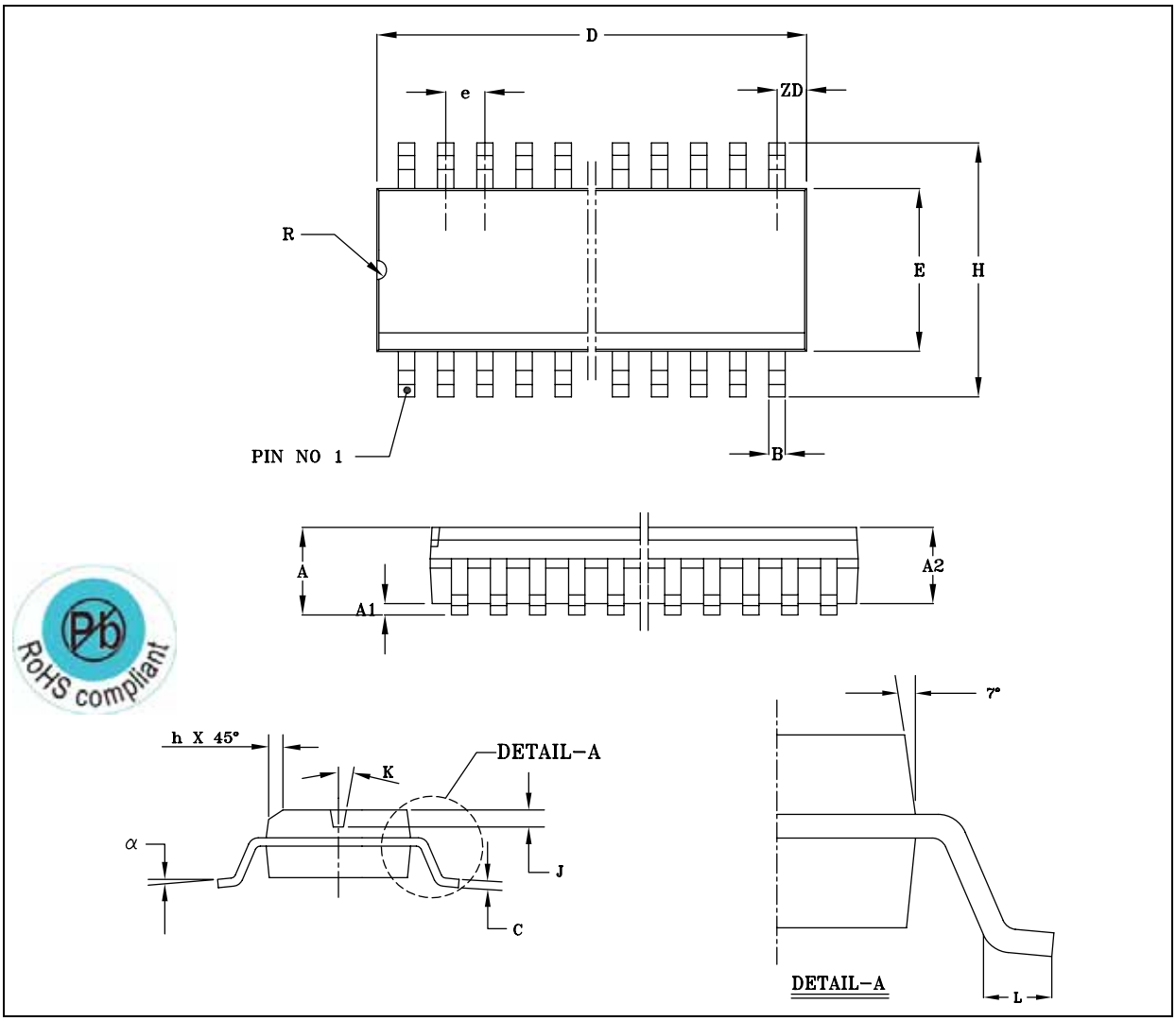
Figure 13. PDIP 20-pin *Package*



Symbol	Inches		
	Min	Nom	Max
A			.210
A1	.015		
A2	.115	.130	.195
b	0.15	0.18	0.22
b1	0.14	0.18	0.20
b2	0.55	0.60	0.65
c	.008	.010	.012
c1	.008	.010	.011
D	1.025	1.030	1.035
D1	.030	.035	.040
E	.300		.325
E1	.240	.252	.260
e	.100 BSC		
eA	.300 BSC		
eB			.430
eC	.000		.060
L	.125		.135
N	20		
Q1	.055	.060	.065

1. For more Information on the PDIP 20-pin package see Ordering Information on page 18.

Figure 14. SOIC 20-pin *Package*



Notes:

1. Lead coplanarity should be 0 to 0.10mm (.004”) max.
2. Package surface finishing:
   (2.1) Top: matte (charmilles #18-30).
   (2.2) All sides: matte (charmilles #18-30).
   (2.3) Bottom: smooth or matte (charmilles #18-30).
3. All dimensions exclusive of mold flash, and end flash from the package body shall not exceed 0.24mm (0.10”) per side (D).

Symbol	Millimeters	
	Min	Max
A	2.44	2.64
A1	0.10	0.30
A2	2.24	2.44
B	0.36	0.46
C	0.23	0.32
D	12.65	12.85
E	7.40	7.60
e	1.27 BSC	
H	10.11	10.51
h	0.31	0.71
J	0.53	0.73
K	7º BSC	
L	0.51	1.01
R	0.63	0.89
ZD	0.66 REF	
α	0º	8º

11 Ordering Information

The AS1108 is available as the standard products shown in Table 25.

Table 25. Ordering Information

Ordering Code	Description	Temperature Range	Delivery Form	Package
AS1108PL*	4-Digit LED Display Driver	0 to +70ºC	Tubes	PDIP 20-pin
AS1108WL	4-Digit LED Display Driver	0 to +70ºC	Tubes	SOIC 20-pin
AS1108WL-T	4-Digit LED Display Driver	0 to +70ºC	Tape and Reel	SOIC 20-pin

*) The PDIP 20-pin Package reached end of life. There is the possibility for a last time buy order until end of July 2011.

Note: All products are RoHS compliant.
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or find your local distributor at http://www.austriamicrosystems.com/distributor

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